Correlations between Radiation Hardness and Variations of FFs Denpending on Layout Structures in a 28 nm Thin BOX FD-SOI Process by Alpha Particles Irradiation

Haruki Maruoka, Masashi Hifumi, Shohei Kanda, Jun Furuta and Kazutoshi Kobayashi
Kyoto Institute of Technology, Japan

***Abstract*— We design three different layouts of DFFs in a 28 nm thin-BOX FD-SOI process to compare their radiation hardness. We measure them by alpha-particle irradiation. Experimental results show that the soft-error probability of two-fingered inverters is 2.6x higher than that of one-fingered one at 0.4 V when DATA and CLK are 1 and 0 respectively. We also measure the relationship between process variations and radiation hardness in each FF. The process variation affects retention voltage of FFs. FFs with higher retention voltage are more vulnerable to radiation than FFs with lower retention voltage.**

I. Introduction

As transistors become downscaling, semiconductor chips become weak to soft errors. They are caused by alpha particles from packages and neutrons from cosmic ray. Single Event Upset (SEU) is a phenomenon that keeping value in FFs and SRAMs are upset by these particles. By rebooting devices, erroneous values are restored. Highly-reliable devices need to equip prevention against soft errors.

Variations of MOSFETs also become serious [1]. SOI processes have smaller variations of threshold voltages than bulk processes because of undoped channels [2]. However, the thickness of body, oxide charge and work functions of metal gates affect the variations [3]. In the SOI processes fewer charge is collected than bulk processes because BOX layers prevent charge collection. Thus, they also have higher soft error tolerance [4].

In this paper, we investigate the radiation hardness by alpha particle irradiation. It is reported in [5] and [6] that bulk processes have a limited effect on alpha SER by process corners. We also investigate the relationship between process variations and radiation hardness in a 28 nm Ultra Thin Body & BOX (UTBB) process. Section II explains the designed layout structures of DFF. Section III shows the experimental results of SEUs by alpha particle irradiation depending on DATA and CLK states. Section IV shows correlations between the process variations and radiation hardness. Section V concludes this paper.

II. Designed Layouts of DFF in a 28 nm UTBB FD-SOI Process

Fig. 1 shows the cross section of the 28 nm UTBB FD-SOI process with 7 nm SOI layers and 25 nm BOX layers. We design three different layouts of DFF (Fig. 2) to investigate the effect of layout structures and shallow trench isolations (STI) to isolate MOSFETs. Layout structures and STI affect MOSFET characteristics. We focused on process variations depending on layout structures. We design the following three different layout structures.

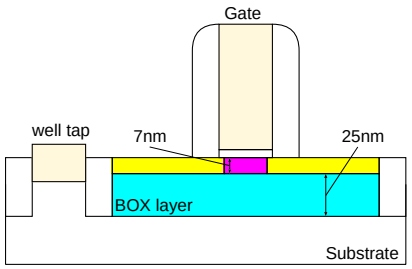


Fig. 1. Cross section of UTBB FD-SOI structure.

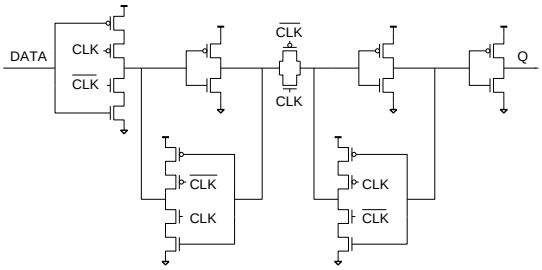


Fig. 2. Conventional FF (DFF).

L0 Diffusions in the slave latch are divided (Fig. 3(a)).
L1 Diffusions in the slave latch are shared (Fig. 3(b)).
L2 Diffusions in the slave latch are shared (Fig. 3(c)). It has two-fingered inverters in the slave latch.

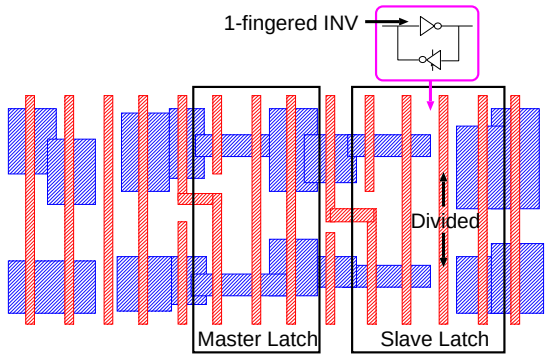
Note that the schematic, sensitive area of DFF and three layout structures in the master latch are equivalent. Fig. 4 shows the fabricated chip with the triple-well structure in a 28 nm UTBB FD-SOI process. Each FF array contains 14,700 bit. Table I indicates simulation results of C-Q delay and dynamic power of each layout at 1.0 V. All values are normalized to those of L0. Each value is almost same because we do not consider the effect of process variation or STI.

III. Static Measurement of Radiation Hardness Depending on DATA and CLK

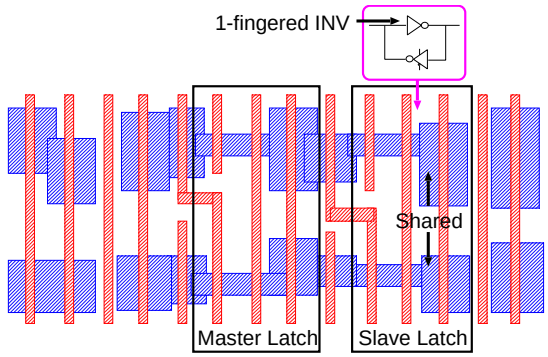
Fig. 5 shows the measurement setup of alpha particle irradiation. A 3M Bq ^{241}Am is used in the experiment. Alpha

TABLE I
C-Q Delay and Power of each FF. All values are normalized to those of L0.

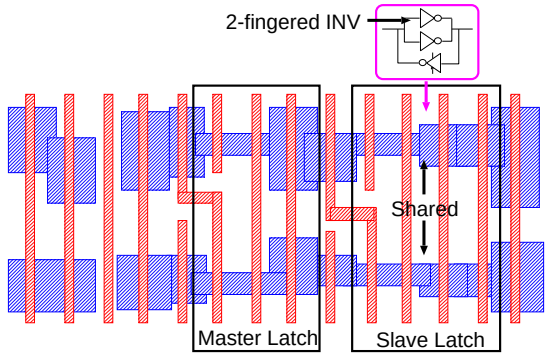
Layout	L0	L1	L2
C-Q Delay	1	0.98	1.03
Power ($\alpha = 10\%$)	1	0.98	0.99



(a) L0 : Layout which diffusions in the slave latch are divided.



(b) L1 : Layout which diffusions in the slave latch are shared.



(c) L2 : Layout with two-fingered inverters.

Fig. 3. Designed DFFs with different layout structures.

particle flux is 3×10^6 $\mathrm{cm^{-2}s^{-1}}$. The irradiation time is 10 min. We measure these static conditions (DATA, CLK) = (0, 0), (0, 1), (1, 0) and (1, 1). Upset transistors by radiation depend on DATA and CLK states. When (DATA, CLK) = (1, 0), the tri-state inverter in the slave latch is vulnerable. Soft error hardness is evaluated by the soft error probability (P_{SE}).

$$P_{\mathrm{SE}} = \frac{N_{\mathrm{SE}}}{N_{\mathrm{bit}}} \quad (1)$$

Where N_{SE} is the number of errors by alpha particle irradiation and N_{bit} is the number of total bits of each FF array. The error bars show 95% confidence.

Fig. 6 shows the results of P_{SE} at 0.4 V in each condition. Except for (DATA, CLK) = (1, 0), P_{SE} of each layout is almost equivalent. P_{SE} of L2, which has two-fingered

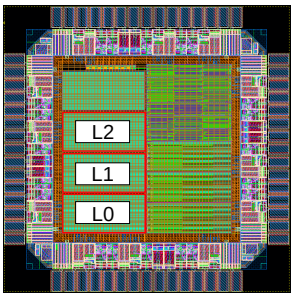


Fig. 4. Fabricated test chip.

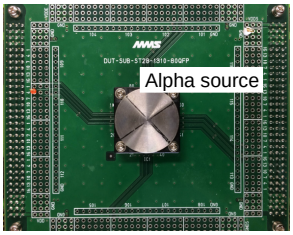


Fig. 5. Alpha test setup.

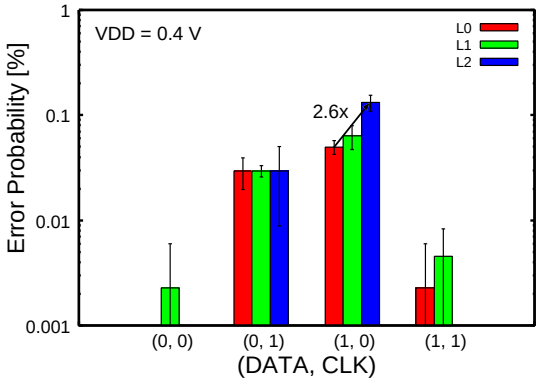


Fig. 6. P_{SE} in each condition by alpha particle irradiation. The error bars show 95% confidence.

inverters in the slave latch, is 2.6x more than that of L0 when (DATA, CLK) = (1, 0).

The radiation hardness is evaluated by critical charge (Q_{crit}) with SPICE simulations [7]. Table II shows Q_{crit} by process corners at 0.4 V when (DATA, CLK) = (1, 0). Q_{crit} of the latch with Fast-Fast decreases by 7 % as compared with Nominal. On the other hand, Q_{crit} of the latch with Slow-Slow increases by 4 %. Therefore, the combination of V_{th} affects its radiation hardness. We investigate the reason why the two-fingered inverters cause soft error vulnerability in the following section.

IV. The Relationship between the σ_{Vth} and Radiation Hardness

A. Flipped FFs by Reducing Supply Voltage

The standard deviation, σ_{Vth} of MOSFETs follows the normal distribution. We focus on MOSFETs away from nominal V_{th} (Fig. 7). We assume that they are more sensitive to soft errors than those near nominal V_{th}. We measure the minimum retention voltage of each layout by reducing supply voltage without the alpha source. Fig. 8 (a) and (b) show the

TABLE II

Q_{crit} SIMULATION RESULTS BY PROCESS CORNERS AT 0.4 V.

Process corner (PMOS-NMOS)	Q_{crit} [fC]
Nominal	0.28
Slow-Slow	0.29
Slow-Fast	0.28
Fast-Slow	0.28
Fast-Fast	0.26

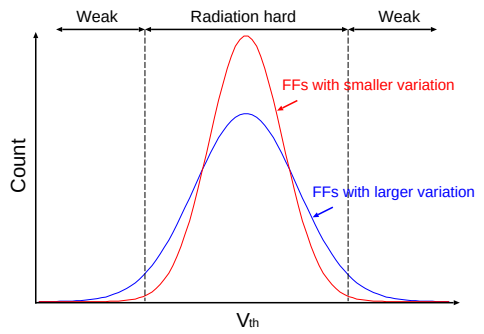
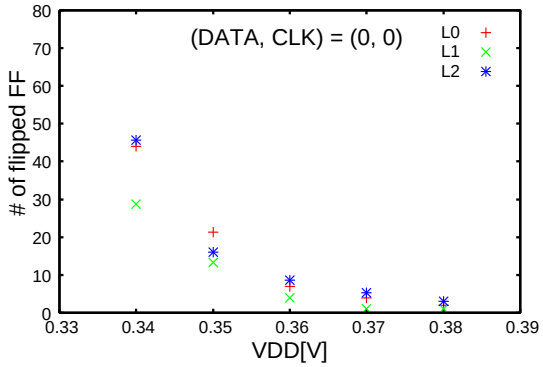
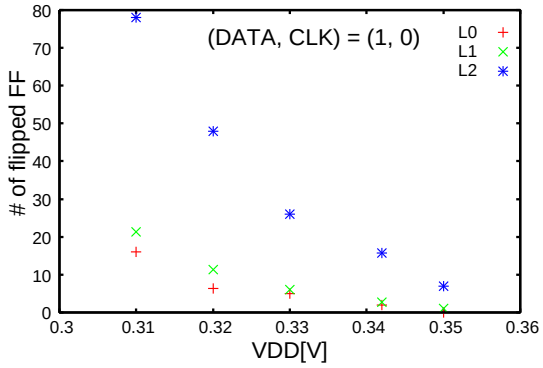


Fig. 7. Difference of radiation hardness depending on variation of MOSFETs.



(a) (DATA, CLK) = (0, 0).



(b) (DATA, CLK) = (1, 0).

Fig. 8. Flipped FFs by reducing supply voltage.

number of flipped FFs when (DATA, CLK) = (0, 0) and (1, 0) respectively. The number of flipped FFs of each layout is almost same when (DATA, CLK) = (0, 0). On the other hand, the number of flipped FFs of L2 is 4x more than the other layouts at 0.31 V when (DATA, CLK) = (1, 0). The layout including two-fingered inverters has the largest σ_{Vth}. The standard deviation σ_{Vth} is proportionally to $1/\sqrt{LW}$ [3]. If we use two-fingered inverters, the σ_{Vth} of MOSFETs in each inverter of L2 is $\sqrt{2}$x more than the one-fingered one in L0 or L1. The σ_{Vth} of two-fingered inverters is also larger than the one-fingered inverter because there are some amount of correlations since they are placed closely.

TABLE III
EXPERIMENTAL RESULTS OF $N_{(\mathrm{SE\&VAR})}$, N_{VAR} AND N_{SE} IN EACH LAYOUT.

Layout	$N_{(\mathrm{SE\&VAR})}$			N_{VAR}			N_{SE}		
	L0	L1	L2	L0	L1	L2	L0	L1	L2
# of FF	0.33	0.67	2.67	34	50	115	10.3	19.3	37.7

B. Correlations between Retention Voltage and Radiation Hardness

We investigate the relationship between retention voltage and radiation hardness of each layout. All measurements are conducted when (DATA, CLK) = (1, 0). First, we measure the number of flipped FFs (N_{VAR}) by reducing supply voltage without placing the alpha source. Then, we measure the number of upset FFs (N_{SE}) with the alpha source at 0.42 V, at which no flipped FF appears. The irradiation time is 30 min. Eq. 2 and 3 show the evaluation formulas of the relationship between the process variation and radiation hardness respectively.

$$\varepsilon_{\mathrm{H}} = \frac{N_{(\mathrm{SE\&VAR})}}{N_{\mathrm{VAR}}} \quad (2)$$

$$\varepsilon_{\mathrm{L}} = \frac{N_{\mathrm{SE}} - N_{(\mathrm{SE\&VAR})}}{N_{\mathrm{bit}} - N_{\mathrm{VAR}}} \quad (3)$$

Where $N_{(\mathrm{SE\&VAR})}$ is the number of FFs flipped by reducing supply voltage and upset by alpha particle irradiation. ε_{H} means the error probability that FFs with higher retention voltage upset by alpha particle irradiation. ε_{L} means the error probability that FFs with lower retention voltage upset by alpha particle irradiation. The error bars show 95% confidence.

Table III indicates the number of $N_{(\mathrm{SE\&VAR})}$, N_{VAR} and N_{SE} in each layout. Fig. 9 shows the experimental results between flipped FFs at 0.32 V and upset FFs by alpha particle irradiation in each layout. There is no correlation between retention voltage and the radiation hardness of L0 because the error bar of ε_{H} is located within ε_{L}. There is also no correlation between retention voltage and radiation hardness of L1. By increasing the number of measurements, the error bar of ε_{H} in L1 may be located within error bar ε_{L} because the number of $N_{(\mathrm{SE\&VAR})}$ is much less than that of L2. Therefore, the process variations in L0 and L1 do not affect radiation hardness. The results of L2 clearly show the difference of radiation hardness between ε_{H} and ε_{L}. ε_{H} is 10x more vulnerable than ε_{L}. In L2 with larger σ_{Vth}, the process variations affect the radiation hardness.

V. CONCLUSION

Layout with two-fingered inverter has 2.6x more vulnerable than layout with one-fingered one by alpha particle irradiation. We focus on the relationship between process variations and radiation hardness. The latch composed of an inverter and a tri-state inverter becomes unstably due to combination of variations. Decreasing retention voltage contributes to soft error hardness. It clearly shows that FFs with higher retention voltage are 10x more vulnerable than

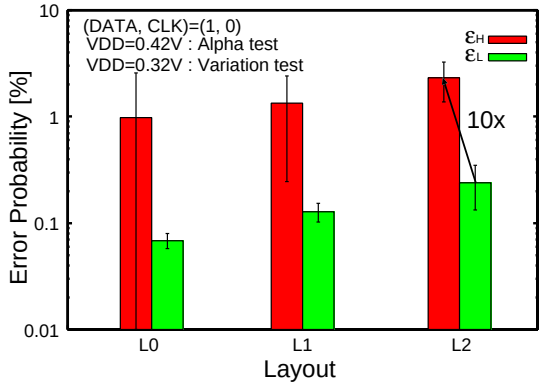


Fig. 9. Experimental results between the retention voltage and the radiation hardness of each FF. The Error bars show 95% confidence.

FFs with lower retention voltage. FFs with lower variations are strong against soft errors.

Acknowledgment: The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC) and ST Microelectronics in collaboration Cadence Corporation, Synopsys Corporation, Mentor Graphics Corporation. This work is supported by STARC and JSPS KAKENHI Grant Number 15H02677.

REFERENCES

[1] M. Pelgrom, A. C. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *JSSC*, vol. 24, no. 5, pp. 1433–1439, Oct 1989.

[2] N. Sugii, R. Tsuchiya, T. Ishigaki, Y. Morita, H. Yoshimoto, and S. Kimura, "Local $v_{\rm th}$ variability and scalability in silicon-on-thin-box (SOTB) CMOS with small random-dopant fluctuation," *Trans on EDS*, vol. 57, no. 4, pp. 835–845, April 2010.

[3] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," in *IEDM*, Dec 2008, pp. 1–4.

[4] P. Roche, J.-L. Autran, G. Gasiot, and D. Munteanu, "Technology downscaling worsening radiation effects in bulk: SOI to the rescue," in *IEDM*, Dec 2013, pp. 31.1.1–31.1.4.

[5] G. Gasiot, M. Glorieux, S. Uznanski, S. Clerc, and P. Roche, "Experimental characterization of process corners effect on SRAM alpha and neutron soft error rates," in *IRPS*, April 2012, pp. 3C.4.1–3C.4.5.

[6] N. Gaspard, S. Jagannathan, Z. Diggins, A. Kauppila, T. Loveless, J. Kauppila, B. Bhuva, L. Massengill, W. Holman, A. Oates, Y. Fang, S. Wen, and R. Wong, "Effect of threshold voltage implants on single-event error rates of D flip-flops in 28-nm bulk CMOS," in *IRPS, 2013 IEEE International*, April 2013, pp. SE.7.1–SE.7.3.

[7] P. Hazucha and C. Svensson, "Impact of CMOS technology scaling on the atmospheric neutron soft error rate," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2586–2594, 2000.