A Low-Power and Area-Efficient Radiation-Hard Redundant Flip-Flop: DICE ACFF

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***Abstract*—Process scaling makes LSI less reliable to soft errors. In this paper, we propose a low-power area-efficient redundant flip-flops for soft errors, called DICE-ACFF. Its structure is based on the reliable DICE (Dual Interlocked storage CEll) and the low-power ACFF (Adaptive-Coupled Flip-Flop). It achieves lower power at lower data-activity. We designed DICE-FF and DICE-ACFF in a 65nm process. Its area is twice as large as conventional DFFs. As for power dissipation, DICE ACFF achieves lower power than the conventional DFF below 20% data activity. When data Activity is 0%, its power is half of the DFF. As for soft error rates DICE ACFFs are 1.5x stronger than conventional DICE FFs by circuit-level critical charge estimations.**

I. Introduction

Process scaling makes LSI less reliable to soft errors. High performance computers (HPCs) are struggling with the power wall. Power consumption eliminates performance of HPCs. They are also very sensitive to soft errors since over several thousands of CPUs have to keep on running without error for a few days. Soft errors are caused by a particle hit. Neutrons are coming from cosmic ray and alpha particles are from radioactive impurities embedded in packages, bonding wires and so on. Memory cells or latches are flipped if some amount of charge is generated due to the particle hits. To reduce soft error rates, various redundant flip-flop structures are proposed, for example, TMR (Triple Modular Redundancy)[1] and DICE (Dual Interlocked storage CEll)[2]. They employ various radiation-hard techniques, but large area and power overhead are required. In this paper, We propose a low-power area-efficient redundant flop-flops for soft errors, called DICE-ACFF. Its structure is based on the reliable DICE and the low-power ACFF (adaptive-coupled Flip-flop)[3].

II. DICE-ACFF

Fig. 1 shows the proposed low-power area-efficient redundant radiation-hard flip-flops, called DICE-ACFF. Its structure is based on the reliable DICE (Fig. 2) and the low-power ACFF (Fig. 3).

The DICE structure mitigates soft errors by duplicating latches implemented by the half C-element as shown in the bottom of Fig. 2. The input and output signals of these half C-elements have cross-coupled connections to be automatically recovered from a flip on a single node. On the other hand, redundant flip-flops such as TMR, BISER[4] and BCDMR[5] mitigates soft errors by majority voting among three storage cells, in which a flipped node is left until the next clock signal is injected to supply an unflipped new value. Compared with these majority-voter-based structures, the DICE structure is area-efficient since latches are not triplicated but duplicated.

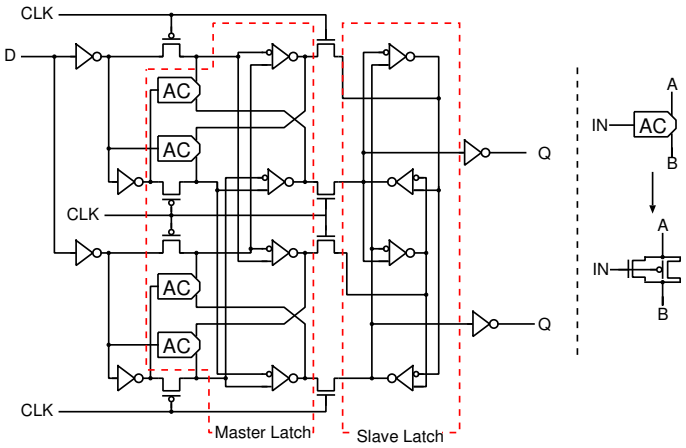

Fig. 1. Schematic diagram of DICE ACFF

ACFF connects master and slave latches by PMOS or NMOS pass transistors. Conventional FFs based on transmission gates (called TGFF hereafter) use two phases of clock signals CLK and $\overline{\text{CLK}}$. ACFFs, however, work by a single phase clock signal, which eliminates local clock buffers dissipating useless power when the activity of the input signal (the data activity, α) is low. In the conventional FFs, power dissipation of clock buffers are dominant if α is low. The AC elements as shown in the right side of Fig. 3 is required to overwrite the master latch by PMOS pass transistors. They weaken the connection between the cross coupled inverters when the input of either inverter becomes 1 and the next value to be overwritten is 0.

The proposed DICE ACFF are implemented by combining these two structures, DICE and ACFF. In the master and slave latches, inverters in the ACFF structure are replaced by half C-elements in the DICE structure. The half C-elements are duplicated and they are cross-coupled in the same manner as the original DICE. The DICE ACFF is implemented in a commercial 65 nm process using the double-height structure (DHC)[6] by sharing PMOS (NWELL) regions, which is much stronger to soft errors than sharing NMOS regions. It is partly because major carriers of NMOS are electrons whose mobility is much faster than holes. NMOS regions are much more sensitive than PMOS regions. Fig. 5 shows a cell layout of DICE ACFF. Its area is almost twice larger than

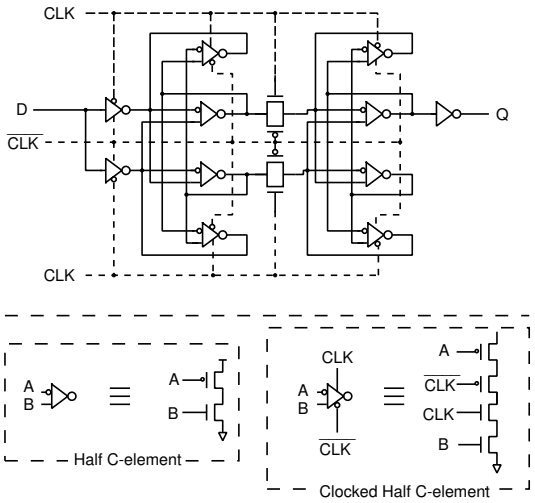

Fig. 2. Schematic diagram of DICE FF

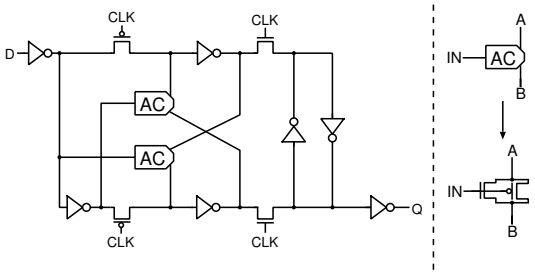

Fig. 3. Schematic diagram of ACFF[3]

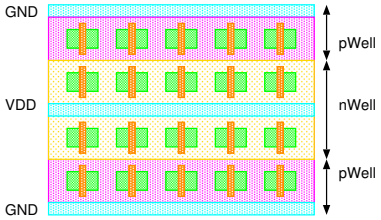

Fig. 4. DHC structure

the conventional DFF (TGFF) but only 1.05x bigger than the convectional DICE FF.

III. Estimation of Soft Error Rates

Stored values in FFs are flipped if generated charge by a particle hit exceeds a certain threshold value, which is called Q_{crit}. In redundant FFs such as DICE, two nodes must be flipped simultaneously. However, the possibility is too low when two continuous or simultaneous hits on two redundant node. We assume that a single particle hit flip multiple redundant nodes.

As already mentioned, the possibility is very low when two particles hit on the critical pair (CP) simultaneously. We assume that generated charge from a single particle is shared by the critical pair. As shown in Fig. 4, the implemented DICE ACFF shares a PMOS region. There is no critical pair among

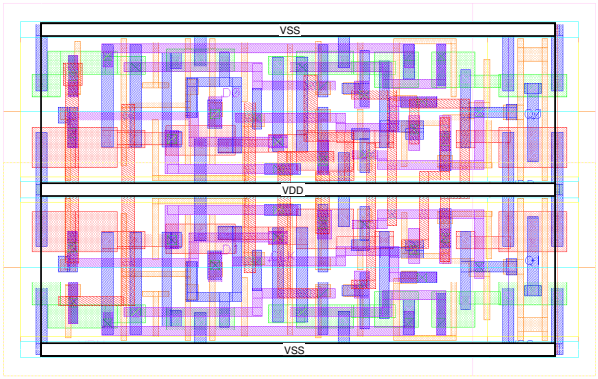

Fig. 5. Cell layout of DICE ACFF in a 65 nm process

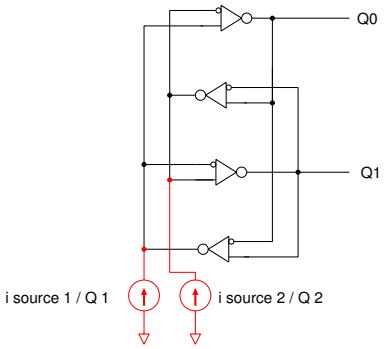

Fig. 6. Single exponential current source attached to 2 node of the latch.

NMOS transistors since they are separated by the PMOS region. We only evaluate Multiple Cell Upsets (MCUs) in the NMOS region. Eq. (1) is an empirical equation to compute soft error rates (SERs) by terrestrial neutrons[7], [8], [9]

$$N_{SER} = F \times K \times A \times \exp(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}) \quad (1)$$

in which, F is a neutron flux on the terrestrial region (0.00565/cm^{2}s), K is a constant value of 2.2×10^{-5}, and A is the total drain area connected to the node. Q_s is a value that can be determined by process parameters. From 65nm neutron irradiation results, Q_s in NMOS is 6.92 fC and that in PMOS is 3.40 fC.

In order to compute MCUs by a single particle hit, we use charge collection ratio according to the distance from the particle hit point. From the heavy ion results in [10], charge collection efficiency (E) is exponentially reduced by the distance x between the drain and the particle hit point computed by the following equations.

$$E_{\mathrm{n}}(x) = 0.285\exp(-1.12x) \quad : \text{for NMOS} \quad (2)$$
$$E_{\mathrm{p}}(x) = 0.538\exp(-2.07x) \quad : \text{for PMOS} \quad (3)$$

In non-redundant FFs such as TGFFs, a single-exponential current source is enough to evaluate Q_{crit}. In the tripli-

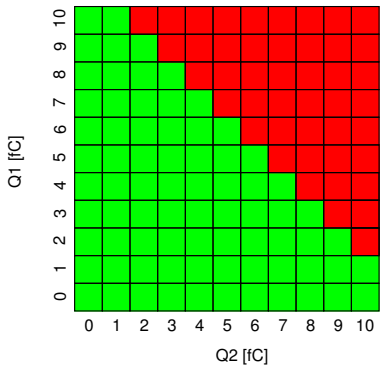

Fig. 7. Error Map for DICE Structure

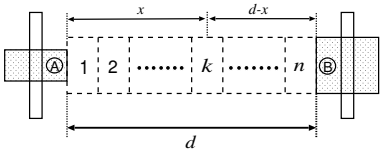

Fig. 8. Compute MCU rates of the critical pair transistors A and B

cated structure, two successive simulations with one single-exponential current source are enough to compute $Q_{\rm crit}$ since two storage elements such as latches or keepers does not influence with each other. In the DICE structure, however, two single-exponential current sources must be attached on the circuit-level simulations as shown in Fig. 6 since two redundant storage elements are cross-coupled. Two independent current sources Q1 and Q2 are attached to the pair of two nodes that can flip the stored value, which is called a critical pair. By changing the amount of charge on Q1 and Q2, we can obtain a Shmoo-like error map as show in Fig. 7.

Fig. 8 shows how to compute MCU rates from the critical charge of two transistors in a critical pair. From Eqs. (2) or (3), we can compute $Q'_{\rm critA}(x)$ and $Q'_{\rm critB}(d-x)$. The maximum value $Q_{\rm mcrit}(k)$ between these two $Q'_{\rm crit}$ values can be considered as the critical charge in the region k.

By assigning $Q_{\rm mcrit}(k)$ to $Q_{\rm crit}$ and the area of the region k to A in Eq. (1), we can obtain $N_{\rm SER}(k)$ in the region k. By summing these values from the all the region, we can obtain the total SER $N_{\rm TSER}$ of the critical pair as follows.

$$N_{\rm TSER} = \sum_{k=1}^{n} Q_{\rm mcrit}(k) \quad (4)$$

IV. Simulation Results

We compare the proposed DICE ACFF in terms of soft-error resilience, power, area, delay and ADPP (Area, Delay and Power Product) with TGFF, ACFF and BCDMR ACFF (Fig. 9)[11].

BCDMR ACFF is another redundant flip-flop based on BCDMR and ACFF. There is no local clock buffer because of its ACFF-based structure, which makes it lower-power at lower data activity. It is one of triplicated redundant FFs by voting two redundant latches and one keeper in the master or slave latch. If one of redundant latches is flipped, the keeper keeps the correct value since the C-element becomes high impedance. Even if the keeper is flipped, the C-element can overwrite the flipped value.

TABLE I
Area and power at 10% data activity of FFs normalized by conventional TGFFs

FF	Area	Power	average delay	rise delay	fall delay
TGFF	1.00	1.00	1.00	1.00	1.00
ACFF	0.76	0.456	0.49	0.43	0.55
DICE FF	2.00	2.28	1.29	1.43	1.18
DICE ACFF	2.10	0.716	0.86	0.73	0.97
BCDMR ACFF	2.40	0.911	1.15	1.21	1.11

TABLE II
Area × Delay × Power of FFs normalized by conventional TGFFs

FF	α=0	α=10	α=25	α=100
TGFF	1.00	1.00	1.00	1.00
ACFF	0.12	0.15	0.21	0.38
DICE FF	4.48	4.95	5.05	5.39
DICE ACFF	1.00	1.39	1.93	3.75
BCDMR ACFF	1.74	2.68	3.92	8.15

When evaluating power dissipation, we bundle 8 FFs with a clock buffer as shown in Fig. 10. It is because FFs based on the ACFF dissipates less power due to its clock-buffer-less structure. Fig. 11 shows power dissipation according to the data activity α normalized by the power of TGFFs. The power dissipation of DICE ACFFs is operated by lower-power than TGFFs when α is below 20%. In general ASICs, the activity ratio α is from 5% to 15%[3]. The proposed DICE ACFF always operates at lower power under the condition. The power dissipations at α=10% is 77% of TGFF.

Table I lists area, power at α=10% and delay. Note that the definition of the delay is CLK to Q estimated from circuit-level simulations with extracted stray RC elements. In the slave latches of ACFF, DICE ACFF and BCDMR ACFF, there is one inverter for output from clock-controlled pass transistors between master and slave latches, while there are two series inverters in the slave latches of TGFF and DICE FF. Thus the CLK-to-Q delay becomes longer in TGFF and DICE FF. In BCDMR ACFF, the C-element and the keeper make the delay longer. As the results delays D becomes longer as thw following order.

$$\begin{aligned} D_{\rm ACFF} &< D_{\rm DICE\ ACFF} < D_{\rm TGFF} \\ &< D_{\rm BCDMR\ ACFF} < D_{\rm DICE\ FF} \end{aligned}$$

Table II shows the ADP products (ADPP). At $\alpha = 0\%$, the ADPPs of DICE ACFF and TGFF are equivalent. As α increases, the ADPP of DICE ACFF increases compared with that of TGFF. But the ADPP at α=10% is still only 39% bigger than that of TGFF. The proposed DICE ACFF is efficient in terms of area, power and delay.

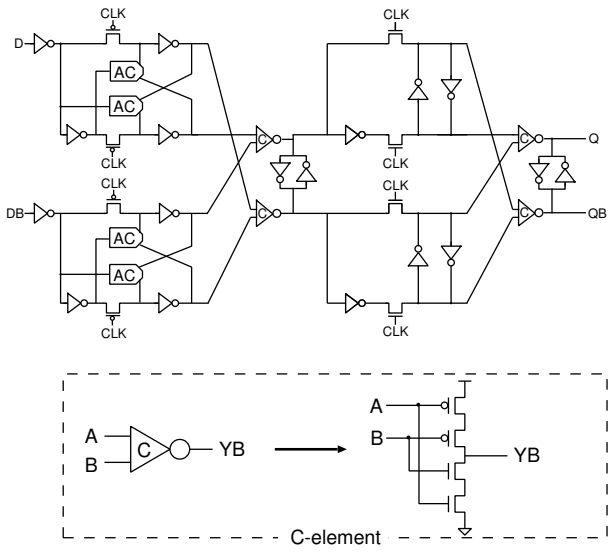

Fig. 9. Schematic diagram of BCDMR ACFF and C-element

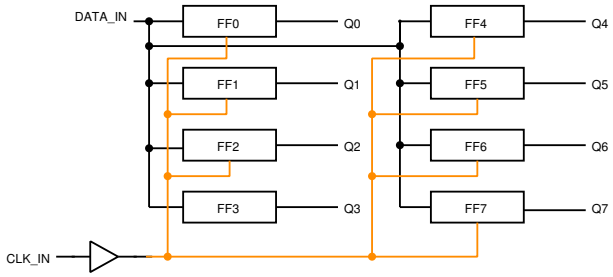

Fig. 10. Simulated circuit structure to compute power dissipation

Table III lists SERs in FIT (Failure in Time)/Mbit. It shows the lowest SERs obtained from all possible stored values and clock states. We assume that there is no soft error in NMOS regions in DICE FF, DICE ACFF and BCDMR ACFF since they are implemented in the DHC structure whose NMOS regions are separated by the shared PMOS region. As shown in the table, TGFF and ACFF have several hundreds

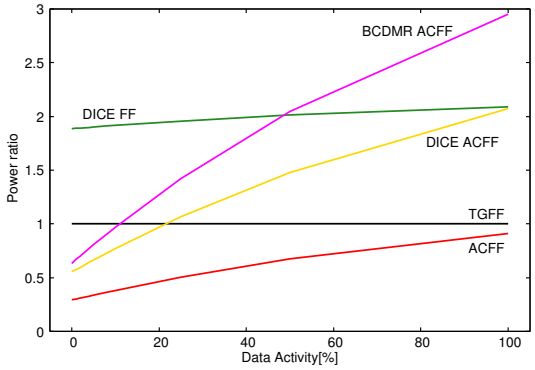

Fig. 11. Simulated power normalized by the power of TGFF

TABLE III
SERs OF FFs

FF	SER [FIT/Mbit]	SER/TGFF	1/ (SER/TGFF)
TGFF	379	1.00	1.00
ACFF	285	0.75	1.32
DICE FF	1.22	0.0032	311
DICE ACFF	0.82	0.0022	462
BCDMR ACFF	0.16	0.00042	2369

TABLE IV
SERs OF DICE FF ACCORDING TO STATES OF INPUT PINS AND CRITICAL PAIRS (CP).

D	CLK	CP		Q_{crit1}	Q_{crit2}	dist. [μm]	SER
1	1	1	2	3.0	5.8	0.80	1.22
1	0	3	4	7.0	8.5	0.82	5.60e-3
0	0	5	6	3.0	6.2	0.68	0.72
0	1	7	8	8.0	9.0	0.82	9.5e-3

TABLE V
SERs OF DICE ACFF ACCORDING TO STATES OF INPUT PINS AND CRITICAL PAIRS (CP).

D	CLK	CP		Q_{crit1}	Q_{crit2}	dist. [μm]	Total SER
1	1	1	3	4.0	5.0	0.84	0.82
		1	8	5.0	19.0	0.84	
		3	6	9.8	20.0	0.84	
		6	8	23	21	0.44	
1	0	2	4	9.9	9.5	0.94	1.90e-4
		2	7	9.5	20.0	2.6	
		4	5	10.0	19.0	2.6	
		5	7	24	21	0.5	
0	0	9	11	5.0	6.3	0.96	5.04e-2
0	1	10	12	5.0	9.8	1.06	1.25e-3

FIT/Mbit due to their non-redundant structures. The proposed DICE ACFF has the 1.5x lower SER than DICE FF which relationship is equivalent to that between ACFF and TGFF. Table IV and V show critical pairs according to the states of D and CLK in DICE FF and DICE ACFF with the simulated critical charges and computed SER values. The node numbers are marked in Figs. 12 and 13. In DICE FF, there is only a single critical pair in one state of D and CLK, while DICE ACFF has multiple critical pairs. The SER values in Table III become the highest SER values among these states. As in Table IV and V, the SERs are highest when D=1 and CLK=1. It is because the critical nodes connected to the output of gates with lower driverbility such as clocked gates or AC elements have lower critical charge. DICE ACFF has lower SER than DICE FF mainly because the lower critical charge and the longer distance between the nodes in the critical pair.

BCDMR ACFF has approximately 5x lower SER than DICE ACFF. It is mainly because of its area penalty. As the distances between critical pairs become shorter, the values of $Q_{\rm crit}$ also becomes smaller according to Eqs. (2) and (3). The main purpose of the DICE ACFF is to achieve lower power and lower area penalty. As in Table I, BCDMR ACFF is 14.3% bigger than DICE ACFF. The ADPP of DICE ACFF is always lower than that of BCDMR ACFF at any data activities α. It means that DICE ACFF achieves lower power, shorter delays and smaller area at the expense of higher SER than BCDMR ACFF.

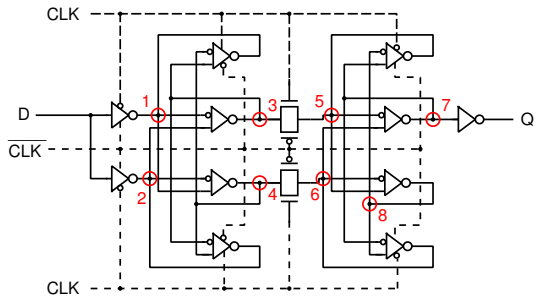

Fig. 12. Node numbers to compute SERs among critical pairs in DICE FF

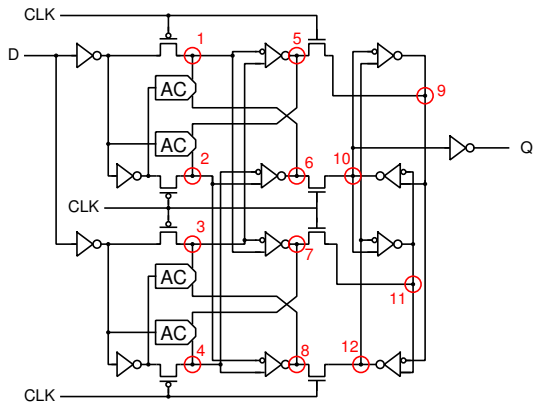

Fig. 13. Node numbers to compute SERs among critical pairs in DICE ACFF

V. Conclusion

We propose low-power area-efficient redundant flip-flops, called DICE ACFF. Its structure is based on reliable DICE and the low-power ACFF. It achieve low-power at lower data-activity. If data activity is lower than 20%, its power is lower than conventional DFF based on transmission gates (TGFF). Conventional ASICs have 5% to 15% data activity. DICE ACFFs always achieve lower power than TGFF in these regions. Its area overhead is 2.1x of the TGFF and 1.05x of the conventional DICE FF. It has 1.5x and 462x less soft error rate than DICE FF and TGFF, respectively. DICE ACFFs is superior to DICE FF in power, area and soft error resilience.

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