Impact of Cell Distance and Well-contact Density on Neutron-induced Multiple Cell Upsets

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***Abstract*— We measured neutron-induced Single Event Upsets (SEUs) and Multiple Cell Upsets (MCUs) on Flip-Flops (FFs) in a 65 nm bulk CMOS process. Measurement results show that MCU / SEU is up to 23.4% and is exponentially decreased by the distance between latches on FFs. MCU rates can drastically be reduced by inserting well-contact arrays between FFs. The number of MCUs is reduced from 110 to 1 by inserting a well-contact array under power and ground rails.**

I. Introduction

As process scaling, radiation-induced single event effect is one of the most significant issues for LSI reliability. Several radiation-hardened designs are proposed – for example, triple modular redundancy (TMR), built-in soft error resilience (BISER) [1], dual interlocked storage cell (DICE) [2], and error correction code (ECC). Radiation-induced multiple error is increased by process scaling [3], [4]. MCU reduces soft error immunity on SRAMs since it cannot be corrected by a simple ECC circuit.

In 90 – 65-nm process, Radiation-induced multiple errors are also reported in logic circuits. MCUs are observed in FFs [5]. It increases soft-error rates on radiation-hardened latches and FFs [6], [7]. Single Event Multiple Transients (SEMTs) in inverter chains are reported by neutron and heavy-ion experiments [8], [9]. MCU is caused by charge sharing and parasitic bipolar effects [10]. MCU rate depends on cell distance and well-contact density. In order to reduce radiation-induced multiple error, each vulnerable transistor is placed on different p-well regions or separated over 1.1μm [11], [12]. The parasitic bipolar effect and the charge sharing also affect SEU occurrence [13] and Single Event Transient (SET) pulse widths [14]. To estimate soft-error rates and increase its resilience, it is necessary to measure characteristics of radiation-induced multiple errors.

In this paper, we show measurement results of neutron-induced MCUs on D-FFs by using 4 different shift registers to estimate soft error rate on redundant-FFs. Test chips are fabricated in a 65-nm bulk CMOS process and accelerated tests are carried out at Research Center for Nuclear Physics (RCNP). We also show the dependence of MCUs on the distance of FFs and well-contact density.

This paper is organized as follows. Section II explains the test circuit structure in detail. Section III shows our neutron-beam experimental setups in RCNP, followed by Section IV which discusses experimental results. Section V concludes this paper.

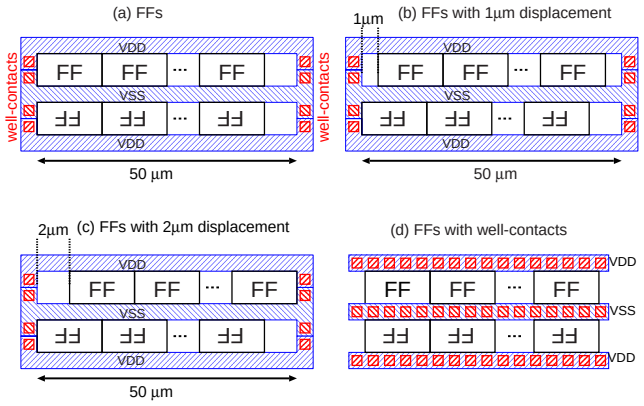

Fig. 1. Conceptual Layout structures of four different shift registers. Clock buffer chains are omitted in this figure.

II. Test Chip Structure

We fabricated a test chip in 65-nm bulk CMOS process to measure soft error by spallation neutron beam. The purposes of the test chip are as follows.

- To estimate neutron-induced soft error rate on redundant FFs and compare it with SEU rate on non-redundant FFs.
- To evaluate cell-distance dependence of MCU rate for effective layout design of redundant FFs.
- To evaluate dependence of MCU rate on well-contact density (well-contact distance). If MCU rate strongly depends on it, MCU is mainly caused by the parasitic bipolar effect. It is because the parasitic bipolar turns on by raising well-potential.

To estimate soft error rate on redundant-FFs, we implement four different shift registers as shown in Fig. 1. Note that they are implemented with conventional non-redundant FFs since we assume that MCU rate on FFs is equivalent to soft error rate on redundant FFs with similar layout structures. All shift registers are constructed by FFs and clock buffer chain [15]. Implemented FFs have the same layout structure except well-contact. Fig. 2 shows the schematic diagram. The master and slave latches are constructed by inverters and tri-state inverters.

Shift registers (a) – (c) in Fig. 1 have 0 μm, 1 μm, and 2 μm horizontal offsets between odd rows and even rows in order to measure MCU rates by changing the distance between latches on FFs. When the clock signal is "1" and

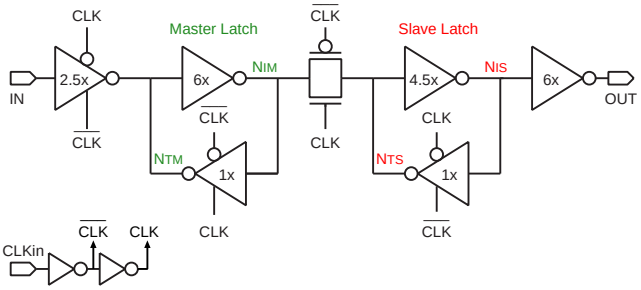

Fig. 2. Schematic diagram of implemented FFs. The values of this figure show normalizing drive strengths.

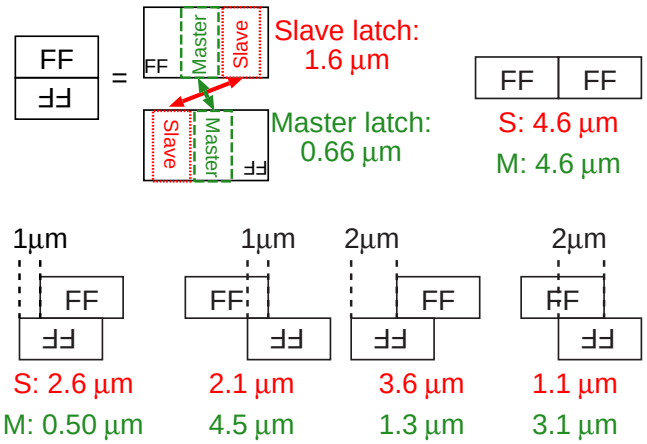

Fig. 3. Distance between master or salve latches on shift register (a) – (c) in Fig. 1.

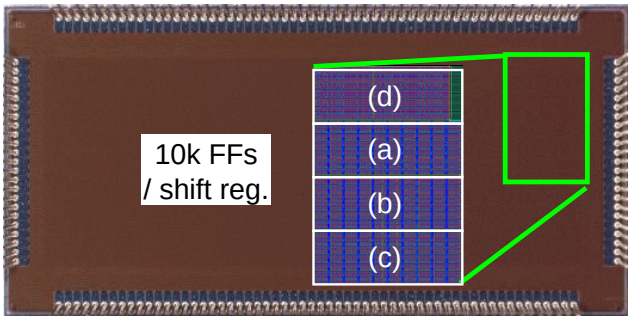

Fig. 4. Chip micrograph with floorplan.

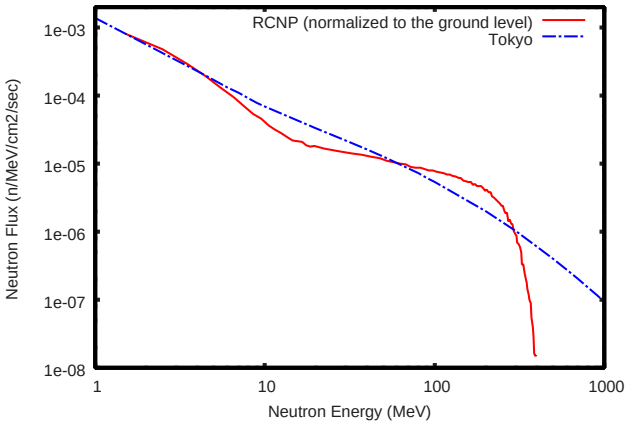

Fig. 5. Neutron spectrum at RCNP.

master latches are in the hold state, we obtain 6 kinds of MCUs simultaneously from observed MCU patterns as shown in Fig 3. In addition, shift registers have different distance between slave latches and between master latches as shown in upper left of Fig. 3. We obtain 12 kinds of MCUs with 0.5 – 4.6 μm by changing clock signal and we can measure distance-dependence of MCUs by using 3 simple shift registers.

Shift registers (a) – (c) have isolated well-contacts which are inserted every 50 μm. In contrast, the shift register of Fig. 1 (d) has well-contact arrays under its power and ground rails, which has 60x higher well-contact density than the other shift registers (a) – (c). Therefore, we obtain dependence of MCU rate on well-contact density by comparing MCU rates between the shift registers (a) and (d) which have same cell-distance.

III. Experimental Setup

Fig. 4 shows a test chip micrograph fabricated in a 65-nm bulk CMOS process. It has twin-well structure and its supply voltage is 1.2 V. Each shift register includes 10k FFs. The total area of four shift registers is 0.5 $\times$ 0.8 mm^2 on a 2 $\times$ 4 mm^2 die.

Accelerated tests were carried out by spallation neutron irradiation at RCNP [16]. Fig. 5 shows the neutron beam spectrum compared with the terrestrial neutron spectrum at the ground level of Tokyo. The average acceleration factor is 3.8×10^8. In order to increase error counts, we measured 28 chips at the same time using stacked DUT boards. An engineering LSI tester is used to control DUTs and collect shifted error data.

During irradiation, all stored values of the shift registers were initialized to "ALL0" or "ALL1". Clock signal is fixed to "1" or "0" to keep master latches or slave latches on FFs in the hold state. All stored values are retrieved every 5 minutes. Expected value of SEU on FFs is less than 3 [SEU / chip / 5 min]. Each chip has 40k FFs and adjacent FFs are rarely flipped by 2 different SEUs. Therefore, when adjacent FFs are flipped, we expect that these flips are caused by MCUs.

TABLE I
THE NUMBER OF SEUS AND MCUS BY NEUTRON IRRADIATION WHEN STORED VALUE IS "ALL0" AND CLOCK SIGNAL IS "1" (MASTER LATCHES ARE IN HOLD STATE).

Shift Register	Min. cell distance	# of SEU	# of MCU	MCU/SEU [%]
(a) FFs	0.66 μm	617	110	17.8
(b) FFs w/ 1 μm	0.5 μm	631	148	23.4
(c) FFs w/ 2 μm	1.3 μm	654	91	13.9
(d) FFs w/ well-contacts	0.66 μm	498	1	0.2

TABLE II

THE NUMBER OF SEU AND MCU RATES BY NEUTRON IRRADIATION WHEN STORED VALUE IS "ALL0" AND CLOCK SIGNAL IS "0" (SLAVE LATCHES ARE IN HOLD STATE).

Stored values	Shift Register	SEU rate [n/Mbit/h]	MCU rate [n/Mbit/h]
ALL0 (N_{TS} = 0)	(a)	60	0
	(b)	78	0
	(c)	79	0
	(d)	91	0
ALL1 (N_{TS} = 1)	(a)	254	15
	(b)	283	10
	(c)	259	33
	(d)	165	0

IV. Experimental Results

Table I shows the number of SEUs and MCUs of the shift registers as shown in Fig. 1 when stored value is "ALL0" and clock signal is "1" (Master latches are in the hold state). Note that the number of SEUs includes that of MCUs. The MCU / SEU is up to 23.4% which is close to that on 65-nm SRAM cells [17]. These results clearly show that soft-error resilience of redundant FFs flipped by MCUs is only 4 times higher than non-redundant FFs. In contrast, the shift register (d) has a very low MCU rate and only one MCU is observed on it. The number of MCUs is reduced from 110 to 1 by inserting well-contact arrays under supply and ground rails of FFs. Therefore, we can improve soft-error resilience of the redundant FFs without delay overhead by inserting well-contacts between their latches. It also shows that in the fabricated technology, almost all MCUs are caused by the parasitic bipolar effect since it is caused by well-potential perturbation [10]. In the shift register (a) – (c), we observe more than 3-bit MCUs as shown in Fig. 6. We assume that 5 to 8-bit MCUs are caused by successive hits by one ion [5] since they spread in line.

Table II shows SEU and MCU rates on shift register (a) and (d) when clock signal is "0" (Slave latches are in the hold state). All shift registers have higher SEU rates when stored values are "ALL1" and output node of tri-state inverter in the slave latch (N_{TS}) in Fig. 2 is "1". The tri-state inverters have smaller critical charge than the inverters since the tri-state inverters have weaker drive strength. Therefore, this result suggests that nMOS transistors are weak to SEUs since N_{TS} is flipped to "0" when a particle hits on nMOS transistor. In the fabricated structure, no MCU is observed at N_{TS} = 0 as shown in Table II and 96% of MCUs are caused on FFs whose p-bulk are shared, which is consistent with the results of ref. [11]. This result shows that almost all MCUs are induced when a particle hits on nMOS transistors constructing the tri-state inverter.

Compared with SEU rates on shift registers, shift register (d) has highest SEU rate at N_{TS} = 0, but it has the lowest at N_{TS} = 1. We assume that it is caused by the parasitic bipolar effect [13].

1) A neutron hits on inverter in FF at N_{TS} = 0.
2) N_{IS} turns to "0" by generated electrons and p-well potential elevates by generated holes.
3) When there are a lot of generated holes, N_{TS} does not turn to "1" since the parasitic bipolar transistors of nMOS transistors turn on by p-well potential perturbation.
4) After p-well potential returns to 0 V, N_{TS} and N_{IS} rise to "1" simultaneously.
5) As a result, N_{IS} return to "1" and N_{TS} keeps "0" since the inverter has about 4 times bigger drive strength as shown in Fig. 2 and its output, N_{IS} rises to "1" more quickly than N_{TS}.

Therefore, the parasitic bipolar effect prevents FFs in (a) – (c) from being flipped at N_{TS} = 0.

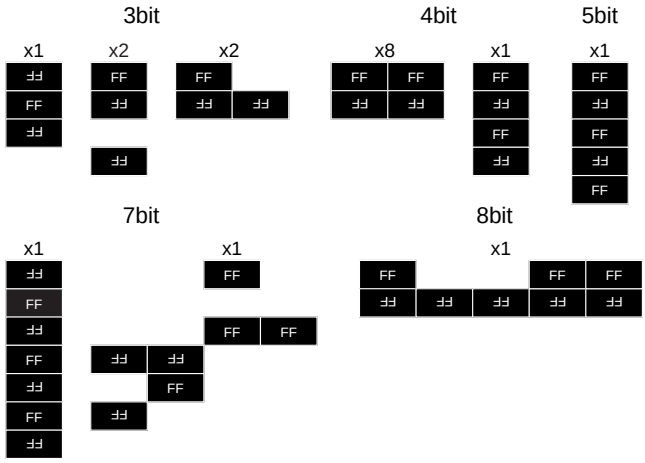

Fig. 6. MCU patterns with more than 3 bits flipped.

Fig. 7 shows the distance-dependence of MCU / SEU on FFs which is obtained from the shift registers (a) – (c). The MCU / SEU (y-axis) is calculated from measurement results at N_{TM} = 1 or at N_{TS} = 1. The MCU / SEU is exponentially decreased according to $d^{1.67}$ (d is the distance between two latches) and fitting line shows that it can be 100% when $d \leq 0.3$ μm. As shown in Fig. 2, master and slave latches in the FF have different structure. However, measurement results of MCU / SEU are distributed on the same straight line. Therefore, the MCU / SEU does not depend on the drive strength and load capacitance. To achieve 100x higher soft-error resilience in redundant FFs than in non-redundant FF, we must implement redundant FFs whose latches are separated by 4 μm from each other. It consumes huge area or complicated design procedures and these drawbacks can not be reduced by the process scaling.

In the fabricated technology, we suggest the placement of redundant FFs as follows and in Fig. 8 for effective soft-error resilience.

1) Inserting well-contacts between their FFs (Fig. 8 (a)).
2) Implementing each FF on different p-well region (Fig. 8 (b)).
3) Implementing p-well-sharing FFs in a horizontal line for separating their FFs by 4 μm from each other (Fig. 8 (c) and (d)).

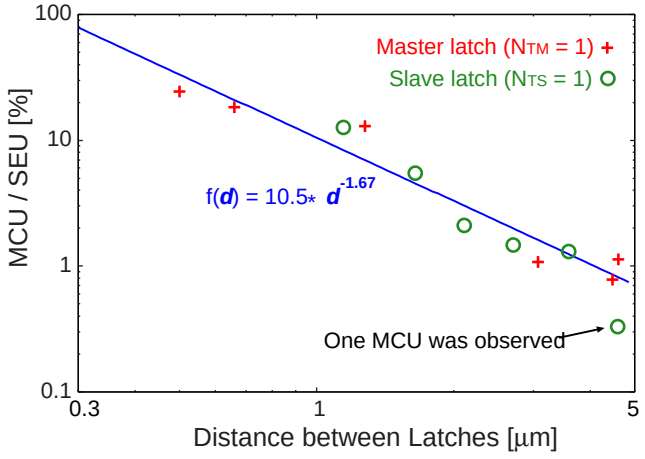

Fig. 7. Distance-dependence of MCUs.

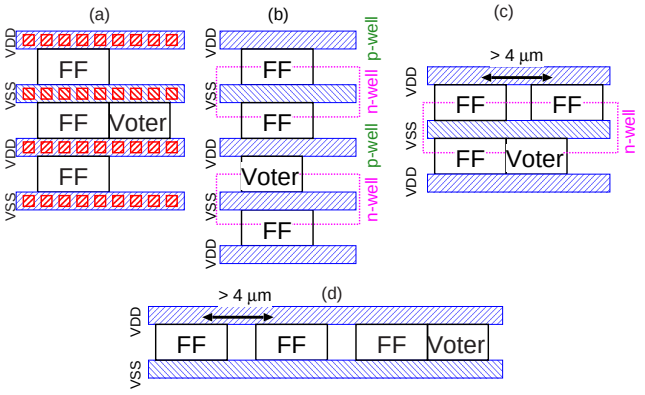

Fig. 8. Placement of triple modular redundant FFs for effective soft-error resilience.

V. Conclusion

We measured neutron-induced MCUs on FFs in a 65 nm CMOS process in order to evaluate their dependences on the distance of FFs and well-contact density. Accelerated test results show that the MCU / SEU is up to 23.4% and is exponentially decreased by the distance of latches. Measurement results also show that MCU rates can drastically be reduced by inserting well-contact arrays between FFs. The number of MCUs is reduced from 110 to 1 by inserting a well-contact array under supply and ground rails of 10k-bit FFs. We can improve soft-error resilience without delay overhead by inserting well contacts between latches on rad-hard FFs.

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