

Measurement Results of Multiple Cell Upsets on a 65nm Tapless Flip-Flop Array

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Abstract—We measured single event upsets (SEUs) and multiple cell upsets (MCUs) of a flip-flop array in a 65nm bulk CMOS process using accelerated white neutron beams. The flip-flop array embeds 84,000 FFs constructing a 84,000bit shift register. Its cell structure is so-called tapless, in which no standard cell contains any well tap. Measurement results from 26 DUTs including 2.2Mbit FFs show that both SEUs and MCUs are observed on the tapless structure. MCUs are only observed when master or slave latch stores a specific value. The ratio between SEU rates of master and slave latches from measurements are well consistent with that from circuit-level simulations. SEU rates are almost constant despite the distance from tap, while MCU rates highly depend on it. The FFs farthest from the well tap are 1.6x and 3.7x more vulnerable than the nearest FFs when master and slave latches are in the latch state respectively. We also propose a layout structure to protect an MCU of three FFs in the TMR structure.

I. INTRODUCTION

Process scaling makes LSIs less reliable to temporal and permanent failures. Temporal failures flip a stored value on SRAMs or flip-flops (FFs). High-energy neutron is one of main sources of temporal failures, which is called a “soft error.” To mitigate soft errors, redundant circuits are usually used. TMR (Triple modular redundancy)[1] is an ultimate solution for soft errors, in which all circuit elements are tripled and unmatched results are resolved by majority voting. It is very robust to soft errors since it does not fail until two modules fail at the same time, but its area penalty is relatively huge.

Aggressive process scaling causes a multiple cell upset (MCU) in addition to a single event upset (SEU). MCUs become a critical issue on SRAMs, since it cannot be recovered by ECC circuits[2]. On the TMR structure, MCUs must be a critical issue. The TMR circuit cannot work correctly if two FFs of three redundant FFs are flipped simultaneously by an MCU. MCUs are induced by parasitic lateral bipolar transistors, base terminals of which are well taps sparsely placed in SRAMs to maximize layout density. To protect processors from SEUs, the parity check mechanism is commonly adopted for registers or latches[3]. Ordinal parity check assumes that only a single bit will be flipped by a soft error. If multiple bits are flipped in a register, it cannot be detected.

Recently, so-called tapless standard cells [4] are widely used to control n-well and p-well potentials to reduce standby power. Tapless standard cells have no tap to tie n-well or p-well to Vdd or ground. Instead, a tap cell is used to tie both wells to Vdd or ground. Conventional standard cells contain built-in well taps strongly tied to Vdd or ground. On

the other hand, in the tapless standard cell design, taps are sparsely placed similar to SRAMs. It causes MCUs due to lateral bipolar effects.

In this paper, we show measurement results of SEUs and MCUs of 65nm FFs using tapless standard cells. Measurements were carried out by accelerated white neutron beams at RCNP (Research Center for Nuclear Physics, Osaka University). The rest of this paper is organized as follows. Section II describes the tapless shift registers in detail. Section III shows our neutron-beam experiments in RCNP, followed by Section IV which discusses experimental results in detail. We propose a robust layout structure for the TMR structure to avoid MCUs in Section V. Section VI concludes this paper.

II. TAPLESS FLIP-FLOP ARRAY

To investigate SEUs and MCUs on flip-flops, we implemented an array of flip-flops constructing a 84,000bit shift register composed of tapless standard cells in a 65nm bulk CMOS process. Fig. 1 shows standard cell structures with/without tap. The tapless structure in the right side has a capability controlling body biases to reduce leakage power. In addition to that tapless structure make transistors wider ($W1 > W0$) than the tapped one since blank space for tap cells can be filled with transistors.

Fig. 2 shows the detailed layout and schematic structure of the shift register. FFs are laid out in a 350×240 array to form the implemented 84,000bit shift registers based on the tapless structure. We use no global clock to simplify layout structure. Clock is injected from the tail of the shift register, while the serial shift-in signal is injected from the head of the shift register. Clock signals for all FFs are serially connected from the tail to the head, which relieves very tight hold constraint of shift registers. The drawback of such layout structure is slower clock frequency. We cannot apply higher clock frequency to such shift registers. However shift operations are required only when reading or writing registers. Slower clock does not affect anything on the SER measurement. Actually, we can apply 2.5MHz clock frequency for the shift operation. It takes 33.6ms. to complete a 84,000bit shift operation.

Tap cells connecting both wells to Vdd or ground are inserted every 6 FFs ($=28\mu\text{m}$) as shown in Fig. 2. All well taps are directly connected to Vdd or ground in this design. We have three sorts of FFs with different distance from tap cells. We categorize these three as F0, F1 and F2 respectively as in the bottom of Fig. 2. Each FF contains master and slave latches

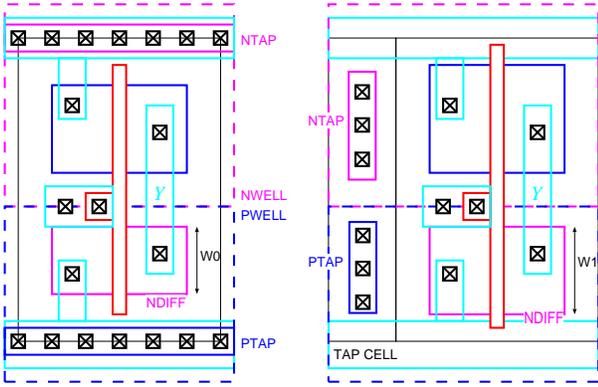


Fig. 1. Conventional standard cell (Left) and tapless standard cell (Right)

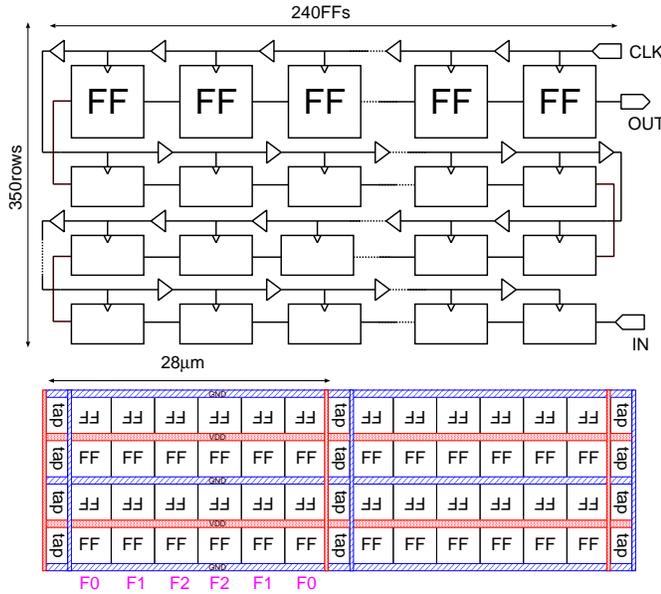


Fig. 2. Schematic and layout structure of the tapless shift register.

as in Fig. 3. These latches have “latch” and “transparent” states by the clock states. When the master latch in the latch state, the slave latch in the transparent state. Neutron-induced soft errors influence latches in the latch state. It may flip the state of a latch, which results in a single event upset. On the other hand, a latch in the transparent state just generates an error pulse so called single event transient (SET) pulse, which disappears and have no influence on the state of the FF. Fig. 4 shows the detailed layout structure of three adjacent FFs. Note that we adopt a twin-well structure, in which NMOSs are placed on p-bulk, while PMOSs are placed on n-well. Master latches are placed perpendicularly, while slave latches are placed diagonally. We predict these measurement results from these layout structure.

- More MCUs are observed between two adjacent cells the p-bulk of which is shared (row $i + 1$ and $i + 2$ in Fig. 4) than those the n-well of which is shared. It is because

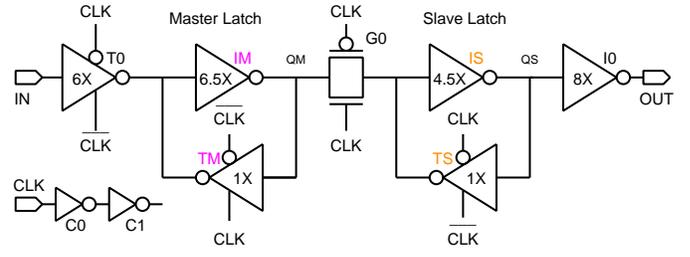


Fig. 3. Schematic diagram of a FF.

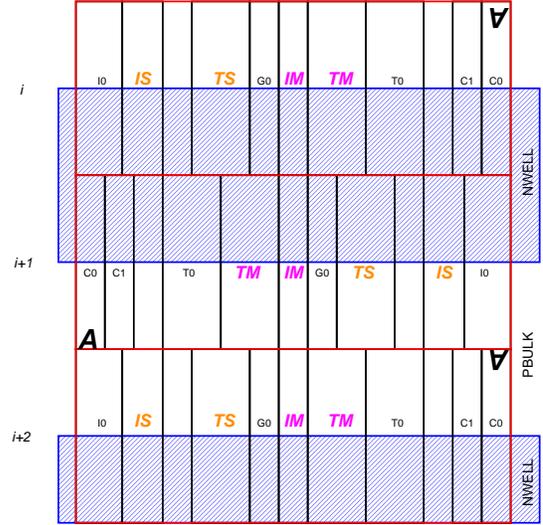


Fig. 4. Detailed layout structure of three adjacent FFs.

the n-well structure decreases induced current compared with the p-bulk[5].

- Master latches are more vulnerable to MCUs than slave latches since the distance between master latches constructed from IM and TM are shorter than that between slave latches constructed from TS and IS.
- FFs close to the tap cells (F0 in Fig. 2) is strongest against MCUs since tap cells stabilize the n-well or p-bulk potential.

Fig. 5 shows a chip micrograph with a partial layout structure. The 84,000bit shift register is implemented in a $0.63 \times 1.1 \text{mm}^2$ region on a $2 \times 4 \text{mm}^2$ die.

III. EXPERIMENTS

Experiments by accelerated white neutron beams were carried out at RCNP. Figure 6 shows the neutron beam spectrum compared with the terrestrial neutron spectrum at the ground level of Tokyo. The average accelerated factor is 3.7×10^8 in this measurement. Figure 7 shows 7-stage stacked DUT boards to increase error counts. Each DUT board has four segments, each of which is equipped with a single DUT. Up to 28x increase of soft errors is expected. Note that input signals are common for every segment, while output signals are independent for 7 DUTs to minimize time for the shift

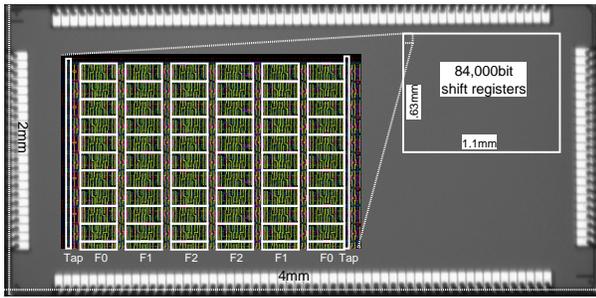


Fig. 5. Chip micrograph and partial layout structure.

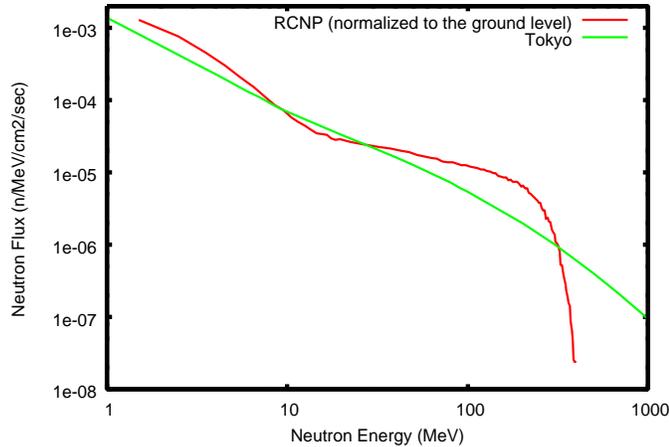


Fig. 6. Neutron spectrum at RCNP.

operation. Since 26 DUTs out of 28 are fully functional, 2.2Mbit FFs ($=84,000 \times 26$) are measured simultaneously. Figure 8 depicts the neutron-beam opening and the stacked DUT boards. An engineering LSI tester is used to control DUTs and collect shifted error data. Supply voltage levels for core and IO transistors are 1.2V and 3.3V, both of which are nominal for the 65nm bulk process.

Prior to the neutron-beam irradiation, all FFs in the shift register are initialized to the stripe pattern as in Fig. 9. FFs in the shaded region composed of 20bits store 1, while FFs in the white region composed of 20bits store 0. The stripe pattern is required to remove unexpected shifts caused by SETs on the clock chain. If an SET pulse is generated at a specific point on the clock chain, FFs located after the generated point may be shifted. The stripe pattern is used to weed out unexpected flips as in Fig. 9.

During irradiation, the clock signal is fixed to 0 or 1 to keep master or slave latches in the latch state. Stored values of the shift registers are retrieved every 5 minutes. After finishing retrieving (shifting), all FFs are restored to the initial state of the stripe pattern.

IV. RESULTS AND DISCUSSIONS

Table I shows number of SEUs and MCUs from measurement results to iterate a 5 min. measurement 20 times for each clock state. Note that number of SEUs includes MCUs.

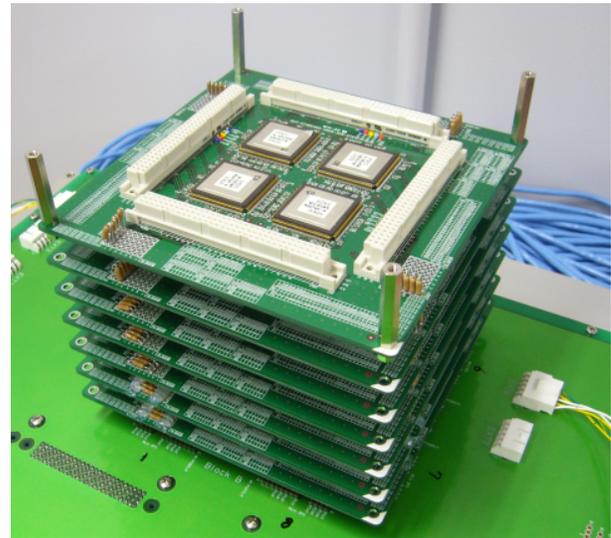


Fig. 7. 7-stage stacked DUT boards. Each DUT board includes four DUTs.

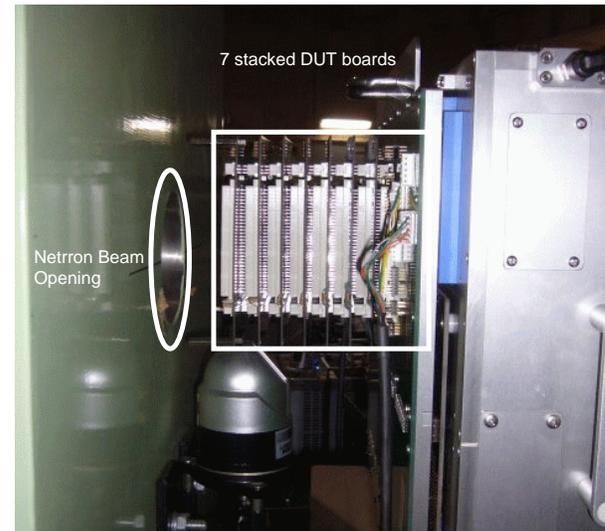


Fig. 8. Neutron-beam opening and 7-stage stacked DUT boards.

We have 520 ($=26\text{chips} \times 20\text{times}$) measurement results for $\text{CLK}=0$ and 1 respectively. We observe several unexpected shifts caused by SET pulses along the clock chain. However, error bits generated from SETs on the clock are successfully removed utilizing the stripe pattern as in Fig. 9.

Table II summarizes SEU and MCU rates on the master and slave latches. Those latches are more vulnerable when the tristate inverters (TM and TS) are vulnerable. It is because the feedback inverters such as IM and IS are stronger than the tristate inverters, TM and TS. Stronger inverters can quickly feed back flipped output values, while weaker tristate inverters slowly feed back them. If feedback is slow, the output node of an injected inverter goes back to its original state before the feedback signal arrives. Thus the number SEUs are bigger when the tristate inverters are vulnerable.

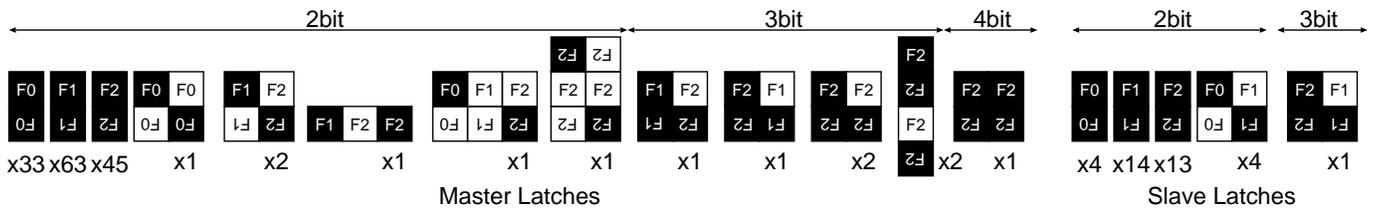


Fig. 10. All MCU patterns on the master latches (left) and the slave latches (right). Filled black rectangles show flipped FFs. F0, F1, F2 correspond to the FF location from the tap cell (See Fig. 4)

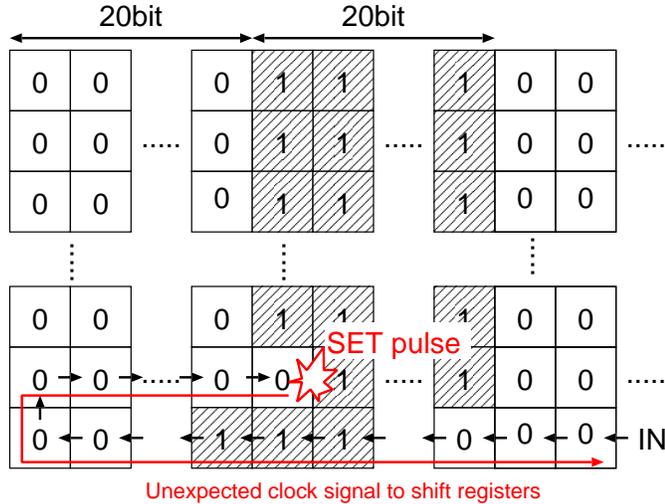


Fig. 9. Initialized pattern for the FF array

TABLE I
TOTAL NUMBERS OF SEUs AND MCUs ON THE MASTER AND SLAVE LATCHES BY THE NETRON IRRADIATION OF 100 MINUTES.

	Master	Slave
SEU	1205	1052
MCU	154	36

Fig. 10 shows all patterns of observed MCUs on the 2.2Mbit FF array. Almost all MCUs are flips of 2bit FFs between vertically-contacted cells whose p-bulks are shared such as F0/F0, F1/F1, F2/F2. These measurement results suggest that no SEU might happen on the n-well. Thus, inverters or tristate inverters whose output is 1 are only vulnerable to soft errors when NMOSs on p-bulk are vulnerable. We observed a few 2bit MCUs among diagonally-contacted FFs or alternately-adjacent FFs that cannot be explained by the lateral bipolar effect. One possible reason is that these multiple flips are results of two independent SEUs. The expected value of the multiple flip up to the 2bit distance is less than 0.2bit/84,000bit.

Closer latches might be more vulnerable to MCUs. In that sense, master latches when IM is vulnerable might be most vulnerable to MCUs since all IMs are laid out perpendicularly as in Fig. 4. However, we observe no MCUs when QM=1 at which IM is vulnerable.

Table III shows SER rates in FIT/Mbit on the terrestrial

TABLE II
MEASUREMENT RESULTS 1 : SEUs AND MCUs ACCORDING TO STORED VALUES IN MASTER OR SLAVE LATCHES BY NEUTRON BEAM IRRADIATION.

Vulnerable Latch	State	Vulnerable Gates	# of SEU (n/Mb/h)	# of MCU (n/Mb/h)
Master (CLK=1)	QM=0	TM	541	88
	QM=1	IM, TS	222	0
Slave (CLK=0)	QS=0	TS	493	19
	QS=1	IS	112	0

TABLE III
COMPARISON OF SEU RATES ON THE TERRESTRIAL ENVIRONMENT BETWEEN MEASUREMENTS AND CIRCUIT-LEVEL SIMULATIONS.

	State	SER (FIT/Mbit)		
		Measurement	Simulation	M/S
Master	QM=0	2900	1527	3.8
	QM=1	1200	844	2.9
	QM=0/QM=1	2.4	1.8	-
Slave	QS=0	2700	1527	3.6
	QS=1	610	381	3.2
	QS=0/QS=1	4.4	4.0	-

environment from measurement results and circuit-level simulations. FIT rates of the FFs from the experimental results are several thousand FIT/Mbit which are almost same as that of ordinal SRAMs, 1000FIT/Mbit. The highest SEU rate is 2900FIT/Mbit of the master latch which stores 0 (QM=0), in which the ratio between MCU and SEU is 0.16. When an SEU occurs on the master latch in that state, MCUs happen once in every 6 SEUs. On the circuit-level simulations, we first obtain the critical charge Q_{crit} for all vulnerable nodes to attach a single-exponential current source on it. Then the SER are computed from the empirical model in [6] as follows.

$$SER = F \times K \times \sum_n^{\text{all vul. nodes}} A_n \times \exp\left(\frac{Q_{crit,n}}{Q_s}\right) \quad (1)$$

F : Neutron Flux, A_n : Drain Area

Q_s : Charge Collection Efficiency

The absolute FIT rates of experimental results and simulations are different mainly because the parameter K is obtained from [6]. However, the ratio between the FIT rates of slave and master latches appeared as M/S from measurements and simulations in Table III are almost equivalent. In addition to that, ratios of SER rates when QM(QS)=0 and QM(QS)=1 are also equivalent. It reveals that the empirical model in Eq. (1)

TABLE IV
MEASUREMENT RESULTS 2: NUMBER OF SEUS AND MCUS PER MBIT-HOUR ALONG THE PERPENDICULAR FFs BY NEUTRON BEAM IRRADIATION.

Vulnerable Latch	Stored Value		Category			Average
			F0	F1	F2	
Master	QM=0	SEU	467	620	536	541
		MCU	57	114	92	88
		MCU/SEU	12.2%	18.4%	17.2%	16.3%
Slave	QS=0	SEU	435	522	524	494
		MCU	7	24	26	19
		MCU/SEU	1.6%	4.6%	5.0%	3.8%

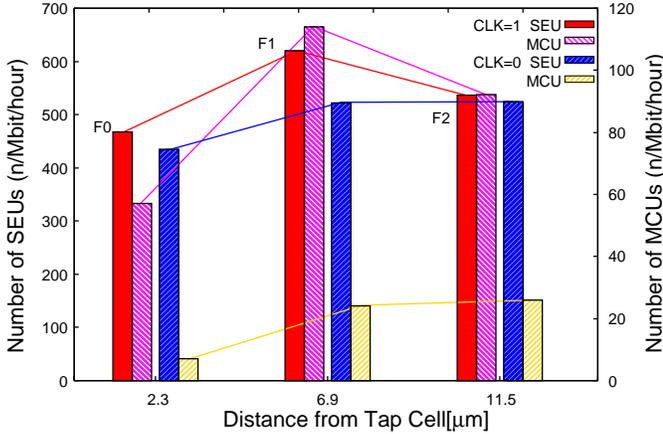


Fig. 11. Number of SEUs and MCUs per Mbit-hour according to the distance from tap cells.

well predicts SER ratios on the flip-flop array.

Table IV and Fig. 11 show number of SEUs and MCUs per Mbit-hour according to the distance from tap cells. As for SEU, FFs in F0 which are nearest to tap cells have less vulnerability compared with those in F1 and F2. But the difference is relatively small. Number of SEUs in F0 are around 15-30% smaller than those in F1 and F2. The SEUs in F1 and F2 are almost equivalent. It is consistent with the results of 150nm[7] and 45nm[8] SRAMs, in which only the SRAM cells nearest to the well-tap are robust to soft errors. The other SRAM cells have almost same vulnerability despite the distance from the well-tap. In our design, latches even at F0 are far from tap cells compared with the SRAMs in [7], [8].

As for MCUs, FFs at F0 is much less vulnerable than those at F1 and F2. Number of MCUs on master latches at F0 is almost 50% of those at F1 and F2 and that on slave latches is 30% respectively. It is because that tap cells prevent lateral bipolar transistors at F0 from turning on to keep the bulk potentials to the ground level. The farthest FFs (F2) is 1.6x and 3.7x more vulnerable than the nearest FFs (F0) when master and slave latches store 0 (QM=0 or QS=0) respectively.

Number of MCUs on slave latches are much less than that on master latches, since master latches are placed perpendicularly, while slave latches are placed diagonally as already shown in Fig. 4. Distances between the nearest transistors of

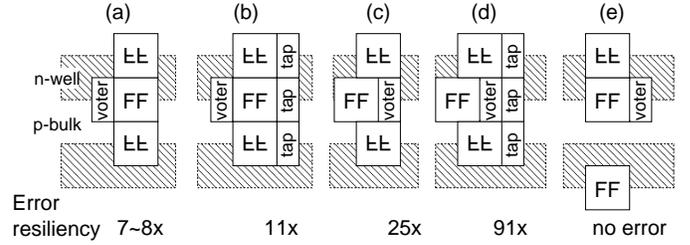


Fig. 12. Error resiliency of TMR FFs according to layout structures compared with the ordinal non-redundant FF.

the adjacent latches are $0.73\mu\text{m}$ for the master and $1.06\mu\text{m}$ for the slave. Resistance along the bulk relieves the bulk potential increased by a particle hit. Longer distance results in larger resistance, which prevent bulk potentials from going up.

V. HOW TO PROTECT MCUS ON TMR STRUCTURES

Experimental results on the neutron irradiation reveals that MCUs occur among adjacent FFs. If FFs constructing a TMR FF are closely laid out, it becomes high when multiple FFs are simultaneously flipped by an MCU. Fig. 12 depicts five different TMR layout structures. Fig. 12 (a, b) are the most vulnerable structures. The bottom two FFs may flip simultaneously by an MCU even if tap cells are closely laid out. The error resiliency of (b) is only 11x compared with the ordinal non-redundant FF. In Fig. 12 (c, d), the middle FF is displaced to separate master and slave latches of those FFs. If tap cells are closely laid out as in (d), its error resiliency is enhanced by 91x. Fig. 12 (e) shows the most robust layout structure. There is no FF whose p-bulk is shared. From the experimental results of our neutron irradiation, we expect no MCU occurs in this structure.

VI. CONCLUSION

We measured SEUs and MCUs of a 2.2Mbit flip-flop array constructed from tapless standard cells in a 65nm bulk CMOS process using accelerated white neutron beams. We observe both MCUs and SEUs. However, MCUs are observed only when master or slave latch stores a specific value. The highest SEU rate on the terrestrial environment is 2,900FIT/Mbit when the master latch stores 0, at which MCU happens once in every 6 SEUs.

SEU rates are almost constant despite the distance from tap, while MCU rates highly depend on it. The farthest FFs is 1.6x and 3.7x more vulnerable than the nearest FFs when master and slave latches are in the latch state respectively. In order to avoid MCUs, it is better to place FFs close to tap cells and to sparsely place each FF. If one of three FFs constructing a TMR FF is separately laid out without sharing p-bulk, we expect that no MCR occurs among these three redundant FFs in the TMR.

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