Analysis of the Distance Dependent Multiple Cell Upset Rates on 65-nm Redundant Latches by a PHITS-TCAD Simulation System

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Abstract

Recently, the soft error rates of integrated circuits is increased by process scaling. Soft error decreases the tolerance of VLSIs. Charge sharing and bipolar effect become dominant when a particle hit on latches and flip-flop. soft error makes circuit more sensitive to Multiple Cell Upset (MCU). We analyze the MCU tolerance of redundant latches in 65 nm process by device simulation and particle and heavy ion transfer code system (PHITS). The MCU rate of redundant latches is exponentially decreased by increasing the distance between redundant latches. These results coincide with the neutron experiments.

I. Introduction

SEU (Single Event Upset) is caused by radiation induced charge collection at a single sensitive node, such as the drain region of a single transistor. Radiation-hardened circuits, such as Triple Modular Redundancy (TMR), or Dual Interlocked storage Cell (DICE) [1] have been employed to suppress the effects of charge collection at a single circuit node. As circuits are scaled down, multiple node charge collection has an increasing impact on the response of the circuit [2]. Soft errors have become an increasingly troublesome issue for memories as well as combinational logic circuits. Soft error makes radiation-hardened circuit design more challenging.

Recently, the charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the charge sharing, also the bipolar effect become dominant when a particle hits on latches or flip-flops. Soft error makes radiation-hardened circuit more sensitive to Multiple Cell Upsets (MCUs) [3]. It is important to suppress the charge sharing and the bipolar effect to mitigate multiple node charge collection.

MCU rate depends on cell distance and well-contact density. In order to reduce radiation-induced multiple errors, each vulnerable transistor is placed on different p-well regions or separated over 1.1μm [4, 5]. The parasitic bipolar effect and the charge sharing also affect SEU [6] and Single Event Transient (SET) pulse widths [7]. Several device simulations results show that charge sharing can be suppressed by high well contact density, or separating the distance between transistors in 130 nm process [8, 9] and 90 nm process [10]. However, the experiments results of these references do not show the relationship between soft error rates and the distance between transistors clearly. The results of 65 nm process have not been presented either. To estimate soft-error rates and increase its resilience, it is necessary to measure characteristics of radiation-induced multiple cell upset.

In this paper, we analyze the impact of cell distance and well-contact density on neutron induced soft error rates of redundant flip-flops by a PHITS [11]-TCAD simulation system. There is only heavy ion model in TCAD simulator. The alpha particle and neutron induced soft error tolerance can be analyzed by PHITS. The proposed simulation system is similar to PHYSERD [12], while the simulation time is much shorter than PHYSERD. It is possible to forecast the soft error tolerance before create the test chips and irradiation experiments by the proposed simulation system.

This paper is organized as follows. Section II shows the impact of cell distance and well-contact density on redundant latches in device-level by PHITS-TCAD simulation system. We compare the simulations and neutron irradiation experimental results [13, 14] in this section. Section III concludes this paper.

II. MCU rates calculation by PHITS-TCAD simulation system

A. PHITS-TCAD simulation system

Fig. 1 portrays a flow chart of our simulation system by PHITS and TCAD. PHITS is devoted to simulations of secondary ion generation via nuclear interaction of an incident particle with constituent atoms in a device, and the sequential charge deposition. The secondary particles are generated when neutron particles hit silicon. PHITS can calculate the deposit energy when a secondary particle cross the sensitive volume of a device as shown in Fig. 1. The deposit energy (E_D) corresponds to the particle's lost energy.

In the TCAD simulation part, generated charge (Q_{gen}) is collected into drain by a particle hit as shown in Fig. 1. An SEU occurs in the circuit when Q_{gen} is large enough. We call it the threshold charge (Q_{th}), which is used to calculate the threshold deposit energy. $E_{deposit}$ can be

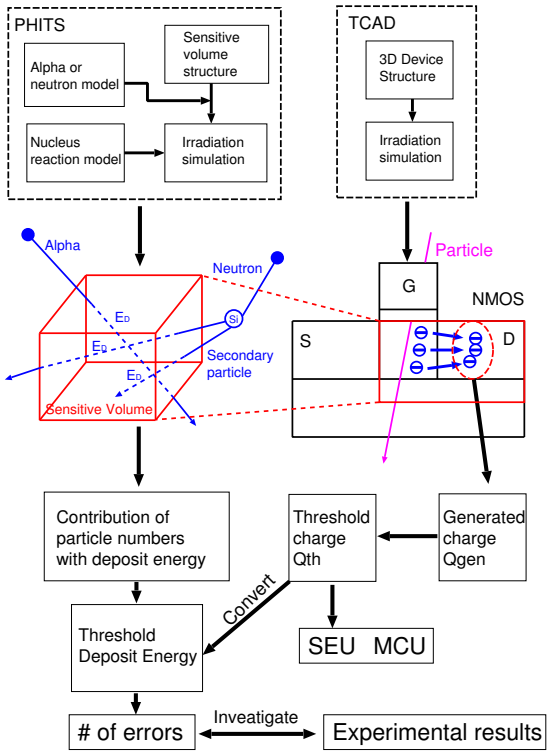


Fig. 1. Flow chart of the PHITS-TCAD simulation system.

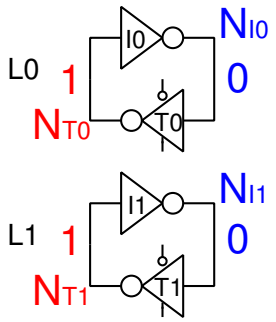


Fig. 2. Redundant latches Two unconnected independent latches).

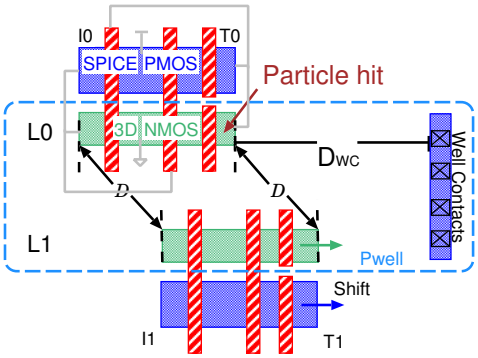


Fig. 3. Layout of two latches in two rows.

convert to the Q_{deposit}. 1 MeV E_{deposit} is equivalent to 50 fC Q_{deposit} [15] in this research.

A list of particle numbers with deposit energy is also obtained by PHITS. The particle, which deposit energy is larger than the threshold deposit energy, causes one SEU. According to the particle list, the total numbers of particles are equal to the number of SEUs.

B. *Device-level Simulation Setup*

In order to analyze the MCU tolerance of redundant latches, we examined several device-simulations by using the circuit as shown in Fig. 2. The circuit including two unconnected independent latches placed in two adjacent rows in a 65 nm bulk technology which is called redundant latches. The redundant latches are regarded as two latches in a TMR structure. A device simulator Sentaurus from Synopsys is used to do all device-level simulations. We assume that a radiation particle hits the tristate inverter T0 of the NMOS transistor of latch L0 in the odd row. The tristate inverter T1 can also be flipped by charge sharing and bipolar effect between T0 and T1. The layout structure of the redundant latches in two rows is shown in Fig. 3. All of the NMOS transistors are placed in the same P-well. Well contacts are placed side by side in the same well. The output nodes (N_{T0}, N_{T1}) of the tristate inverters T0 and T1 are initially set to "1". Output voltage of the tri-satate inverter is decreased by particle hits on the NMOS of the tristate inverter. The redundant latches are simultaneously flipped by charge sharing and bipolar effect.

Based on the circuit and layout structures, we construct a 3D device-level NMOS model as shown in Fig. 4. This 3D NMOS model is constructed in a triple well structure. The distance between the well contacts and latches is defined as D_{WC}. D is the distance between redundant latches L0 and L1. D is 0.3 μm when the redundant latches are aligned vertically as shown in Fig. 4. A Gaussian heavy-ion model is used in device simulations. The ion hits T0 at 0.1 ns from the beginning of simulation. Linear energy transfer (LET) is the energy of the heavy ion in device simulation.

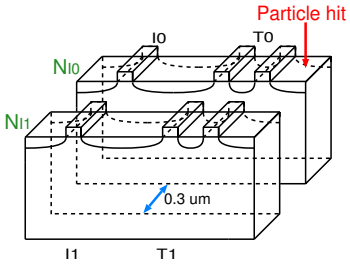


Fig. 4. 3D device-level structure of redundant latches in two rows. A particle hit at the tristate inverter T0.

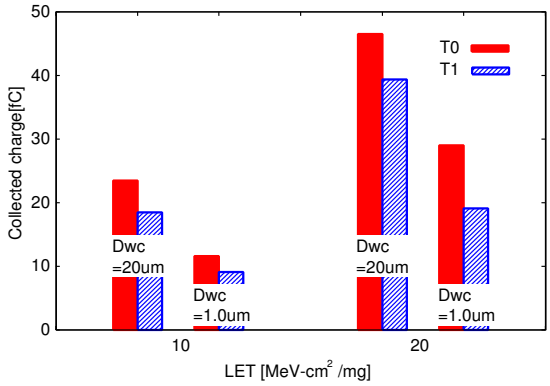


Fig. 5. Collected charge of the redundant latches L0 and L1 influenced by D_{WC}. LET is 10 and 20 MeV·cm^2/mg.

C. *Contribution of Well-contact Position to Suppress MCU*

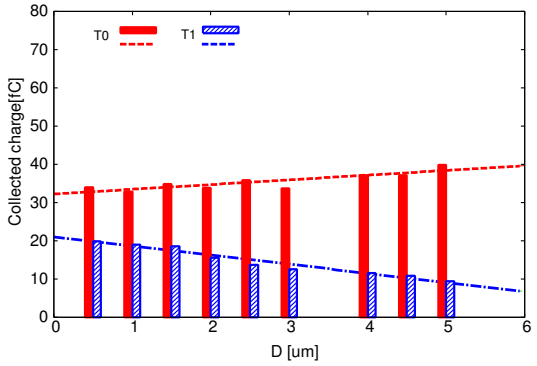
In order to analyze the relationship between well-contact position and MCU tolerance, we place the well contacts adjacent to latches, $\mathrm{D_{WC}}$ is shorten to 1.0 μm from 20 μm. LET of the ion particle are 10 and 20 MeV·cm^2/mg. The redundant latches are aligned vertically (D = 0.3 μm) in these simulations. The volumes of collected charge of L0 and L1 are shown in Fig. 5. When the distance D_{WC} is shorten from 20 μm to 1.0 μm, the magnitude of collected charge of the redundant latches L0 and L1 decreases by 50%. It is because the well potential under latches keeps steady by placing well contacts close to the latches. Bipolar effect under L0 and L1 is suppressed. Thus, less charge is collected into the redundant latches.

D. *Contribution of Cell Distance D to Suppress MCU*

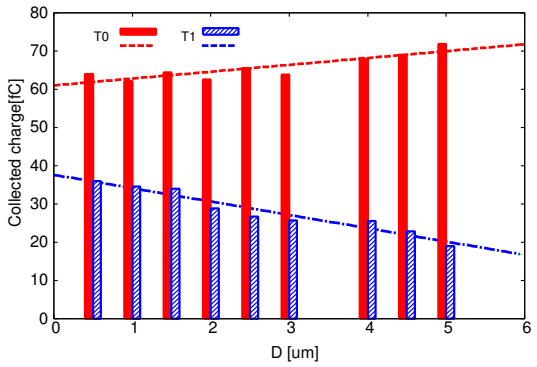
Fig. 6 shows the magnitude of collected charge of L0 and L1 when D is increased. D_{WC} is 20 μm. LET values of the ion particle are 10 and 20 MeV·cm^2/mg. The collected charge of L0 increases gradually while the collected charge of L1 decreases by increasing D as shown in Fig. 6. Less charge is collected into L1 as a function of D, for a given LET. Therefore, the charge sharing becomes weak between redundant latches by longer D. The collected charge of L0 becomes dominant. It is because less charge is shared by L1.

E. *MCU rates calculation and analysis*

Fig. 8 shows the model of sensitive volume used in the PHITS simulations. The volume of hole model is 4 μm × 4 μm × 12 μm. The red parts are sensitive area which volume is 0.2 μm × 0.2 μm × 0.5 μm. Neutron particles hit the device perpendicularly. The does is 10^9. The secondary particles are exported by the neutron nuclear reactions. The deposit energy is generated when the secondary particles hit the sensitive volumes. Table I shows



(a) LET=10 MeV·cm^2/mg



(b) LET=20 MeV·cm^2/mg

Fig. 6. Collected charge to L0 and L1 by increasing D. D_{WC}=20 μm.

the threshold Deposit energy and the number of SEUs and MCUs, the ratios of MCU/SEU are also shown in Fig. 8. The experimental results are also shown in Fig. 8. The results by PHITS-TCAD simulations are consistent with the experimental results. The ratio of MCU to SEU exponentially decreases by increasing D. The ratio of MCU to SEU decreases to 0.2% when D is longer than 5.0 μm.

III. Conclusion

We analyze the neutron induced MCU rates in the 65-nm bulk redundant latches. Based on the results of device simulations, we show that MCU is suppressed when the distance between the redundant latches (D) is increased. Total collected charge of L0 and L1 decreases by 50% by placing the well contacts adjacent to the redundant latches at which the distance between well contacts and redundant latches D_{WC} is 1.0 μm. According to the PHITS-TCAD simulation results and experimental results the ratio of MCU to SEU exponentially decreases by increasing the distance of latches D. The ratio of MCU to SEU decreases to 0.2% when D is longer than 5.0 μm. The PHITS-TCAD simulation results are consistent with the experimental results. It is possible to forecast the soft error tolerance before create the test chips and irradiation experiments by the proposed simulation system.

TABLE I
THE RATIOS OF MCU TO SEU BY PHITS-TCAD SIMULATION SYSTEM.

Distance	E_D	N_{SEU}	N_{MCU}	MCU/SEU
0.3μm	0.128	322	169	52.5%
0.5μm	0.177	322	115	35.7%
1.0μm	0.241	322	76	23.6%
1.5μm	0.366	322	35	10.9%
2.0μm	0.573	322	15	4.66%
2.5μm	0.658	322	11	3.42%
3.0μm	0.690	322	10	3.11%
4.0μm	1.097	322	1	0.31%

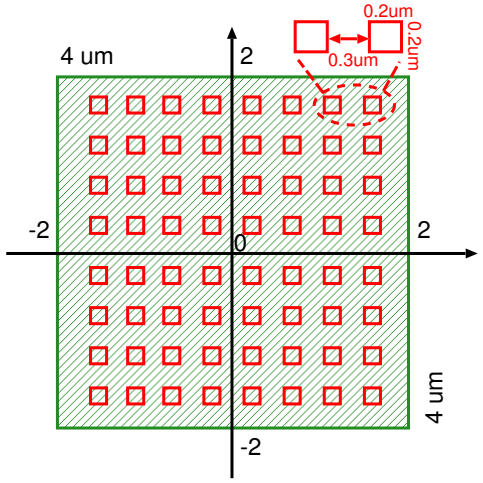


Fig. 7. Device model used in PHITS simulation.

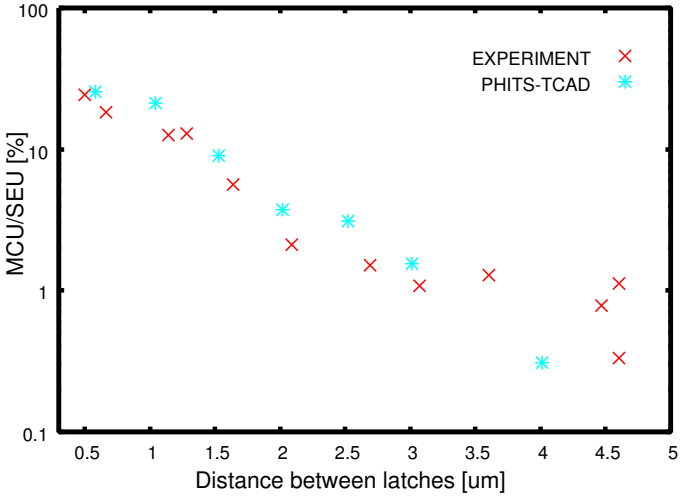


Fig. 8. The ratios of MCU to SBU by PHITS-TCAD simulation system and neutron irradiation experiments. The simulation results are consistent with the experimental results.

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