Radiation-hard Layout Structures on Bulk and SOI Process by Device-level Simulations

Kuiyuan Zhang, Kazutoshi Kobayashi
Dept. of Electronics, Kyoto Institute of Technology
Kyoto, Japan
kzhang@vlsi.es.kit.ac.jp

Abstract

This paper analyze the soft error tolerance related to layout structures on 65-nm bulk and SOI processes. The layout structure in which well contacts are placed between redundant latches suppresses MCU effectively. Also the tolerance of SOI structure transistor is estimated by TCAD simulations. The charge collection mechanism is suppressed by the BOX (Buried Oxide) in SOI transistor. Charge sharing and bipolar effects between SOI redundant latches are suppressed. There is no MCU occurrence in SOI redundant latches.

I. Introduction

SEU (Single Event Upset) is caused by radiation induced charge collection at a single sensitive node, such as the drain region of a single transistor. Radiation-hardened circuits, such as Triple Modular Redundancy (TMR), or Dual Interlocked storage Cell (DICE) [1] and Error Correction Code (ECC) [2] have been employed to suppress the effects of charge collection at a single circuit node. As circuits are scaled down, multiple node charge collection has an increasing impact on the response of the circuit [3]. Soft errors have become an increasingly troublesome issue for memories as well as combinational logic circuits. It makes radiation-hardened circuit design more challenging.

Recently, the charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the charge sharing, also the bipolar effect become dominant when a particle hit on latches or flip-flops. It makes radiation-hardened circuit more sensitive to Multiple Cell Upsets (MCUs) [4,5]. The parasitic bipolar effect and the charge sharing also affect SEU [6] and Single Event Transient (SET) pulse widths [7]. It is important to suppress the charge sharing and the bipolar effect to mitigate multiple node charge collection.

In this paper, the tolerance of three kinds of layout structures, which constructed on bulk process redundant latches, are compared by TCAD simulations in the section II. We also analyze the tolerance of SOI transistors in different conditions in section III. We conclude this paper in Section IV

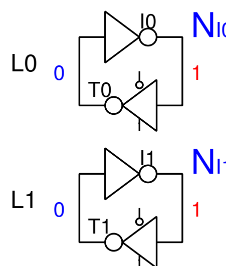


Fig. 1. Redundant latches.

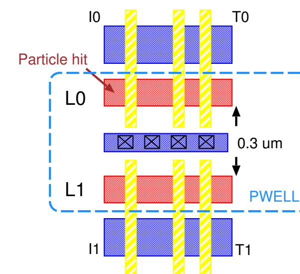


Fig. 2. layout structure A: well contacts are placed between latches.

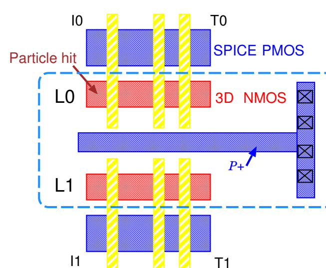


Fig. 3. Layout structure B: well contacts are placed beside latches with P+ tap between latches.

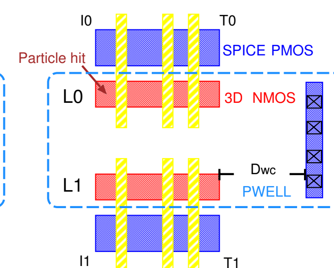


Fig. 4. Layout structure C: well contacts are placed beside latches without any tap.

II. Radiation-hard Layout Structures of Bulk Transistors

A. Three Kinds of Layout Structures

Fig. 1 shows a circuit including two latches placed on two adjacent rows in a 65nm bulk technology. Figs. 2-4 show three kinds of layout structures of the circuit. Structure *A* is a layout in which well contacts are placed between latches (Fig. 2). Structure *B* (Fig. 3) is a layout in which well contacts are placed beside latches with P+ tap between latches. Structure *C* (Fig. 4) is a layout in which well contacts are placed beside latches without any tap between redundant latches. In this section, the tolerance of these layout structures to soft errors are compared by TCAD simulations. In the layout structures *B* and *C*, the distance between latches and well contacts is defined as D_{WC}.

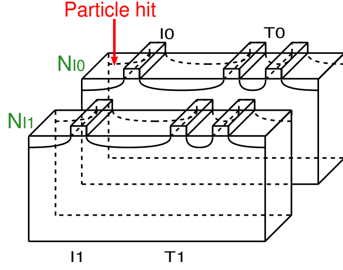


Fig. 5. 3D device-level structure of redundant latches in two rows. A particle penetrate at the drain of NMOS I0.

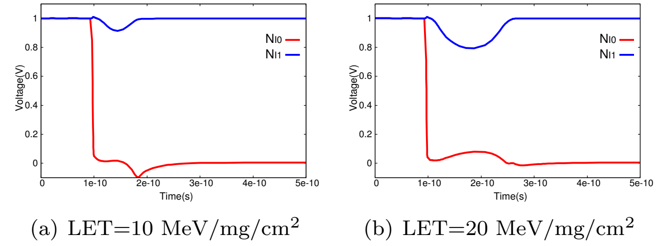
B. Simulation Setup

A device simulator Sentaurus is used to do all TCAD simulations. A radiation particle penetrates the NMOS transistor of the inverter I0 perpendicularly. All of the NMOS transistors are placed in the same P-well. The output nodes ($\mathrm{N_{I0}}$, $\mathrm{N_{I1}}$) of the inverter I0 and I1 are initial set to "1". Output voltage of inverter is decreased by charge collection and bipolar effects when a particle hits NMOS of the inverter. Thus, the redundant latches become very sensitive to a particle penetration. It is order to analyze the tolerance of each layout structure to MCU. The energy transferred by the radiation particle is described by its linear energy transfer (LET) value. LET is defined as the energy transferred (for electron-hole pair generation) by the radiation particle per unit length, normalized by the density of the target material (for VLSI designs, this is the density of Silicon). Thus the unit of LET is MeV/mg/cm^2. Based on the circuit and layout structures, we create a 3D device-level NMOS model as shown in Fig. 5. It is a triple well structure. The distance between the redundant latches L0 and L1 is 0.3 μm as shown in Fig 5. All device-level models are fabricated based on a 65 nm process.

C. Comparison of the Tolerance of Layout Structures

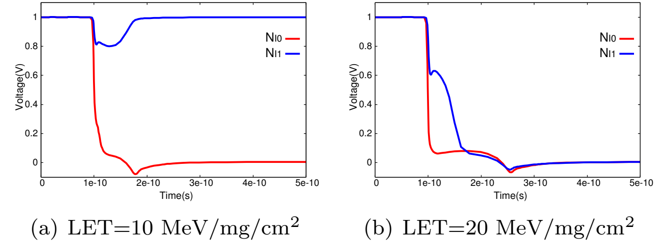
Fig. 6 shows two pairs of voltage outputs when a particle penetrates latch L0 of the layout structure A with LET=10 and 20 MeV/mg/cm^2. As the particle penetrates, the output $\mathrm{N_{I0}}$ of latch L0 upsets while the output $\mathrm{N_{I1}}$ does not upset as shown in Fig. 6(a) and (b). In this case, generated charge under the latch L0 can not cross over the well contacts to the L1 side. Thus the charge sharing between L0 and L1 is almost prevented. The bipolar effects [8] is also suppressed effectively, because the well contacts suppress the well potential elevation.

Fig. 7 shows another two pairs of voltage outputs when a particle penetrates latch L0 in the layout structure B with LET=10 and 20 MeV/mg/cm^2. The output N_{I0} of latch L0 upset while the output $\mathrm{N_{I1}}$ does not flip when LET=10 MeV/mg/cm^2 as shown in Fig. 7(a). However, when LET is increased to 20 MeV/mg/cm^2, node $\mathrm{N_{I0}}$ and $\mathrm{N_{I1}}$ are flipped simultaneously as shown in Fig. 7(b),



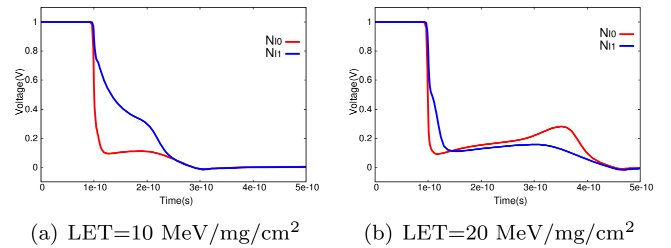
(a) LET=10 MeV/mg/cm^2 (b) LET=20 MeV/mg/cm^2

Fig. 6. The voltage outputs of redundant latches in layout structure A by a particle.



(a) LET=10 MeV/mg/cm^2 (b) LET=20 MeV/mg/cm^2

Fig. 7. The voltage outputs of redundant latches in layout structure B by a particle.



(a) LET=10 MeV/mg/cm^2 (b) LET=20 MeV/mg/cm^2

Fig. 8. The voltage outputs of redundant latches in layout structure B by a particle.

MCU occurs in the layout structure B by a higher energy particle.

When the redundant latches are constructed in the stucture C, the voltage outputs by the paticle are shown in Fig. 8. The well contacts is placed beside latches in the structure C. It cannot suppresses well potential elevation effectively. The charge sharing and bipolar effects appear in the structure C. Thus, both latches upset simultaneously when LET=10 and 20 MeV/mg/cm^2 as shown in Fig. 8(a) and 8(b). Table I shows the threshold LET of the three kinds of layout structures. The threshold LET of MCU on the structures B and C are decreased by 52.86% and 23.71% compared with that on A respectively.

Fig. 9 shows the threshold LET of the particle which upsets the redundant latches simultaneously according to $\mathrm{D_{WC}}$. The threshold LET exponentially decreases when the distance between well contact and the redundant latches, $\mathrm{D_{WC}}$ is increased. The LET of the structure B is bigger than that of C. The LET of the structure C reduces steeper than structure B when $\mathrm{D_{WC}}$ is increased. It is because that the p+ tap between latches stabilizes the well potential of structure B. The well potential of B do not change lot by a particle. The well potential

TABLE I
THE THRESHOLD LET OF THE THREE KINDS OF LAYOUT STRUCTURES.

Layout structure	LET of SEU	LET of MCU
A	7.0	35.0
B	6.3	18.5 (52.86% of *A*)
C	5.2	8.3 (23.71% of *A*)

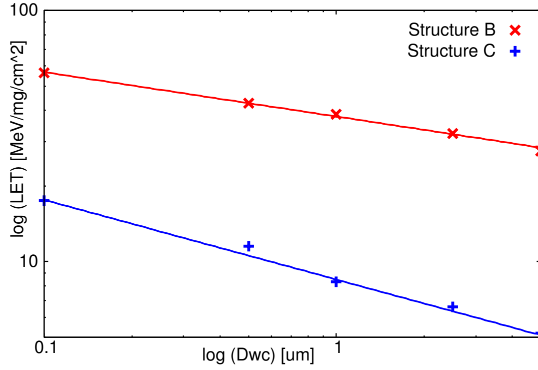


Fig. 9. LET of paticle which upset redundant latches simultaneously accroding to D_{WC}.

of C is stabilized when well contacts are placed close to latches. It makes structure C stronger to particle. However, the tolerance of structure C becomes weaker when well contacts are placed far away from latches.

III. The Tolerance of SOI Transistors to Soft Error

In this section, the tolerance of SOI transistor is analyzed by TCAD simulations. Fig. 10 shows an SOI model. A 10 nm BOX (Buried Oxide) [9] is placed under drain and source regions. The depth of the SOI (transistor) region is 12 nm. This SOI transistor is constructed based on a 65 nm process. The tolerance of redundant SOI latches are compared in this section. In this section, a conventional latch circuit as Fig. 1 are used in device-level simulations.

A. *Tolerance Analysis by Changing Particle Penetrate Positions*

Fig. 11 shows the voltage outputs when a particle penetrates drain and gate region of SOI redundant latches respectively. the LET of the particle are 10, 20 and 50 MeV/mg/cm^2. As the charge collection is suppressed by BOX, little charge is collected into drain when a particle penetrates the drain region. The latches do not flip as shown in Fig. 11(a). When a particle penetrates gate region of the SOI latches, the voltage output does not upset when LET=10 MeV/mg/cm^2. However, the outputs start to upset when the LET is increased to 20 MeV/mg/cm^2

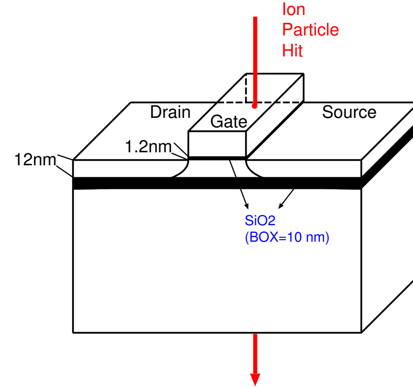
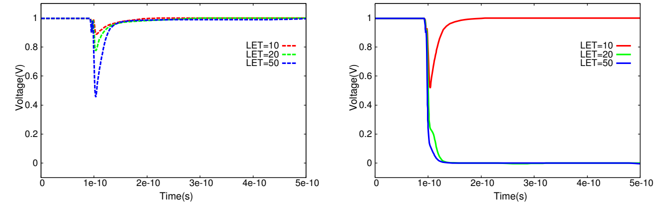


Fig. 10. 3D device-level SOI transistor.



(a) The particle penetrate on drain region

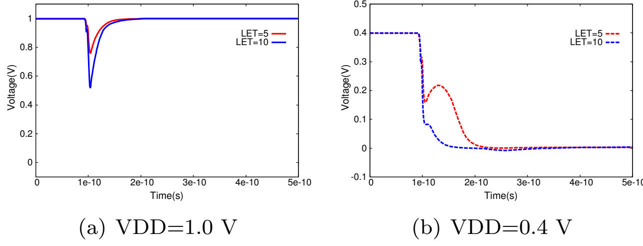
(b) The particle penetrate on gate region

Fig. 11. The voltage outputs of redundant latches in layout structure B by a particle.The voltage outputs of SOI latch by a particle. LET=10, 20 and 50 MeV/mg/cm^2.

as shown in Fig. 11(b). Large amount of charge is collected into drain when a particle penetrates the gate region and crosses the body region of the SOI transistor. The parasitic bipolar transistor of SOI turns on by the body potential elevation. The possibilites when a particle hits on the small gate region is much smaller than that on the much larger drain region. Even when a particle hit on the gate region. generated charge is very small because of the smaller sensitive volume on the gate region over BOX. Thus, SOI transisitors become much stronger than bulk transistors. It makes SOI transistors become weak to high energy particle.

B. *Tolerance Analysis by VDD Scaling*

Fig. 12 shows the voltage outputs by a particle whcih penetrates the gate region. The VDD is set in 1.0V and 0.4V respectively. There is no dopant in the channel of SOI transistors. Variations are suppressed in the SOI structure. Thus, the VDD of SOI transistors can be decreased as low as 0.4V. The LET of the ion particles are 5 and 10 MeV/mg/cm^2. When the VDD is 1.0V, the outputs does not upset as shown in Fig 12(a). The charge collection mechanism is suppressed by BOX of SOI transistors. However, when VDD is scaled to 0.4V, the outputs start to upset as shown in Fig. 12(b). The tolerance of SOI transistor to soft error decreases by VDD scaling.



(a) VDD=1.0 V (b) VDD=0.4 V

Fig. 12. The voltage outputs of SOI latch by a particle penetrate on gate region. LET=5 and 10 MeV/mg/cm^2.

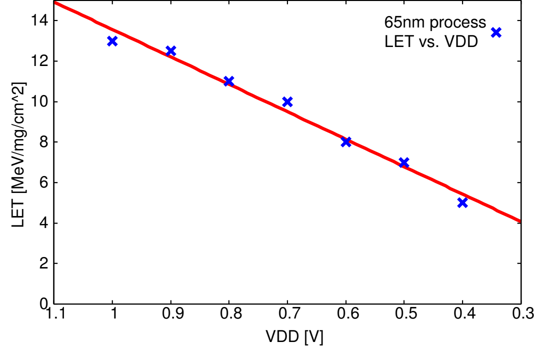
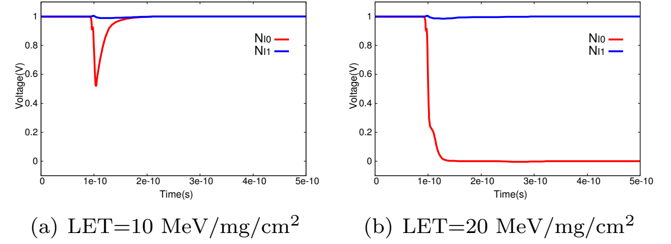


Fig. 13. LET of particle which upset SOI latch vs. VDD

The relationship between power supply voltage and the tolerance of SOI transistors is shown in Fig. 13. The tolerance of SOI transistor to soft error linearly decreases by VDD scaling.

C. *Comparison the Tolerance between Bulk and SOI Redundant Latches*

Fig. 14 shows the voltage outputs when a particle penetrates SOI redundant latches. The LET of the particle are 10 and 20 MeV/mg/cm^2. The redundant latches are constructed in the layout structure C, which sensitive to soft errors as described in Section II. It is order to compare the tolerance between SOI and Bulk structures. When LET=10 MeV/mg/cm^2, the SOI redundant latches do not upset as shown in Fig. 14(a), while the bulk redundant latches upset simultaneously as shown in Fig.8(a). When LET is increased to 20 MeV/mg/cm^2, only the output N_{I0} upsets as shown in Fig. 14(b), while N_{I0} and N_{I1} upset at the same time as shown in Fig. 8(b). The BOX on the SOI structure suppresses the charge sharing and bipolar effects between the latches L0 and L1 strongly. MCUs are suppressed in SOI redundant latches, even though layout structure C is used. Table II shows the threshold LET when SEU(MCU) occurs in SOI and bulk redundant structure. The threshold LET of SEU is decreased by 44% cpmpared with that on A when the redundant latches are fabricated in bulk structure instead of SOI. There is no MCU occurrence in SOI redundant latches. Thus, the tolerance of SOI redundant latches to soft error is stronger than bulk structure according to the results of TCAD simulations.



(a) LET=10 MeV/mg/cm^2 (b) LET=20 MeV/mg/cm^2

Fig. 14. The voltage outputs of SOI redundant latches by a particle penetrate on gate region of latch L0. LET=10 and 20 MeV/mg/cm^2.

TABLE II
THE THRESHOLD LET OF SOI AND BULK REDUNDANT LATCHES IN LAYOUT C.

Structure	LET of SEU	LET of MCU
SOI	12.4	N/A
Bulk	5.2 (44% of SOI)	8.3

IV. Conclusion

Based on the results of TCAD simulations, between the bulk structures we show that the layout structure in which well contacts are placed between latches suppresses MCUs effectively. The charge sharing mechanism and bipolar effects are suppressed by these well contacts. No MCUs occurs in this kind of layout structure. In SOI structures, there is little charge collected into the drain region. It increases the tolerance of SOI transistor to soft errors. The gate region of SOI is sensitive to high energy particle. The tolerance of SOI transistors linear decreased by VDD scaling. However, MCUs do not occur in SOI redundant latches in any layout structure by TCAD simulations.

References

[1] D. Krueger, E. Francom, and J. Langsdorf. Circuit Design for Voltage Scaling and SER Immunity on a Quad-Core Itanium Processor. In *ISSCC*, pages 94–95, Feb. 2008.

[2] Ando, H., Seki, K., Sakashita, S., Aihara, M., Kan, R., Imada, K., Itoh, M., Nagai, M., Tosaka, Y., Takahisa, K. et al.: “Accelerated Testing of a 90nm SPARC64V Microprocessor for Neutron SER”, *The Third Workshop on System Effects on Logic Soft Errors* (2007).

[3] B.D. Olson, D.R. Ball, K.M. Warren, L.W. Massengill, N.F. Haddad, S.E. Doyle, and D. McMorrow. Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design . In *Nuclear Science, IEEE Transactions on*, number 52 , Issue: 6, pages 2132 – 2136, Dec. 2005.

[4] Wen, S., Wong, R., Romain, M. and Tam, N.: "Thermal Neutron Soft Error Rate for SRAMS in the 90NM – 45NM Technology Range", *Reliability Physics Symposium (IRPS), 2010 IEEE International*, pp. 1036 –1039 (2010).

[5] G. Gasiot, D. Giot, and P. Roche. Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering. *IEEE Transactions on Nuclear Science*, 54(6):2468 –2473, December 2007.

[6] K. Zhang, R. Yamamoto, J. Furuta, K. Kobayashi, and H. Onodera. Parasitic bipolar effects on soft errors to prevent simultaneous flips of redundant flip-flops. In *IEEE International Reliability Physics Symposium (IRPS)*, pages 5B.2.1 –5B.2.4, April 2012.

[7] N.M. Atkinson, A.F. Witulski, W.T. Holman, J.R. Ahlbin, B.L. Bhuva, and L.W. Massengill. Layout technique for single-event transient mitigation via pulse quenching. *IEEE Transactions on Nuclear Science*, 58(3):885 –890, June 2011.

[8] K. Zhang, J. Furuta, R. Yamamoto, K. Kobayashi, and H. Onodera A Radiation-Hard Redundant Flip-Flop to Suppress Multiple Cell Upset by Utilizing the Parasitic Bipolar Effect. *IEICE trans. 2012CDP0013*, Vol.E96-C, No.4, pp. 511-517, Apr. 2013.

[9] R. Tsuchiya, M. Horiuchi, S. Kimura, et al. Silicon on thin BOX: a new paradigm of the CMOSFET for low-power high-performance application featuring wide-range back-bias control. *Proceedings IEDM 2004*, pp.631-634, Dec. 2004.