Impact of Drive Strength and Well-contact Density on Heavy-ion-induced Single Event Transient

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Abstract—We measure distributions of heavy-ion-induced Single Event Transient (SET) pulse widths from the 4 kinds of inverter chains to measure their characteristics and estimate SET-induced soft error rates on a Flip-Flop (FF) and a delayed TMR FF. Test chip was fabricated in 65-nm bulk CMOS process and measurement results show that maximum SET-induced soft error rate on a FF is equivalent to 20% of Single Event Upset (SEU) rate. On the delayed TMR with 400ps delay element, SET-induced soft error rate can be reduced from 2 $\times 10^{-10}$ cm^2/inv to less than 2 $\times 10^{-11}$ cm^2/inv by using 4x inverters with 2μm well-contact distance.

I. Introduction

Radiation-induced soft errors are a significant concern for LSI reliability, as they flip stored value in a memory cell. A particle generates electron-hole pairs during penetrating into silicon bulk. Generated minority carriers are collected by drain diffusion and flip transistor's output transiently. Radiation-induced soft errors are classified into SEU and SET according to a location of a particle hit. SEU is induced in a memory cell such as FFs or SRAMs and directly flips its stored value, while SET is induced in the combinational logic and injects a temporal pulse. An SET will cause an error only if it propagates and gets stored in a FF. Therefore, error rate due to SET depends on the clock frequency [1].

To reduce soft error rate, Triple Modular Redundancy (TMR) FF is commonly used. Fig. 1 shows the delayed TMR FF which is constructed by three FFs, a voter circuit, and two delay elements [2]. Since output is decided by a majority vote of stored values, an SEU can be removed. Two delay elements prevent an SET pulse from being capturing by multiple FFs. However, if an SET pulse width is bigger than delay time of the delay element, multiple FFs may capture SET pulse simultaneously. Therefore, there are trade-off between operation speed and SET mitigation. To achieve suitable SET mitigation, we need to measure SET pulse width and its characteristic.

In this paper, we measure pulse width distributions of heavy-ion-induced SETs from 4 kinds of inverters to es-

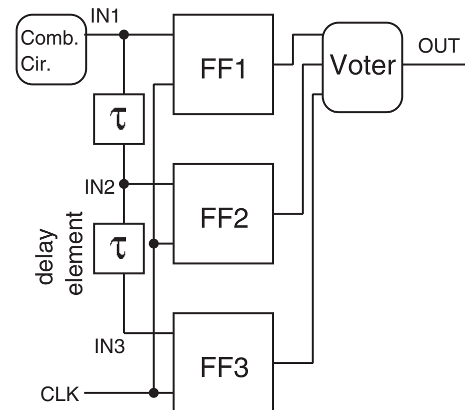

Fig. 1. Delayed Triple Modular Redundancy FFs.

timate SET-induced soft error rates on the FF and the delayed TMR FF. Accelerated tests were performed the Takasaki Ion Accelerators for Advanced Radiation Application (TIARA) of Japan Atomic Enery Agency (JAEA). A measurement circuit for SET pulse width was used to evaluate neutron-induced SET pulse width [3]. The rest of this paper is organized as follows. Section II explains the circuit structure to measure SET pulse widths, Section III shows our heavy-ion-beam experimental setup in TIARA, followed by Section IV which shows experimental results by accelerated test. Section V concludes this paper.

II. SET Pulse Width Measurement Circuit

To measure distribution of SET pulse widths by the accelerated test, we implement SET pulse width measurement circuit which contains a time-to-digital converter (TDC) and a target circuit constructed by logic gates. The target circuit functions as the source of SETs and TDC measures pulse width of an SET caused on the target circuit.

A. *Implemented Time-to-digital Converter*

Fig. 2 shows the time-to-digital converter based on a ring oscillator[3].

If an SET is injected from the target circuit, one input

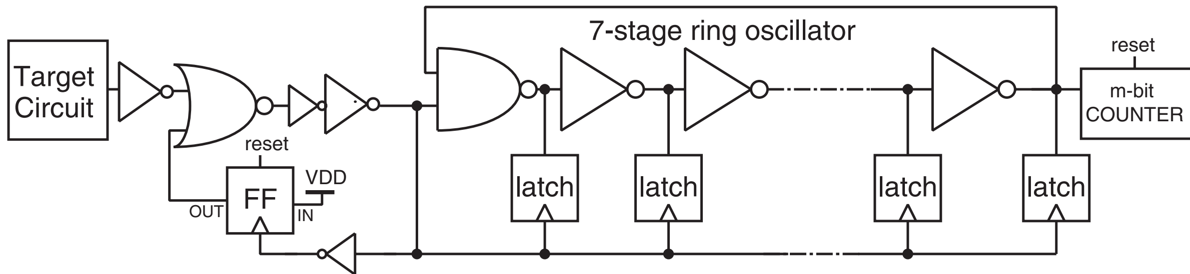

Fig. 2. SET pulse width measurement circuit.

of NAND gate turns to "1" by the SET. The ring oscillator keeps on oscillating while the SET pulse is injected. The counter counts the number of oscillation and the latches hold each output value of the logic gates in the oscillator immediately when ring oscillator stops. Then, the SET pulse width can be computed by the number of oscillation stored in the counter and the states of the latches. Thus, the proposed circuit can measure SET pulse width by the resolution of each gate delay. In this circuit, to detect SET occurrence and prevent further SET capture, we implement a FF and a NOR gate as shown in Fig. 2.

B. *Target Circuit Structure*

The target circuit construction is the most important factor to measure SET pulse widths accurately. It is because that when an SET is injected into the target circuit, it linearly shrinks or expands as it propagates by a propagation-induced effect [4]. Therefore, if a long inverter chain are implemented as the target circuit, measured pulse width strongly depends on where an SET is injected.

Fig. 3 shows the target circuit structure based on [1]. It contains 16 chains of 50 inverters to reduce the propagation-induced effect. They are connected to the TDC by NOR and NAND gates tree. Therefore, the TDC also measure an SET pulse width on the NAND and NOR gates. However, the total number of NAND and NOR gates is 15 and it is relatively low compared with 800 inverters. We implement 1x and 4x inverter chains with 2 kinds of well-contact distance, 50 μm or 2 μm to measure impact of the drive strength and the well-contact density (distance) on the distribution of the SET pulse widths.

III. Experimental Setup

Fig. 4 shows a test chip micrograph fabricated in a 65-nm bulk CMOS process. It has twin-well structure and its supply voltage is 1.2 V. In order to measure heavy-ion-induced SET pulse widths, 180 units of the proposed circuit are implemented with four different types of inverter chains as shown in Table I. In this test chip, we also implement shift registers to measure SEU rate on FFs and compare it to SET rate on inverters. All units are implemented in a 1.1×0.7 mm^2 region on a 4×2 mm^2 die.

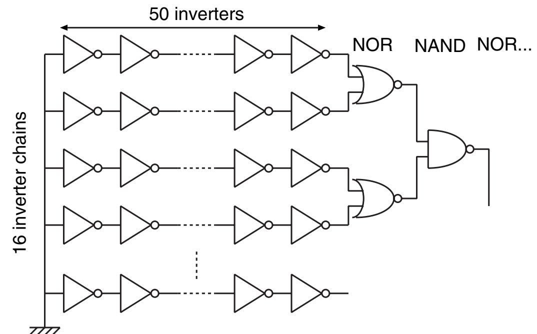

Fig. 3. Target circuit structure including 800 inverters, 10 NOR gates, and 5 NAND gates.

Fig. 4. Chip micrograph.

Accelerated tests were performed at TIARA. The test chip was irradiated in a vacuum chamber with a broad beam of N, Ne, Ar and Kr. Linear Energy Transfer (LET) of the ions are listed in Table II. These ions were irradiated normal angle to the chip surface.

IV. Experimental Results and Discussions

In this section, we show measurement results of SET pulse widths and SET rates on inverter chains. To show SET rate, we use cross section [cm^2/inv.] which is calcu-

TABLE I
Structures and drain areas of inverters. Drain areas are normalized to that of 1x inverter.

Drive Strength	well-contact distance	Drain Area	
		PMOS	NMOS
4x	50μm	2.5	2.2
	2μm	2.5	2.2
1x	50μm	1	1
	2μm	1	1

TABLE II
IONS AND LET USED FOR ACCELERATED TEST.

ion	LET[MeV-cm^2/mg]
N	3.1
Ne	6.1
Ar	15.8
Kr	40.3

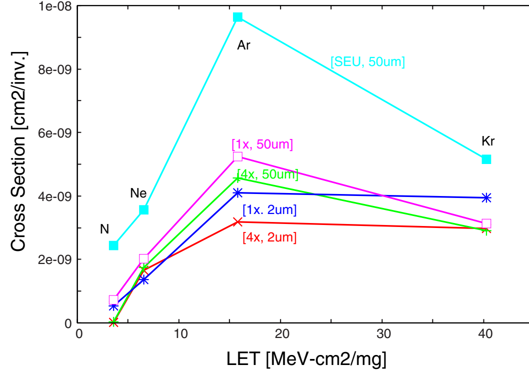

Fig. 5. SET rates on inverters and SEU rate on FFs.

lated according to the following equation.

$$\text{Cross Section} = \frac{(\text{num. of SETs})}{\text{fluence} \times (\text{num. of inv.})} \quad (1)$$

where, fluence is the number of irradiated ions during accelerated tests.

A. SET Rates on Inverter Chains and SEU Rate on FFs

Fig. 5 shows SET rates on inverters and SEU rate on FFs. X-axis shows LET and y-axis shows cross section which is calculated by Eq. (1). 4x inverters have smaller SET rate than 1x inverters. Especially, 4x inverters have almost 0 cm^2/inv at LET = 3.1 MeV-cm^2/mg. This result shows that amount of charge generated by electron-hole pairs is smaller than that of gate capacitance of 4x inverter and generated charge cannot flip output of 4x inverter when LET of irradiated ion is less than 3.1 MeV-cm^2/mg. In this measurement, when well-contact distance is 50 μm, SET rates and also SEU rate are decreased at LET = 40.3 MeV-cm^2/mg. We assume heavy ions with higher LET generate widespread electron-hole pairs and they affect multiple transistors. In this case, SET occurrence mechanism becomes more complex like pulse quenching [5]. Compared with SEU rates on FF, SET rates are 2x – 4x smaller than SEU rate. Since combinational circuits consist of a lot of logic gates, SET rate is not negligible for LSI reliability in 65-nm process.

B. Distributions of SET Pulse Widths

Fig. 6 shows average SET pulse widths and Fig. 7 shows distributions of SET pulse widths on each inverter chains. Average SET pulse width is increased by increase in the LET of irradiated ions. However, SET pulse width is widely distributed. SET pulse width depends on not only the LET but also the location of ion strike. Average SET pulse width can be reduced by using inverter with higher drive strength or shorter well-contact distance.

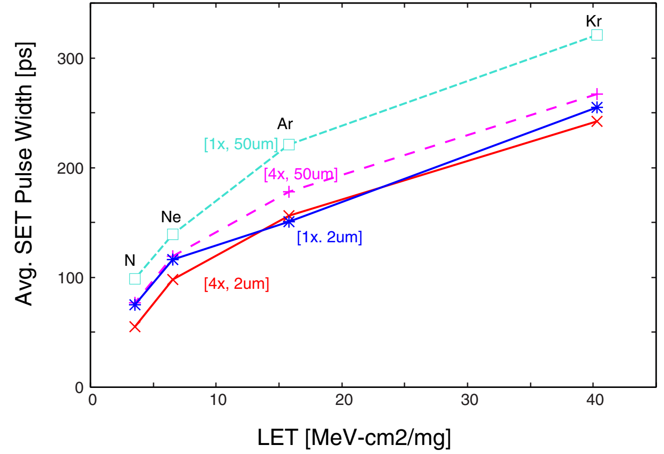

Fig. 6. Average SET Pulse Widths on Each Inverter.

C. Estimation of Soft Error Rate by SET on FF and TMR FF

Soft error by SET is caused when SET is captured in a FF. The probability that the FF stored SET is determined by SET pulse width (p) and clock frequency (f). Therefore, SET-induced soft error rate in the FF ($\text{SER_FF}_{\text{SET}}(f)$) is determined as the following equation[6].

$$\text{SER_FF}_{\text{SET}}(f) = \sum_{p=w}^{1/f+w} N_{\text{SET}}(p) \frac{p-w}{1/f} \quad (2)$$

where $N_{\text{SET}}(p)$ denotes the rate of the SET pulse width p, which is obtained from measurement results as shown in Fig. 7. Parameter w is latching window time which is equivalent to sum of setup time and hold time of a FF.

In the case of a delayed TMR FF, SET-induced soft error rate ($\text{SER_TMR}_{\text{SET}}(f)$) depends on the delay parameter (τ) of delay elements. Fig. 8 shows three conditions of filtering SET pulse by delay elements. By considering these three conditions, $\text{SER_TMR}_{\text{SET}}(f)$ is expressed as follows.

$$\begin{aligned} \text{SER_TMR}_{\text{SET}}(f) &= 2 \sum_{p=\tau+w}^{2\tau+w} N_{\text{SET}}(p) \frac{p-w-\tau}{1/f} \\ &\quad + \sum_{p=2\tau+w}^{1/f+w} N_{\text{SET}}(p) \frac{p-w}{1/f} \quad (3) \end{aligned}$$

When delay elements are not inserted ($\tau = 0$), $\text{SER_TMR}_{\text{SET}}(f)$ is equivalent to $\text{SER_FF}_{\text{SET}}(f)$

Fig. 9 shows $\text{SER_TMR}_{\text{SET}}(1\text{GHz})$ calculated by Eq. (3) and measurement results. When irradiated ions

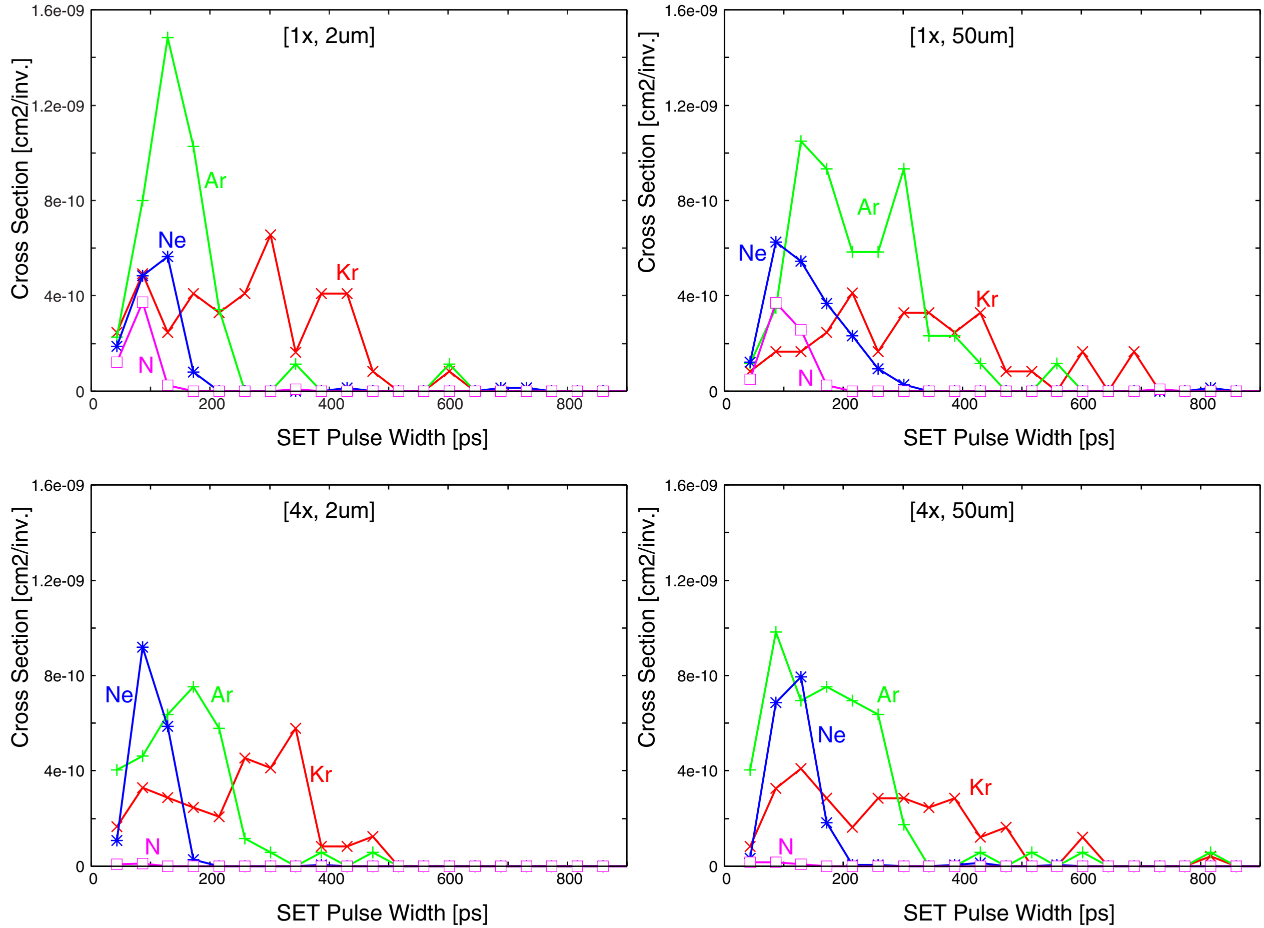

Fig. 7. distributions of SET pulse widths on inverters.

are N or Ne, $\text{SER_TMR}_{\text{SET}}(1\text{GHz})$ can be eliminated by 200ps delay elements. In contrast, when irradiated ions are Ar or Kr, we need to implement over 400 ps delay elements to reduce it to less than 2 $\times 10^{-10}$ cm^2/inv. However, when we implement higher drive strength inverters with shorter well-contact distance, we can achieve $\text{SER_TMR}_{\text{SET}}(1\text{GHz}) < 2 \times 10^{-11}$ cm^2/inv by using 400 ps delay element. Compared with SEU rates as shown in Fig. 5, $\text{SER_FF}_{\text{SET}}(1\text{GHz})$ ratios by N, Ne, Ar, and Kr are ∼3%, ∼8%, ∼12%, and ∼20% respectively. Therefore, SET mitigation technique is also necessary for LSI reliability according to the number of logic gates on combinational circuits and we can reduce SET-induced soft error rate on delayed TMR by using higher drive strength inverters with shorter well-contact distance.

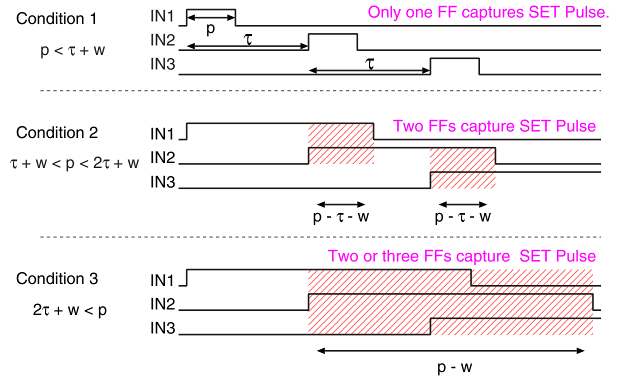

Fig. 8. Filtering a SET pulse by delay elements.

V. Conclusion

We measure distributions of heavy-ion-induced SET pulse widths from the 4 kinds of inverter chains to measure its characteristic and estimate SET-induced soft error rates on the FF and the delayed TMR FF. We also measure SEU rates on FFs to compare with SET rates and SET-induced soft error rates. Measurement results show that SEU rate is 9.64×10^{-9} cm^2/bit and SET rates are 3.18×10^{-9} cm^2/inv – 5.25×10^{-9} cm^2/inv when irradiated ions are Ar (LET = 15.8 MeV-cm^2/mg). Maximum SET-induced soft error rate on a FF is equivalent to 20% of SEU rate. SET mitigation technique is also necessary for LSI reliability since combinational circuits consist of a lot of logic gates. On the delayed TMR with 400ps delay element, SET-induced soft error rate can be reduced from 2 $\times 10^{-10}$ cm^2/inv to less than 2 $\times 10^{-11}$ cm^2/inv by using 4x inverters with 2μm well-contact distance. We

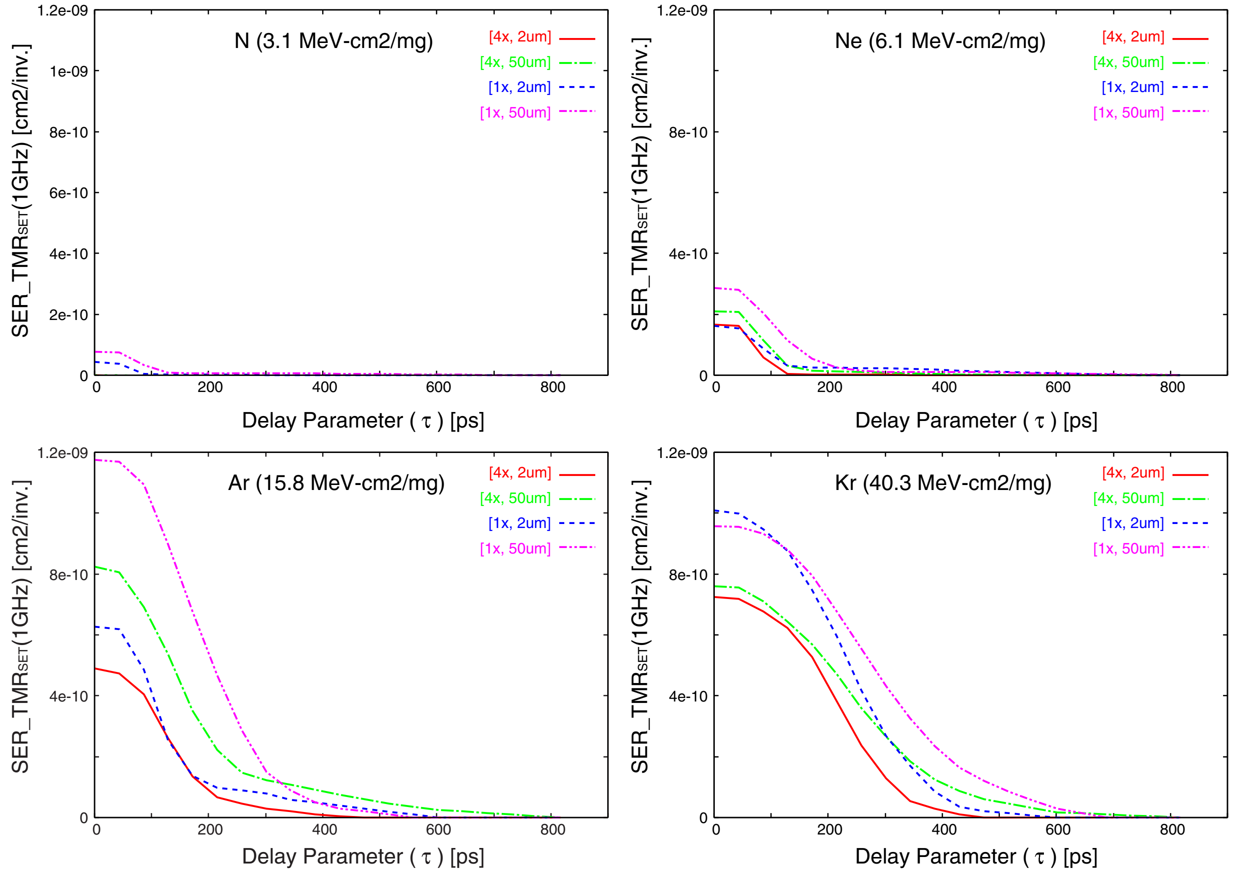

Fig. 9. SET-induced soft error rates on the delayed TMR FF.

can reduce SET-induced soft error rate on delayed TMR by using higher drive strength inverters with shorter well-contact distance.

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