Device-level Simulations of Parasitic Bipolar Mechanism on Preventing MCUs of Redundant Flip-Flops

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Abstract— Parasitic bipolar mechanisms can effectively prevent MCUs of redundant flip-flop, which improve the tolerance of soft errors. Device-level simulations reveals that no MCU occurs in redundant latches storing the opposite values by the parasitic bipolar effect, while MCU occurs by a particle hit with high energy in the redundant latches storing the same value.

I. Introduction

Various redundant flip-flop structures are proposed such as TMR, DICE [1] or BISER [2] to mitigate soft errors. However, aggressive process scaling makes the probability of multiple cell upsets (MCUs) greater. MCUs are one of critical issues to diminish soft-error resiliency of radiation-hard designs because these designs are very weak to simultaneous flips. Parasitic bipolar transistors play an important role on soft errors in a current deep-submicron process [3]. If a particle hit on a transistor, adjacent transistors are affected by parasitic bipolar effects, which results in an MCU of redundant components.

In this paper, we introduce a robust structure of redundant latches by storing the opposite values so as to prevent any simultaneous flip. Device-level simulations show that the robust structure can effectively prevent simultaneous flip by a particle hit.

II. Parasitic Bipolar Mechanism on Preventing Soft Error

Fig. 1 shows a conventional latch structure and its layout. We set "1" to be the output (which is named by N1) of I0 and set "0" to be the tristate inverter T0's output (N0). Therefore, NMOS in I0 and T0 is OFF and ON, respectively. Fig. 2 and 3 show two device-level simulation results with LET=0.1 pC/μm and 5 pC/μm respectively when a particle hit on the NMOS transistor in I0. It can be found that the output voltage of I0 is flipped as shown in Fig. 2 by a particle hit on the NMOS of I0. It is because of the NMOS in I0 is turned to "ON" from "OFF" by the bipolar effect. Then the NMOS of T0 have to change its state by the changing input (the output of I0). So soft-error occured. However, suppose that a particle hit has enough energy so that not only the well potential of I0 but also the well potential of T0 will rise up.

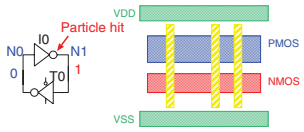

Fig. 1. Latch with inverter I0 and tristate inverter T0

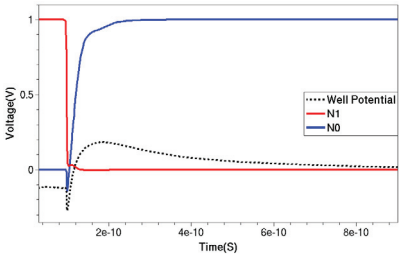

Fig. 2. device simulation with LET=0.1 pC/μm

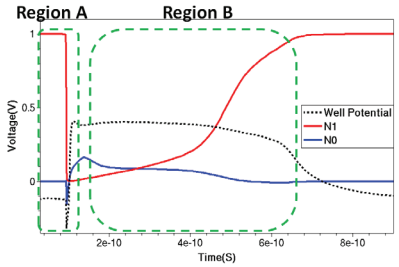

Fig. 3. device simulation with LET=5 pC/μm

Then the parasitic bipolar transistor of T0 is turned on. It may keep the NMOS in T0 hold "ON" instead of being changed to "OFF", so eventhough N1 goes down at first as shown in region A of Fig. 3, it can go back to its original value as show in region B of Fig. 3.

Thus the latch does not flip by the parasitic bipolar effects. It is possible to enforce redundant flip-flops to soft errors by utilizing these bipolar effects. These parasitic bipolar effects are more dominant in the triple-well than in the twin well since both p- and n-wells are floating in the triple well. SRAMs in the triple well has 3.5x higher probability of MCUs com-

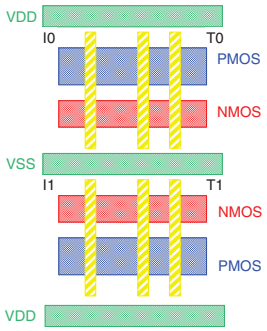

Fig. 4. Two redundant Latches on the double-height structure

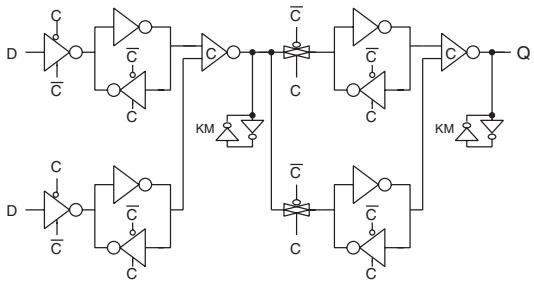

Fig. 5. BISER FF's structure

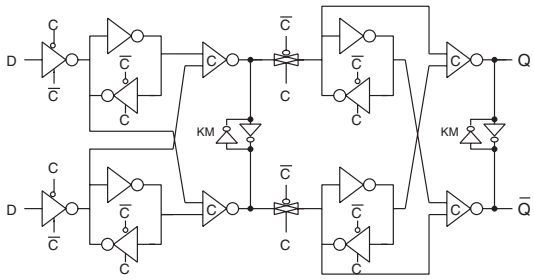

Fig. 6. BCDMR FF's structure

pared to twin well in a 65-nm process by neutron irradiation. It is possible to eliminate upsets from soft errors by enhancing circuit structures which utilizes these bipolar effects [4].

III. 2D Device-level simulation results

Fig. 4 shows a double-height cell structure [7] to prevent simultaneous flips on PMOS transistors in two latches by placing NMOS transistors between them. It is very robust to soft errors on PMOS regions by separating critical components. However, it is very weak to soft errors on NMOS regions. If both redundant latches stores the same value, they can be flipped at the same time by a particle hit. On the other hand, if both latches stores the opposite values, a particle hit with large amount of energy only will flips one of redundant latches. Thus the possibility of the redundant flip can be drastically reduced when both latches stores the opposite values.

Obviously, 3D device simulation is the best way to analyze the radiation tolerance of a latche in the double-height cell structure. However, it will take 30-40 hours to finish a 3D device-level simulation at which the simulation time is 0.2 ns. For getting the results quickly, we decide to chang the structure from double-height to single-height as shown in Fig. 7. Therefore, we can finish a 2D device simulation in 0.25-0.5 hours, which is almost 100x faster than the 3D simulation. Although the latch's structure is changed but the radiation tolerance of single-height structure is similar to the double-height one because the distance between NMOS of the inverters I0 and I1 is shorter than the distance between NMOS of the inverter I0 and the tristate inverter T1. It makes sure that the parasitic bipolar effect of NMOS in I1 is stronger than in T1 in both case. Thus we can get the same simulation results which use the single-height cell structure as use the double-height cell structure.

Fig. 8 shows a pair of redundant latches which store the same value in BISER or DICE FFs, while Fig. 9 shows of those which store the opposite values in BCDMR FFs [6]. By the way, BISER and BCDMR FF's structures are shown in Fig. 5 and 6.

Fig. 10 and show a device-level structure used in mixed-mode 2D device simulations. Fig. 11 shows a particle hit on the right-side of NMOS of I0. The distance between the two latches is 0.3μm, and the well-tap is palced 2.75μm far away from the right-side of T1. Fig. 12 and 13 represent the states of a pair of redundant latches according to the charge "Q" collected to N0 in which latches stores the same value as in Fig. 8 and the opposite values as in Fig. 9, respectively. We assume that a particle hit on the NMOS transistor of I0. The values of charge, Q_{critNx}, Q_{maxNx} denote the critical charge and the maximum charge of the Node x, respectively. The node x will flip when the charge value is between Q_{critNx} and Q_{maxNx} as shown in Fig. 2, however it can go back to its original value by parasitic bipolar effects if the charge value above the maximum charge (Q_{maxNx}) as shown in Fig. 3. Therefore, when two redundant latches stores the same value, they are flipped at the same time by charge between Q_{critN3} and Q_{maxN1} as shown in Fig. 12. On the other hand, when they store the opposite values, the vulnerable region disappeared as shown in Fig. 13. In that case, T1 is flipped also, but its critical charge is much more than I0 because of its poor drivability. Therefore, there is no region in which both redundant latches are flipped at the same time. The charge values are also plotted in Fig. 12 and 13, which are obtained from 2D device-level simulation.

Fig. 14 and 15 show transient voltage waveforms obtained from device-level simulations when a particle hits with LET=0.3 pC/μm and 1 pC/μm on the latches storing the same value. The node N1 flips at LET=0.3 pC/μm and goes back to its original state at LET=1

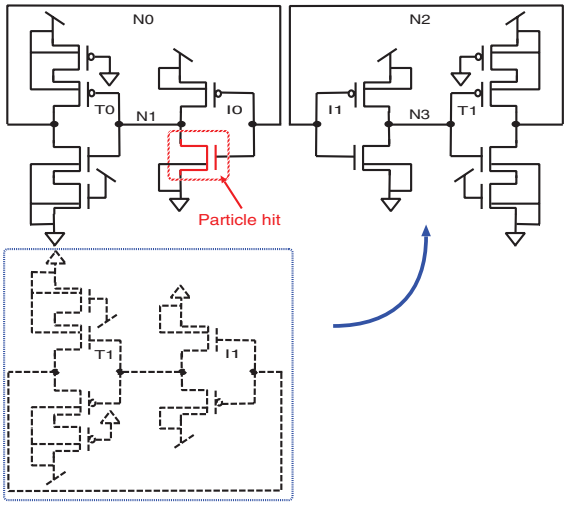

Fig. 7. How to modify a 3D structure constructed by two rows to a 2D structure in a single row.

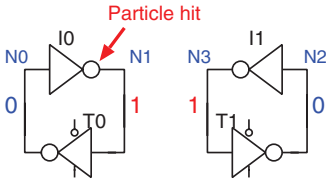

Fig. 8. Two redundant latches of storing the same value

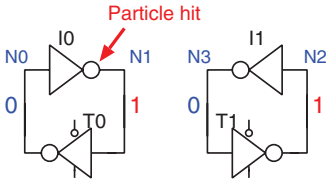

Fig. 9. Two redundant latches of storing the opposite value

pC/μm, while N3 is fliped in the both cases.

On the other hand, Fig. 16 and 17 show transient voltage waveforms obtained when a particle hits with LET=0.3 pC/μm and 1 pC/μm on the latches storing the opposite value. The node N1 flips at LET=0.3 pC/μm and goes back to its original state at LET=1 pC/μm, while N3 does not flip in the both cases.

IV. Conclusion

We introduce a structure of redundant FFs which is robust to MCUs by utilizing the parasitic bipolar effect. Redundant FFs storing the same value are very sensitive to MCUs induced by the parasitic bipolar effect, while those storing the opposite values are not sensitive to MCUs. Device-level simulations results also prove that the parasitic bipolar effects can decrease the number of MCUs.

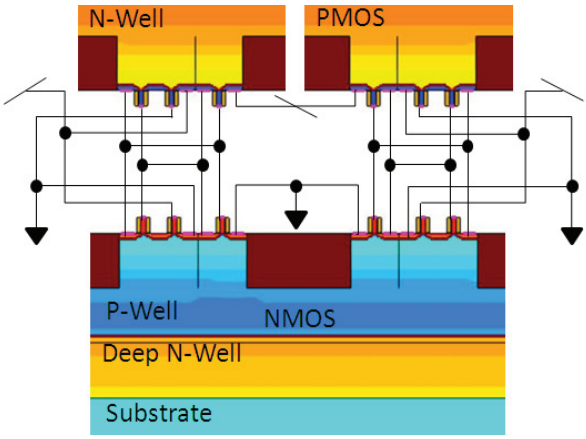

Fig. 10. 2D device-level structure

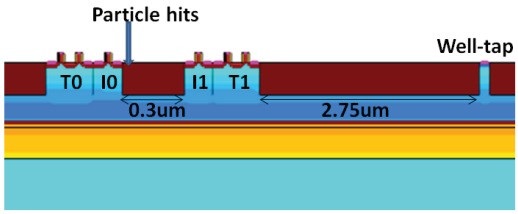

Fig. 11. particle hits on right-side of NMOS of I0

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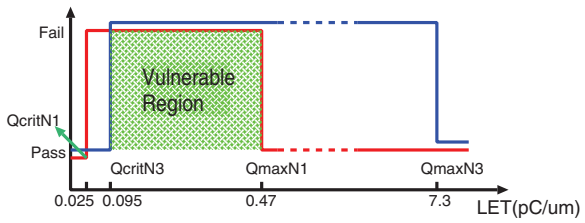

Fig. 12. Pass and Fail status by paticle energy when storing the same value

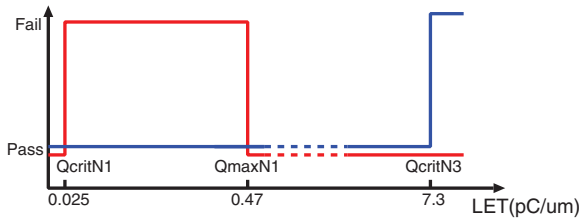

Fig. 13. Pass and Fail status by paticle energy when storing the opposite value

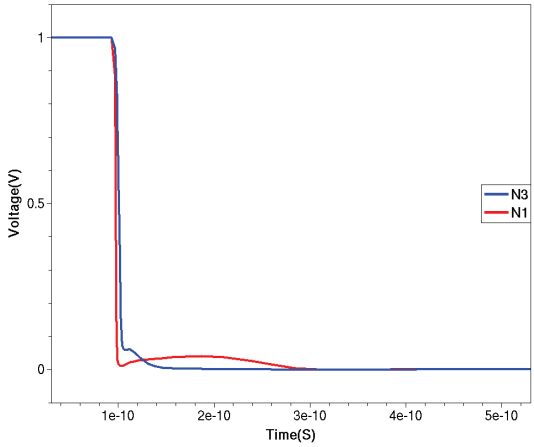

Fig. 14. Transient waveforms by device simulation when both latches stores the same value with LET=0.3 pC/μm

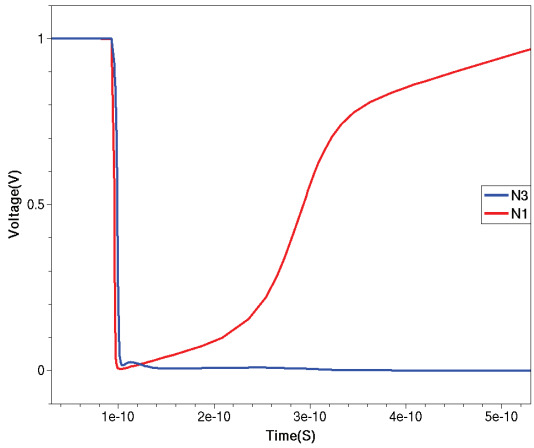

Fig. 15. Transient waveforms by device simulation when both latches stores the same value with LET=1 pC/μm

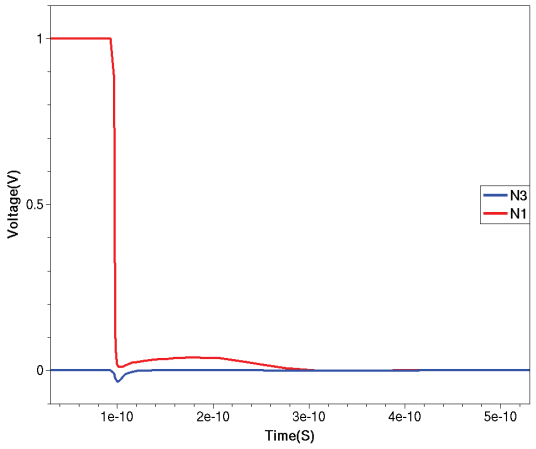

Fig. 16. Transient waveforms by device simulation when both latches stores the opposite value with LET=0.3 pC/μm

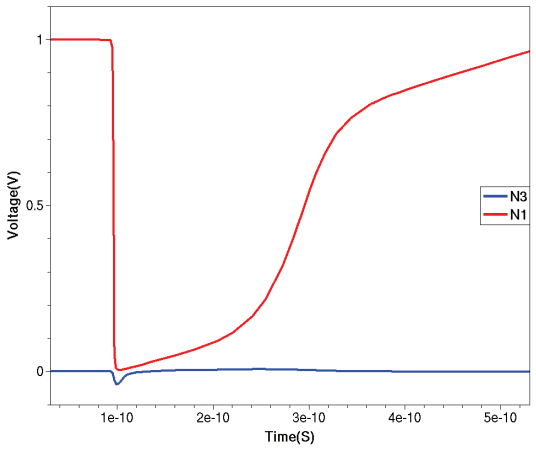

Fig. 17. Transient waveforms by device simulation when both latches stores the opposite value with LET=1 pC/μm