Circuit performance degradation on FPGAs considering NBTI and process variations

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Abstract— LSI scaling causes the reliability problem. It is important to analyze the degradation of Negative Bias Temperature Instability(NBTI) in circuit designs. Yield is affected by variations. In the near future, NBTI and variations will decrease reliability on FPGAs fabricated in a nanometer process. In this work, we show the effect of NBTI and variations on 65nm FPGAs. According to our results, cicuit design margin can be reduced.

I. Introduction

Negative Bias Temperature Instability(NBTI) was first reported in 1967 [1]. NBTI is a well-known LSI degradation as well as Hot Carrier Injection(HCI), Time Dependant Dielectric Breakdown(TDDB). Threshold voltage(V_{th}) of PMOS increases with time caused by negative bias voltage. Which is called stress condition. Recently, NBTI is known as one of the dominant factors that determine the life time of circuit [2]. NBTI degradation depends on temperature, supply voltage, frequency and device parameters. NBTI recoveries when negative bias moves away(Fig. 1). Which is called relax condition. NBTI degradation includes recoverable part and permanent part. According to latest work, they have various origins. Because of recovery of degradation, it is difficult to measure NBTI for modeling it. Several measurement methods are proposed in [3] [4] [5]. Some NBTI models are suggested in [6] [7]. An accurate NBTI model is still disscused, because it critically depends on the performance situation and process node. Positive Bias Temperature Instability(PBTI) occurs in NMOS device. V_{th} of NMOS increases with time caused by positive bias voltage. PBTI is supposed a particular note at after 40nm process using hi-k. It is ignorable at 65nm process because its effect appears much later than NBTI.

Variations became remarkable defects at after 90nm process. It is the phenomenon that fluctuate V_{th} caused by doping substances and accuracy. V_{th} of MOS devices follows the gauss distribution. We call center typical, upper 3σ slow and lower 3σ fast. It is considered when architects design layouts and schematics.

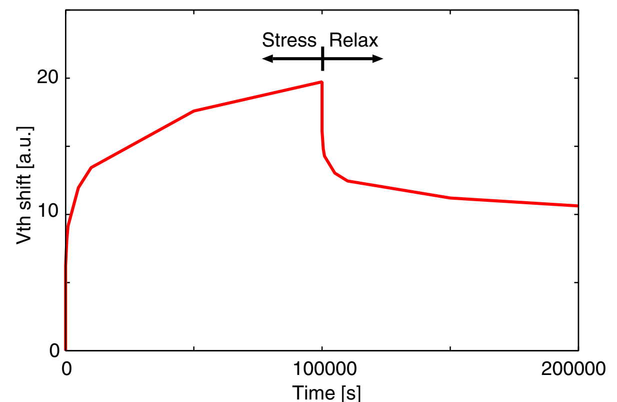

Fig. 1. NBTI Degradation and Recovery Model

In this work, we evaluate NBTI effect on the circuit to use proposed model. We analyse two kind of circuits, the ring oscillator(ROSC)s of the inverter gate and the circuit elements of FPGAs. ROSCs are widely known general circuits. We evaluate delay degradation of the aging ROSCs. Recent years, performance of FPGAs is becoming comparable to that of Application Specific Integrated Circuit(ASIC). Domain of using FPGA is expected to become huge. FPGA has many good features, short development period, inexpensive development cost, and easy designing. Vendors can produce FPGAs with the latest process. But some problems, such as variations, are exposed at scaling process. It is important for investigating how NBTI affects circuit to consider variation effect. We evaluate delay degradation of the aging circuit elements of FPGAs.

First of all, related works are introduced on section II. Experimental methodology and NBTI model are explained on section III. We show the result from simulation experiments on section IV. We discuss results on section V. And the conclusion is on section VI.

II. Related Work

NBTI degradation effects on some of circuit elements of FPGAs are discussed in [8]. They propose Relaxing Bitstream Technique to gain back lost stability and performance. A survey paper about reliability in FPGAs [9], explaines various faults and detection/repair methods. The latest paper of NBTI on FPGAs [10], also considers HCI and evaluate both DC and AC NBTI effects. They suggest that NBTI and variations are related each other in [11–13]. But they do not evaluate circuit performance degradation, only V_{th} degradation models are proposed.

III. NBTI considering variations

In this section, we explain our experimental methodology. There are many models which show how NBTI or variations affect PMOS V_{th}. We apply V_{th} degradation(ΔV_{th}) calculated by those models to circuit netlists. NBTI degradation models considering recovery effect were proposed by [14] [15]. We use the approximation formule, Eq. (1, 2) proposed by [16].

$$\Delta V_{\mathrm{th,stress}} = A \times t^n \tag{1}$$

$$\Delta V_{\mathrm{th,relax}} = \Delta V_{\mathrm{th0}}(1 - B \times \log(t - t_0)) \tag{2}$$

Eq. (1, 2) are degradation amount of V_{th} at stress and relax conditions respectively. Parameters A and B are determined as follows. In that case, it will degradate by 10% after 10 years continuous stress. We assume V_{th} will degradate by 8.9% after 5 years continuous stress. While it will recover by 3% after 5 years continuous relaxation. NBTI under stress continuous is called static NBTI. NBTI alternating between stress and relax is called dynamic NBTI. Dynamic NBTI degradation is fluctuated by frequency and duty cycle. We ignore frequency dependancy since degradation is almost constant above 10kHz clock frequency [16]. We assume that duty cycle is 0.5. n is time exponent. t_0 is total stress time. Static and dynamic NBTI degradation models are shown in Fig. 2. It is based on parameters of a 65nm process typical PMOS device.

We use three parameter sets of variations, typical(TT), slow(SS) or fast(FF). We propose two methods considering both NBTI and variations. First, each variations have constant degradation amount calculated using Eq. (1, 2). Parameters assumed are in Table I. We call it Constant Degradation Model(CDM). Under NBTI effect, fast PMOS devices degrade much faster than slow PMOS devices [7]. So we assume degradation as in Table II. We call it Variation Degradation Model(VDM). V_{th} calculated by those models are shown on Fig. 3. In Fig. 3, cd_S and cd_F are calculated by CDM, vd_S and vd_F are calculated by VDM. We use those two methods to evaluate circuit performance degradation. V_{th} changes linealy with one of device parameters, V_{TH0} [17].

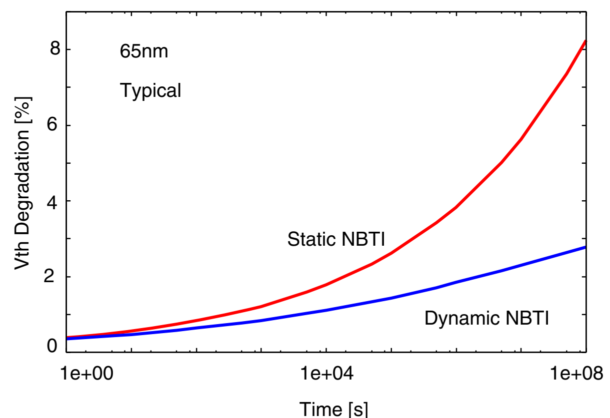

Fig. 2. Static and Dynamic NBTI Degradation Models

TABLE I
Degradation models of NBTI not considering variations

Type	INIT	Static Deg./dec.	Dynamic Deg./dec.
SS	1.08	10%	3%
TT	1	10%	3%
FF	0.92	10%	3%

IV. Result

In this section, we show the results of predictive degradation of two kinds of circuits, the ROSCs of the inverter gates and the circuit elements of FPGAs. We explain the circuits and results.

A. NBTI on Ring Oscillators of the Inverter Gates

We evaluate frequency degradation of the ROSCs of the inverter gates. The ROSCs are the circuit that connect odd number invertors in series. The simulation circuit is shown in Fig. 4. It includes 5 CMOS inverters chain and 4 fanout CMOS inverters for each of them. We call it 5ROSC. The 5ROSC's frequency is about 2.6GHz at $t = 0$, typical variations.

We evaluate frequency degradation affected by dynamic NBTI on three types of variation, TT, SS and FF. We use the two models explained in section III. All of PMOS devices have the same V_{th0} value in one netlist. The result is shown on Fig. 5. In Fig. 5, cd_F and cd_S are simulated

TABLE II
Degradation models of NBTI considering variations

Type	INIT	Static Deg./dec.	Dynamic Deg./dec.
SS	1.08	3%	1%
TT	1	10%	3%
FF	0.92	30%	9%

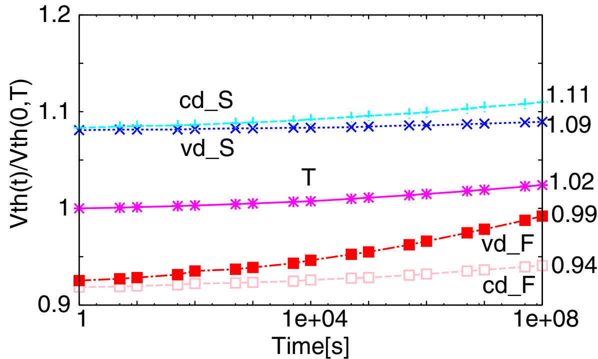

Fig. 3. Comparing two methods of $V_{\rm th}$ degradation

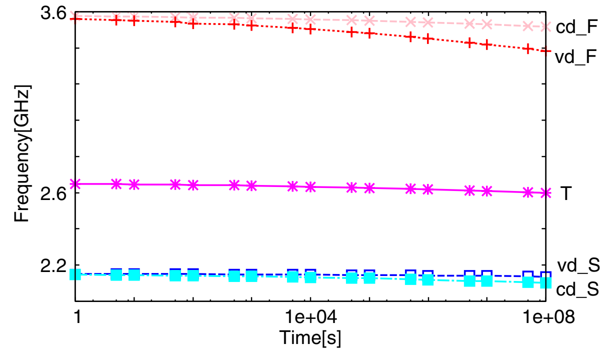

Fig. 5. Frequency Degradation on Dynamic NBTI in 5ROSC

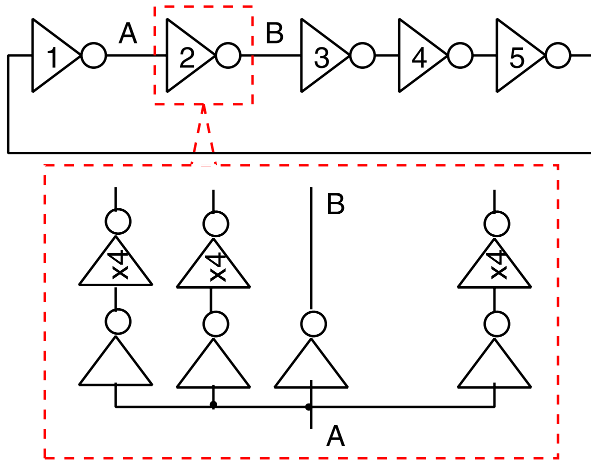

Fig. 4. 5 Stage Ring Oscillator

with CDM, vd_F and vd_S are simulated with VDM. Frequency of fast PMOS devices decreases 2% for 10^8s.

B. NBTI on FPGAs

We focus on the circuits including PMOS devices called level restorer on FPGAs. We evaluate fall delay time($T_{\rm df}$) degradation of level restorer circuit. The simulation circuit is shown in Fig. 6. It consists of two inverters(INV1 and INV2) connected through an NMOS path transistor(MNP) and a level restorer PMOS(MLR). MLR can prevent INV2 from floating. Circuit fan-out is four. We assume input voltage rising in 1ns and falling in 1ns. Ae adjust MLR width for $T_{\rm df} = T_{\rm dr}$ at typical vatiations.

We evaluate $T_{\rm df}$ degradation affected by dynamic NBTI on three types of variation, TT, SS, FF. We use the two models explained in section III. All of PMOS devices are applied the same $V_{\rm th0}$ value in one netlist. The results are shown in Fig. 7, 8, 9. In Fig. 8, 9, cd_ are simulated with CDM, and vd_ are simulated with VDM. At $t = 0$ typical $T_{\rm df}$ is about 0.16ns, slow $T_{\rm df}$ is about 0.24ns, fast $T_{\rm df}$ is about 0.83ns.

V. Discussion

We propose the Variation Degradation Model cinsiderinf fast PMOS devices are the most sensitive to NBTI [7]. Fig. 5, 9 show that fast PMOS devices cause higher performance degradation than the other two variations. Fast PMOS devices are not dominant factors determining the critical path delay. Circuit design margins do not care about degraded fast PMOS. On the other hand, slow PMOS devices determining the critical path delay are robust for NBTI. Circuit performance is not affected by slow PMOS degradations. According to this, we are be able to reduce circuit design margin from the conventional pessimistic value.

VI. Conclusion

In this work, we evaluate circuit performance degradation affected by NBTI and variations. Frequency of 5ROSCs decreases 2% on dynamic NBTI for 10^8s. Performance of circuits consisting of fast PMOS devices is sensitive about NBTI effect. $T_{\rm df}$ of level restorer circuits increase 3% on dynamic NBTI for 10^8s. Level restorer circuits are weak as much as 5ROSCs for NBTI. According to our results, circuit design margin can be reduced.

Acknowledgements

This work is supported by VLSI Design and Education Center(VDEC), the University of Tokyo in collaboration with Synopsys, Inc, Cadence Design Systems, STARC, e-Shuttle, Inc. and Fujitsu Ltd.

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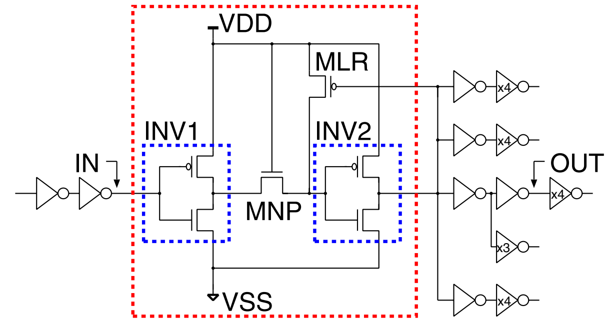

Fig. 6. Level Restorer Circuit on FPGAs

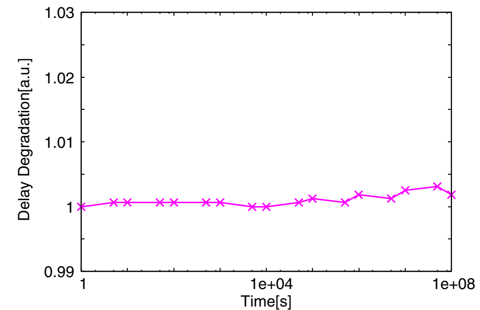

Fig. 7. Typical Variation, T_{df} Degradation on Dynamic NBTI in Level Restorer Circuit

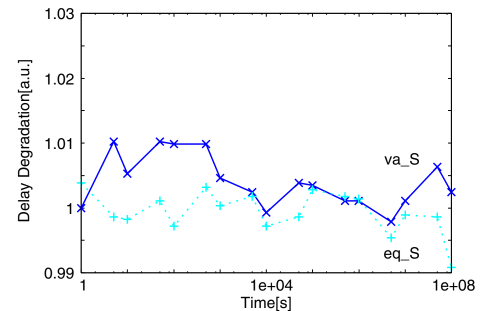

Fig. 8. Slow Variations, T_{df} Degradation on Dynamic NBTI in Level Restorer Circuit

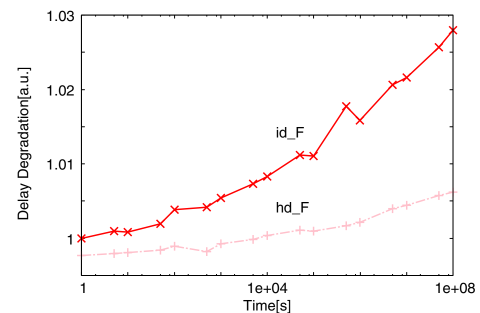

Fig. 9. Fast Variations, T_{df} Degradation on Dynamic NBTI in Level Restorer Circuit