Soft Error Tolerance of Standard and Stacked Latches Dependending on Substrate Bias in a FDSOI Process Evaluated by Device Simulation

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***Abstract*— Soft error tolerance in a thin BOX FDSOI process depends on substrate bias because soft errors are mainly caused by the parasitic bipolar effect (PBE). Substrate-bias dependence of soft error tolerance is evaluated by changing thickness of a BOX layer by device simulations. We compare the soft error tolerance between standard and stacked flip-flops (FFs). At 10 nm BOX thickness, soft error tolerance of both FFs greatly change by body bias. But at 100 nm BOX thickness, soft error tolerance of standard FF is stable but that of the stacked FF is not stable. The BOX thickness has a large impact on the PBE by the substrate bias.**

I. Introduction

The radiation-induced soft error becomes a serious reliability issue in high performance devices for mission critical applications. Storage elements such as flip flops (FFs) or latches must be protected from soft errors on reliable applications for terrestrial region and outer space.

For a device-level radiation-hardened technology, fully-depleted silicon on insulator (FDSOI) is strong against soft errors [1], [2]. In FDSOI a buried oxide (BOX) layer is formed between substrate and transistor regions. The BOX layer prevents charge collection generated by drift and funneling from substrate. The structure with a 10-25 nm thin BOX layer (T_{BOX}) is called thin BOX FDSOI [3], [4]. Charge collection directly cause soft error in bulk devices, while in FDSOI the parasitic bipolar effect (PBE) is a dominant factor to cause soft error [5]. Figure 1 shows how electron-hole pairs are generated in diffusion and collected to channel. PBE turns on the parasitic bipolar transistor under the channel to turn on the MOSFET. Because a substrate bias affects PBE, soft error tolerance depends on substrate voltage in FDSOI. In this paper, we discuss radiation hardness of a standard FF and an FF with stacking structure. The stacking structure consists of two series-connected (stacked) transistors. Stacking transistors is effective to reduce soft error rates in FDSOI. We evaluate soft error tolerance by changing substrate bias in various BOX thicknesses.

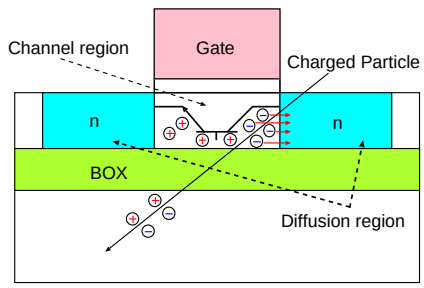
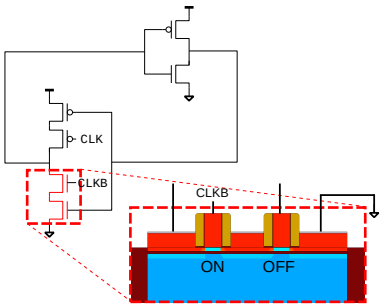
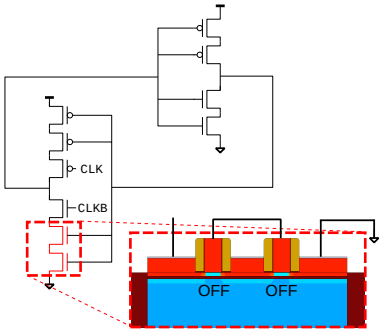


Fig. 1. Holes generated in the diffusion region are collected in the channel region and then the drain-body-source parasitic bipolar transistor turns on.



(a) Standard clocked latch



(b) Stacked clocked latch

Fig. 2. Schematic diagram and the cross-sectional view of the 3D model used for device simulations.

This paper is organized as follows. Section II shows device simulation setups in a 65 nm thin BOX FDSOI process. In Section III, device simulation results are shown. In Section IV, diffusions about the difference of mechanism of soft error. Finally, we describe the impact of BOX thickness to soft error tolerance in the thin BOX FDSOI.

II. Simulation Setup

We use a 65 nm thin BOX FDSOI 3D transistor model calibrated by SPICE models extracted from fabricated devices as in [6]. Figure 2 shows cross-sectional views of NMOS transistors and the schematic diagrams of a standard clocked latch and a stacked clocked latch. Stacked latch is strong against soft errors because of its stacked (clocked) structure. Even if one of the stacked transistors turn on, the other still turns off. The possibility of simultaneous turn on both of the stacked transistors is very small since they are isolated by the BOX layer.

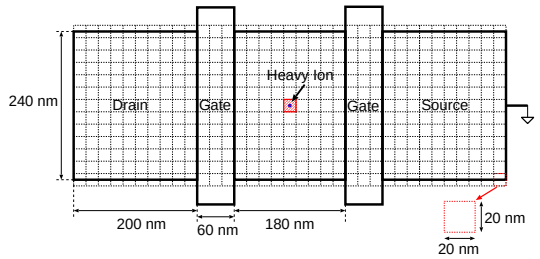


Fig. 3. Simulation setup to evaluate sensitive areas induced by a heavy ion with LET of 15.8 MeV-cm^2/mg. The heavy ion strikes at the center of each grid.

TABLE I

THRESHOLD LET FROM DEVICE SIMULATIONS.

Substrate Bias	Threshold LET [MeV-cm^2/mg]			
	T_{BOX} = 10 nm		T_{BOX} = 100 nm	
	Standard	Stacked	Standard	Stacked
0.5 V	4.0	12.5	2.9	10.4
0 V	6.1	13.2	3.1	11.7
−0.5 V	11.3	16.6	3.0	11.8

The two stacked transistors in the red-dot rectangles are modeled in the device level and the other transistors are in the SPICE level to reduce simulation times with keeping accuracy. Supply voltage is fixed to 0.8 V and substrate bias (V_{sub}) is swept from 0.5 V to −0.5 V only on the 3D structure to compare soft error tolerance. We evaluate soft error tolerance in terms of CS (Cross section) and threshold LET (linear energy transfer). When evaluating CS, the LET value is 15.8 MeV-cm^2/mg which is almost same as the LET of secondary ions generated by a high-energy neutron hit to an Si atom. In order to evaluate CS, heavy ions are irradiated at the center of every 20 nm grid as shown in Fig. 3. In order to evaluate the threshold LET, heavy ions are irradiated at the weakest point of each structure. In the standard latch, a heavy ion penetrates the gate terminal of one of the two off-state transistors. In the stacked latch, it goes through between the gate terminals of the off-state stacked transistors. Track radius of the heavy ion ($\mathrm{r_t}$) is expressed by (1) from [7]. Evaluating the impact of the BOX thickness on soft error tolerance, BOX thickness is swept from 10 nm to 100 nm.

$$\mathrm{r_t} = 7.16765 \times 10^{-3} \times \sqrt{\mathrm{LET}} \quad (1)$$

III. Simulation Results

Table I shows the device simulation results of threshold LET. It is increased as the substrate bias goes down on both of the standard and stacked latches at the 10 nm BOX thickness. On the contrary at 100 nm, the threshold LET of the standard latch is almost constant, while threshold LET of the stacked latch increases by decreasing body bias. Figures 4 and 5 show CS by Ar irradiation. As the substrate bias goes down, CS also decreases. In the stacked latch at 10 nm BOX thickness, CS disappears. Soft error tolerance becomes better by lowering the substrate bias at T_{BOX} = 10 nm. The stack structure has higher soft error tolerance than the standard structure. LET and CS of the stacked structure are 1.47x and 0.19x of the standard structure respectively. When the substrate bias changes from 0.5 V to −0.5 V in both structures at T_{BOX} = 10 nm, the threshold LET and CS

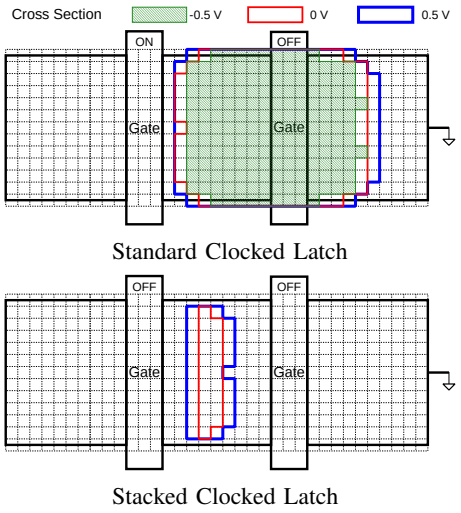


Fig. 4. Transision of cross section at BOX thickness = 10 nm.

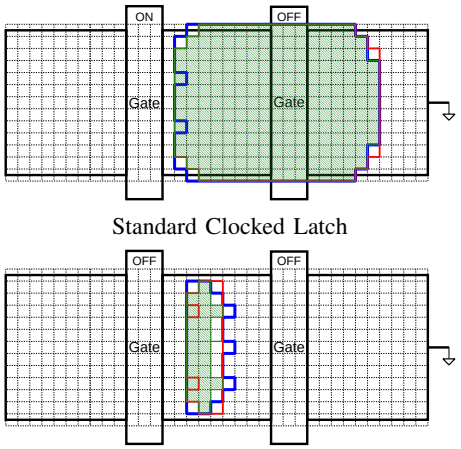


Fig. 5. Transision of cross section at BOX thickness = 100 nm.

TABLE II

CROSS SECTION BY AR IRRADIATION.

Substrate Bias	Cross Section [cm^2/ion]			
	T_{BOX} = 10 nm		T_{BOX} = 100 nm	
	Standard	Stacked	Standard	Stacked
0.5 V	8.52×10^{-10}	1.64×10^{-10}	8.36×10^{-10}	1.36×10^{-10}
0 V	7.88×10^{-10}	0.8×10^{-10}	8.36×10^{-10}	1.16×10^{-10}
−0.5 V	6.96×10^{-10}	0	8.28×10^{-10}	0.92×10^{-10}

are changed by the substrate bias. In the standard latch at T_{BOX} = 100 nm, the threshold LET increases only by 3.3% and CS decreases by 1.0%. However in the stacked latch, as the BOX layer becomes thick, soft error tolerance of the stacked latch changes more drastically by substrate bias more than that of the standard latch. Substrate bias on soft error tolerance does not have a big impact at any BOX thickness. The soft error tolerance decreases as the BOX layer becomes thicker. This is because the potential of the channel region becomes lower as the BOX layer becomes thicker.

IV. Discussions

In the standard structure with a BOX layer of 10 nm, 6.1 MeV-cm^2/mg heavy ions are irradiated to the irradiation point 1 in Fig. 6 by sweeping substrate bias. Note that the LET of 6.1 MeV-cm^2/mg is the threshold LET when the V_{sub} = 0 V as shown in Table I. Figure 7 shows the output

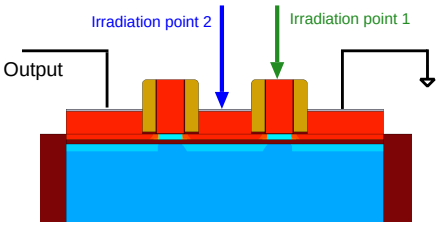


Fig. 6. In the standard structure, a heavy ion is irradiated to point 1 to compare the substrate bias dependence. When comparing the difference between the standard and the stack structure, irradiate point moves to 2.

current for the three substrate bias of −0.5 V, 0 V and 0.5 V. By increasing the substrate bias, the peak current increases but the current falls to 0 earlier. As can be seen from Table I, at $V_{\rm sub}$ = −0.5 V, the heavy ion with the LET of 6.1 MeV-cm^2/mg is over the threshold LET of 4.0, while at $V_{\rm sub}$ = 0.5V, it is under threshold LET of 11.3. The higher current peaks just after the heavy ion hit at 200 ps are mainly caused by charge collection, but the current tails after the peaks are mainly caused by PBE. The above different factors to cause soft errors lead to the different dependency to substrate bias of the standard and stacked latches discussed in the following paragraph.

In order to compare the stack and standard latches at $V_{\rm sub}$ = −0.5 V, 15.8 MeV-cm^2/mg heavy ions are irradiated to the irradiation point 2 in Fig. 6. Figure 8 shows two current waveforms at the output nodes. In the standard latch, the output current is mainly generated by charge collection since the current peak instantly goes down. On the other hand, the output current of the stacked latch has lower peaks and keeps to flow even at 400 ps. It clearly shows in the stacked latch current by a heavy ion hit is mainly from PBE instead of charge collection since both of the stacked transistors are in off state as shown in Fig. 2. After discharging the intermediate node between the stacked transistors, the electric field between substrate and the diffusion between them disappears. Then no charge collection occurs and PBE becomes dominant. In the standard latch, however, one of the stacked transistors is in on state as shown in Fig. 2. Until the output node is flipped, the electric field between substrate and the diffusion of the output node remains and collect carriers by the charge collection.

V. Conclusion

In order to evaluate the impact of substrate bias to soft error tolerance, device simulations are conducted to sweep substrate bias and BOX thickness. The stacked latch is better in terms of soft error tolerance than the standard latch at any substrate bias and BOX thickness. The stack structure has 1.47x larger threshold LET and 0.2x smaller CS than the standard latch at $V_{\rm sub}$ = 0 V with 10 nm BOX thickness. But in the standard latch with 100 nm BOX layer, soft error tolerance becomes flat at substrate bias. In the stacked latch, however, substrate bias affects soft error tolerance at any BOX thickness since PBE is a dominant factor to cause soft errors instead of charge collection. On the other hand, soft error is caused by only PBE in the stacked latch. The device simulation results clearly shows the dominant factors

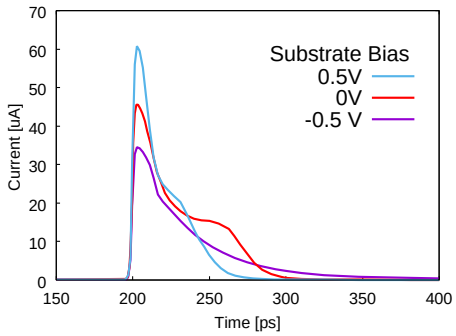


Fig. 7. Output current by substrate bias.

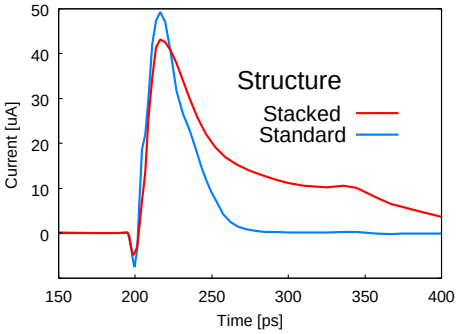


Fig. 8. Output current by structures of latches.

in the stacked latch and the standard latch. By increasing the thickness of the BOX layer, the soft error tolerance of the standard latch becomes insensitive to substrate bias. On the contrary, the stacked latch is still sensitive to body bias at the 100 nm BOX thickness. The thickness of the BOX layer is one of key parameters for soft error tolerance in the stacked structure which has more soft error immunity than the standard nonstacked structure.

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References

[1] P. E. Dodd, M. R. Shaneyfelt, K. M. Horn, D. S. Walsh, G. L. Hash, T. A. Hill, B. L. Draper, J. R. Schwank, F. W. Sexton, and P. S. Winokur. SEU-sensitive volumes in bulk and SOI SRAMs from first-principles calculations and experiments. *IEEE Trans. Nucl. Sci.*, 48(6):1893–1903, December 2001.

[2] K. Hirose, H. Saito, Y. Kuroda, S. Ishii, Y. Fukuoka, and D. Takahashi. SEU resistance in advanced SOI-SRAMs fabricated by commercial technology using a rad-hard circuit design. *IEEE Trans. Nucl. Sci.*, 49(6):2965–2968, December 2002.

[3] Y. Morita, R. Tsuchiya, T. Ishigaki, N. Sugii, T. Iwamatsu, T. Ipposhi, H. Oda, Y. Inoue, K. Torii, and S. Kimura. Smallest vth variability achieved by intrinsic silicon on thin box (sotb) cmos with single metal gate. In *VLSI Tech. Symp.*, pages 166–167, June 2008.

[4] P. Roche, J. Autran, G. Gasiot, and D. Munteanu. Technology downscaling worsening radiation effects in bulk: Soi to the rescue. In *2013 IEEE International Electron Devices Meeting*, pages 31.1.1–31.1.4, Dec 2013.

[5] M. Raine, M. Gaillardin, T. Lagutere, O. Duhamel, and P. Paillet. Estimation of the single-event upset sensitivity of advanced SOI SRAMs. *IEEE Trans. Nucl. Sci.*, 65(1):339–345, January 2018.

[6] K. Yamada, H. Maruoka, J. Furuta, and K. Kobayashi. Radiation-hardened flip-flops with low-delay overhead using pmos pass-transistors to suppress set pulses in a 65-nm fdsoi process. *IEEE Transactions on Nuclear Science*, 65(8):1814–1822, Aug 2018.

[7] K. Warren, L. Massengill, R. Schrimpf, and H. Barnaby. Analysis of the influence of mos device geometry on predicted seu cross sections. *IEEE Transactions on Nuclear Science*, 46(6):1363–1369, Dec 1999.