Radiation-Hardened Flip-Flops with Small Area and Delay Overheads Using Guard-Gates in FDSOI Processes

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***Abstract*— In this paper we propose radiation-hardened flip-flops (FFs) with small area and short delay overheads in a 65 nm fully depleted silicon on insulator (FDSOI) process. We designed two FFs composed of a guard-gate to eliminate SET pulses in the latch. Although the number of additional transistors is only two, one of the proposed FFs has high soft error tolerance at CLK = 1. Although the number of additional transistors is six, the other has high soft error tolerance at CLK = 0 and 1. We evaluated the radiation hardness of the newly designed structure by device simulations. Simulation results show that the stored values of the proposed FFs are not upset even though a charged particle with LET of 60 MeV-cm^2/mghits.**

I. Introduction

According to process scaling, soft errors become a significant issue to threaten the reliability of a semiconductor chip since a stored value in strage elements such as flip-flops or SRAMs is flipped. When a radiated particle hits transistors, electron-hole pairs are generated in Si and collected at the drain region of transistors. The resulting perturbation in the output node voltage is called a single event transient (SET) pulse. A SET pulse will cause a soft error described as single event upset (SEU). To improve the tolerance of flip-flops (FFs) against soft errors, several redundant FFs such as triple modular redundancy (TMR) [1] have been proposed for effective countermeasures. However, they have longer delay time and larger area, power consumption than conventional FFs. Fully depleted silicon on insulator (FDSOI) processes have higher tolerance for soft errors than a conventional bulk process without any performance overhead, because the buried oxide (BOX) layer prevents charge from being collected from substrate [2]. In this paper, we propose radiation-hardened FFs with small area and delay overheads in a 65 nm FDSOI process.

II. Radiation-Hardened Flip-Flops

Fig. 1 shows a conventional DFF called the transmission gate FF (TGFF). It has no tolerance against soft errors.

A. Conventional Radiation Hardened Flip-Flop

The guard-gate is an inverter with two inputs and one output as shown in Fig. 2 [3]. The signal coming to one of the inputs is delayed using two inverters. The guard-gate eliminates all SET pulses which are shorter than the delay of two inverters since it has the one input delayed by two inverters. Moreover, the guard-gate has the stacked structure [4]. Stacked structure in FDSOI is isolated by the BOX layer. When a radiated particle hits on one transistor in the stacked structure, its output does not flip unless both transistors upset at the same time as shown in Fig. 3. Thus, the guard-gate has high soft-error tolerance.

Figure 4 shows guard-gate FF (GGFF) [5]. The master latch (ML) and the slave latch (SL) contain the guard-gates. GGFF has about 100x stronger against SEU than DFF in a 16 nm bulk FinFET processes. However, it has larger area and delay overheads than conventional FFs because it has 12 more transistors than TGFF.

B. Proposed Radiation-Hardened Flip-Flop

In Fig. 5, the proposed FF named the feedback recovery FF (FRFF) is shown. The guard-gate in FRFF is composed of the ML and the SL as shown in Fig. 6. Although the number of additional transistors is only two, FRFF has high soft error tolerance at CLK = 1. In Fig. 7, the proposed FF named the dual FRFF (DFRFF) is shown. DFRFF has two guard-gates. One guard-gate is implemented with the ML and the SL at CLK = 1 as like FRFF. The other is composed of the SL and the output inverter at CLK = 0. DFRFF has higher soft error tolerance than FRFF by adding two transistors.

III. Simulation Results and Discussions

A. Soft-error Tolerance of Proposed FFs

We evaluate soft-error tolerance of DFRFF by device simulations at CLK = 1. The device simulations are carried

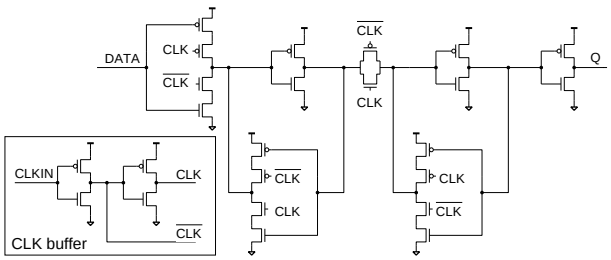


Fig. 1. Transmission-gate FF.

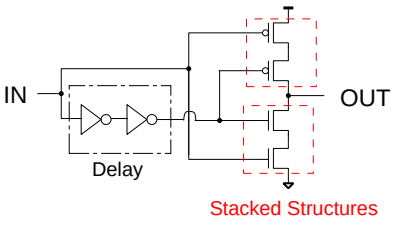


Fig. 2. Guard-Gate design.

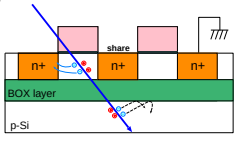


Fig. 3. Stacked structure.

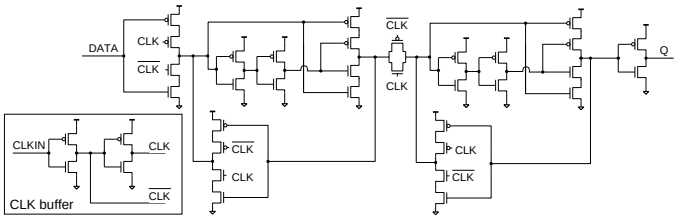


Fig. 4. Guard-Gate FF.

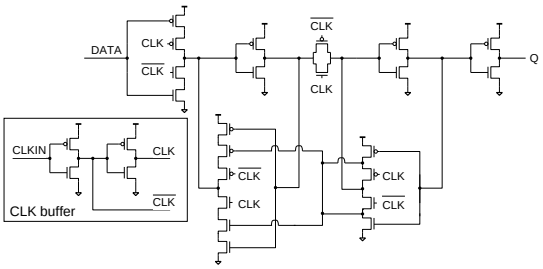


Fig. 5. Proposed Feedback Recovery FF.

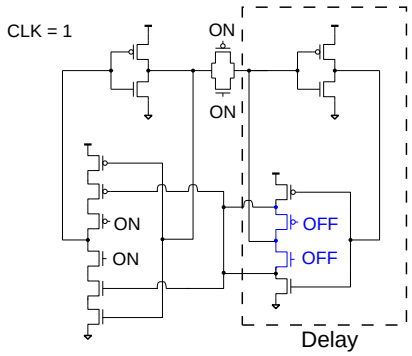


Fig. 6. Static condition of FRFF at CLK=1. Guard-gate in FRFF is composed of ML and SL.

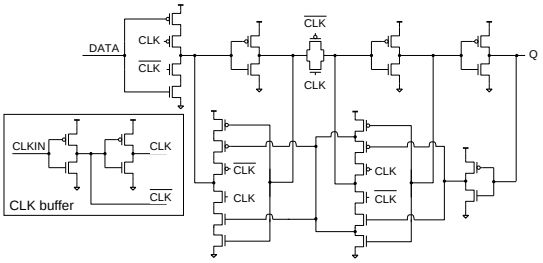


Fig. 7. Proposed Dual Feedback Recovery FF.

out using Sentauras from Synopsys. We constructed three-dimensional structures of an inverter in a 65 nm FDSOI process with a thin BOX layer for the device simulations. Figure 8 depicts the schematic and the cross section on device simulations of DFRFF at CLK = 1.

NMOS transistors are more vulnerable to particle hits than PMOS transistors [6]. Thus, we evaluate soft-error tolerance of DFRFF when a particle hits an NMOS transistor. By setting the initial value of N0 to 0 V at CLK = 1, a particle

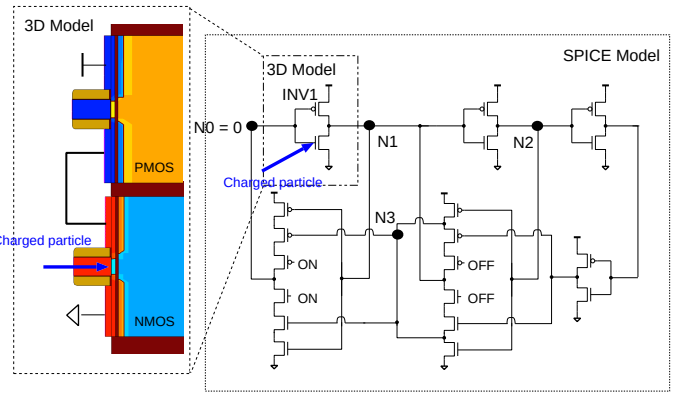


Fig. 8. Schematic and cross section on device simulations of ML. By setting the initial value of N0 to 0 V, a heavy ion hits at the NMOS transistor at V_{DD} =1.2 V and 0.6 V.

with liner energy transfer (LET) of 60 MeV-cm^2/mg hits at the NMOS transistor in INV1 as shown in Fig. 8. FFs have enough soft error tolerance in outer space if 60 MeV-cm^2/mg particles do not cause any SEU. It is because particles with higher energy than 60 MeV-cm^2/mg is much less than those below 60 MeV-cm^2/mg in outer space [7].

Figures 9 (a), (b) show simulation results at the supply voltage (V_{DD}) = 1.2 V and 0.6 V respectively. The stored value of DFRFF does not upset as shown in Fig. 9, even though a particle has LET of 60 MeV-cm^2/mg which is 10x larger than the threshold LET of the conventional latch. N1, N2 and N3 are influenced by a charged particle hit at V_{DD} = 1.2 V, but the amplitude of the SET pulse on N0 is attenuated to 0. In addition, only N1 and N2 are influenced by a charged particle at V_{DD} = 0.6 V, because the delay time of two inverters at V_{DD} = 0.6 V is 5.5x longer than that at V_{DD} = 1.2 V.

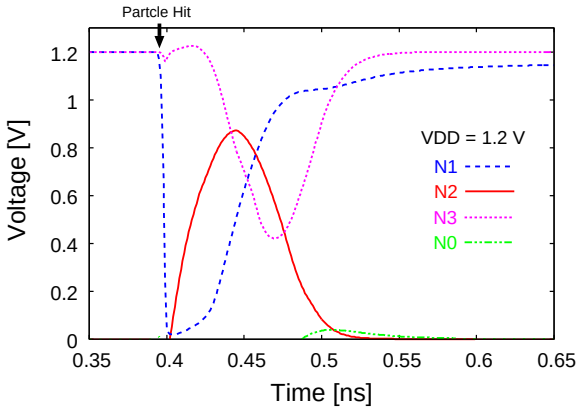
These results prove that the proposed FFs have a high and enough resilience to soft-error to make them appropriate for highly reliable devices in outer space.

B. Circuit Performance

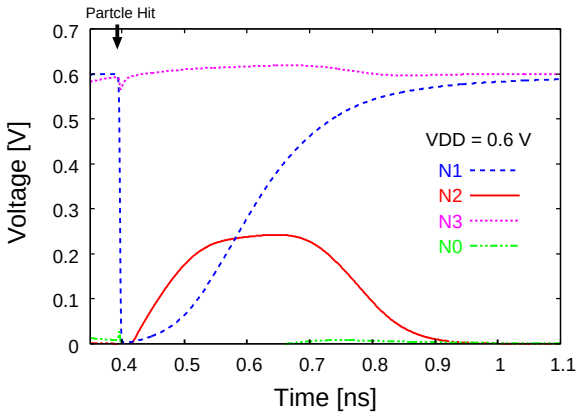
We measure delay time and power consumption of FFs using SPICE simulations at V_{DD}= 1.2 V. Table I indicates the simulation results of area, delay time, power at 10% data activity and the number of transistors. All values are normalized to those of TGFF. The values in parentheses are normalized to those of GGFF. The delay time and the area of GGFF are 2.2x longer and 1.4x bigger than that of TGFF, but the delay time and the area of FRFF are 52% shorter and 28% smaller than that of GGFF. FRFF also has less than 6% delay, area and power overheads than those of TGFF. The delay time and the area of DFRFF are 51% shorter and 20% smaller than those of GGFF. The power of the proposed FFs are most than 4% smaller than GGFF.

IV. Conclusion

We proposed two FFs which have soft-error resilience against a radiated particle with 60 MeV-cm^2/mg. The proposed FRFF with high soft-error tolerance only at CLK = 1 has 52% shorter delay time and 28% smaller area than the



(a) V_{DD} = 1.2 V



(b) V_{DD} = 0.6 V

Fig. 9. SEU simulation results at CLK=1. N1 and N2, N3 are influenced by a particle hit in Fig. 8. Stored value of ML in DFRFF is not upset up to LET = 60 MeV-cm^2/mg.

TABLE I

SIMULATION RESULTS OF AREA, D-Q DELAY, POWER AND NUMBER OF TRANSISTOR OF EACH FF AT V_{DD}= 1.2 V. ALL VALUES ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF GGFF.

FF	D-Q delay	Area	Power	# of Tr.
TGFF	1	1	1	24
GGFF	2.20 (1)	1.47 (1)	1.06 (1)	36
FRFF	1.06 (0.48)	1.06 (0.72)	1.03 (0.97)	26
DFRFF	1.08 (0.49)	1.18 (0.80)	1.02 (0.96)	30

GGFF. The proposed DFRFF with high soft-error tolerance at CLK = 0 and 1 has 51% shorter delay time and 20% smaller area than the GGFF.

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