Threshold Dependence of Soft-Errors induced by α particles and Heavy Ions on Flip Flops in a 65 nm Thin BOX FDSOI

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***Abstract*— IoT devices are usually driven by battery and are hard to be rebooted. Leakage current must be minimized by using high-threshold transistors. We evaluated soft-error tolerance depending on threshold voltage of transistors by α particle and heavy ion irradiation. Two chips are exposed, one is general purpose (GP) transistors and the other is low-power (LP) transistors in a 65 nm Fully-Depleted Silicon On Insulator (FDSOI) process. LPDFFs (DFFs with LP transistors) were 3051x stronger against soft errors than GPDFFs (DFFs with GP transistors) by α particle. There were a few errors on LPDFFs. The measurement results by heavy ions also reveal the average Cross-Sections (CSs) of the LPDFFs are 50% and 54% smaller than those of GPDFFs.**

I. Introduction

Reliability issues have become a significant concern due to soft errors with technology downscaling [1]. Temporal failures and aging degradation are two major concerns. Soft errors are one of temporal failures that flip stored values caused by radioactive particles such as α particles, neutrons and heavy ions. A flipped cell can be recovered by rebooting or rewriting. However, it is a serious issue especially for critical devices dealing with human life or social infrastructures. In the device-level, the Fully-Depleted Silicon On Insulator (FDSOI) structure can suppress soft errors. This structure prevents charge from being collected from substrate.

Semiconductor chips for low power must reduce leakage current. Low-power operation is mandatory for numerously-distributed internet of things (IoTs) driven by battery and hard to reboot. We evaluated the soft-error tolerance of two chips with general-purpose (GP, lower threshold) and low-power (LP, higher threshold) transistors.

Section Ⅱ explains the related works. Section Ⅲ explains the experimental setup. We explain the measurement results of GP and LP chips by α particle and heavy ions irradiation in Sect. Ⅳ. We conclude this paper in Sect. Ⅴ.

II. Related Works

In [2], the soft-error tolerance of flip-flops (FFs) with low, standard and high threshold transistors of a 28 nm bulk process were evaluated. Table I shows the normalized soft-error rates (SER) by α particles and the Cross Section (CS) by O, Ne, Ar, Cu, and Xe irradiation. The CS is an area of upsets when a particle passes a circuit block [3]. Equation (1) shows how to calculate the CS.

$$\mathrm{CS}\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}} \times N_{\mathrm{FF}}} \tag{1}$$

N_{error} is the total number of errors by heavy ions. N_{ion} is the number of heavy ions per 1 cm^2 (fluence). N_{FF} is the number of FFs. The linear energy transfer (LET) values of these ions are 2.2, 3.5, 9.7, 21.2 and 58.8 $\mathrm{MeV\text{-}cm}^2/\mathrm{mg}$ respectively. As a result, the soft-error rates of them were nearly same.

TABLE I
NORMALIZED P_{se} AND CS IN A 28 NM BULK PROCESS[2].

		CS					
FF	V_{th}	SER	O	Ne	Ar	Cu	Xe
DFF	standard	1	1	1	1	1	1
	low	1.04	0.94	1.00	1.14	1.12	0.95
	high	1.03	1.06	0.85	1.07	0.96	1.00

(a) GP (b) LP

Fig. 1. Fabricated chip micrographs with GP and LP transistors.

III. Experimental Setup

We fabricated LP and GP chips and evaluated their soft-error tolerance. Figure 1 (a) (b) show the chip micrographs that contain 83,520 bit GPDFFs (DFFs with GP transistors) and 20,160 bit LPDFFs (DFFs with LP transistors) respectively. Figure 2 shows the cross section of the NMOS transistor in a 65 nm thin-BOX FDSOI process.

α particles irradiation tests were conducted using a 3 MBq ^{241}Am. Each irradiation time was 300 sec. and irradiation was repeated for 10 times. Figure 3 (a) shows the experimental setup of the α particle irradiation test.

We conducted heavy-ions irradiation test at Takasaki Ion accelerators for Advanced Radiation Application (TIARA). We exposed GP and LP chips to Ar and Kr ions. Figure 3 (b) shows the experimental setup of the heavy-ions irradiation test. Each irradiation time was 30 sec. and irradiation was repeated for 5 times. Table II shows LET, energy and the fluences of heavy ions exposed to GPDFFs and LPDFFs.

We measured these chips at static conditions of (DATA,

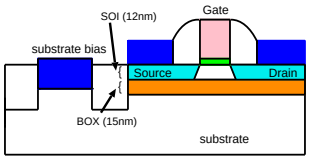
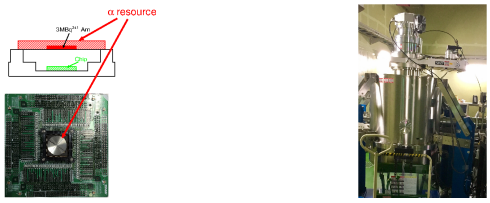


Fig. 2. Thin BOX FDSOI.

TABLE II
LET, ENERGY, FLUENCE OF HEAVY IONS.

	Ar	Kr
LET $[\mathrm{MeV\text{-}cm}^2/\mathrm{mg}]$	17.5	40.9
Energy [MeV]	107	230
Average fluence with GP transistors $[\mathrm{n/cm}^2]$	2.62×10^6	2.44×10^6
Average fluence with LP transistors $[\mathrm{n/cm}^2]$	2.75×10^6	2.88×10^6



(a) α particle (b) heavy ion

Fig. 3. Experimental setups.

TABLE III
NORMALIZATION OF LEAKAGE CURRENT, THRESHOLD-VOLTAGE AND D-Q DELAY OF FF ABOUT GP AND LP TRANSISTORS.

	GP	LP
Threshold-Voltage	1	1.31
Leakage current	1	0.008
D-Q Delay of FF	1	1.64

CLK) = (0,0), (0,1), (1,0), and (1,1) at supply voltage ($V_{\rm dd}$) of 0.8 V by α particles and heavy ions irradiation. We measured those two chips by the following procedure.

1) Initialize serially-connected FFs by all 0 or all 1
2) Stabilize CLK to 0 or 1
3) Expose α particles or heavy ions
4) Read out stored values of FFs
5) Count the number of upsets
6) Repeat 1)-5) for four (DATA, CLK) conditions

IV. Measurement Results

A. Analysis by circuit simulations

Table III shows normalized leakage current, threshold voltage and D-Q delay of FFs with GP and LP transistors in the 65 nm thin-BOX FDSOI process by circuit simulations. The leakage current of LP transistors is 99% lower than that of GP transistors. LP transistors are suitable for IoT devices that are working periodically for a long battery life.

B. Analysis by The Measurement

- α Particles Irradiation Test

Table IV shows the average numbers of upsets on GPDFFs and LPDFFs by α particles. The results of GPDFFs are from [4]. Figure 4 shows the experimental results by α particles. The error bars are 95 % confidence. There is no or a few errors on the LPDFFs at all static conditions. The LPDFFs are stronger against soft errors than GPDFFs at all static conditions.

- Heavy Ion Irradiation Test

Table V shows the average numbers of upsets on GPDFFs and LPDFFs by Ar and Kr. Figures 5 and 6 show the

TABLE IV
AVERAGE NUMBERS OF UPSETS AND TOTAL NUMBERS OF FFS ON GPDFFS AND LPDFFS IN THE 65 NM THIN-BOX FDSOI PROCESS BY α PARTICLES.

	(DATA,CLK)				
chip (FF)	(0,1)	(1,1)	(0,0)	(1,0)	average
GP (83520 bit)	1449.9	108.9	8.9	960.4	632.0
LP (20160 bit)	0.1	0.1	0	0	0.05

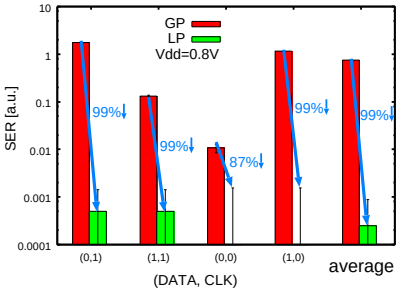


Fig. 4. Measurement results by α particle.

TABLE V
AVERAGE NUMBERS OF UPSETS AND TOTAL NUMBERS OF FFS ON GPDFFS AND LPDFFS IN THE 65 NM THIN-BOX FDSOI PROCESS BY AR AND KR IRRADIATION.

		(DATA,CLK)				
ion	chip (FF)	(0,1)	(1,1)	(0,0)	(1,0)	average
Ar	GP (83520 bit)	285.8	141.2	144.8	167.4	148.8
	LP (20160 bit)	29.0	23.0	21.2	20.2	23.4
Kr	GP (83520 bit)	473.0	156.4	162.4	271.6	265.9
	LP (20160 bit)	55.0	32.4	28.2	27.2	35.7

experimental results by Ar and Kr with error bars with 95% confidence.

The LPDFFs are stronger against soft errors than GPDFFs at all static conditions. These results clearly reveal that the average CSs of the LPDFFs are 50% and 54% smaller than those of GPDFFs by Ar and Kr ions respectively.

Our assumption is that the reason is the difference of the number of carriers in diffusion. Equation (2) expresses auger recombination originated from electrons and holes. It is in proportion to the cube of the number of carriers.

$$R_{\rm auger} = C_{\rm n} n(np - {n_{\rm i}}^2) + C_{\rm p} p(np - {n_{\rm i}}^2) \qquad (2)$$

$C_{\rm n}$ and $C_{\rm p}$ are the constant of auger recombination. n and p are the electron and the hole density. $n_{\rm i}$ is the intrinsic carrier density.

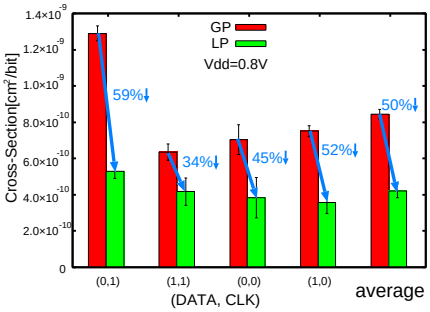


Fig. 5. Measurement results by Ar irradiation.

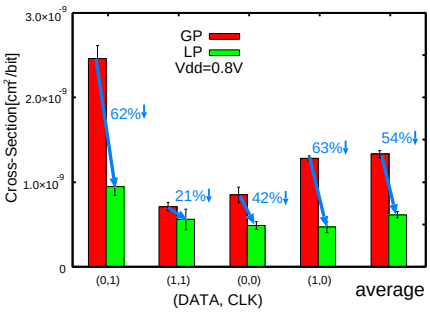


Fig. 6. Measurement results by Kr irradiation.

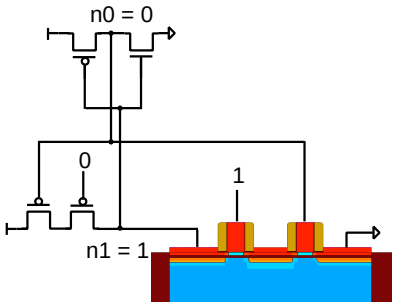


Fig. 7. Latch on device and circuit simulations. NMOS of tristate inverter is implemented by 3D device model. Other transistors are in the circuit level.

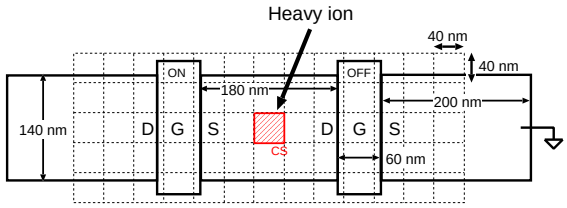


Fig. 8. Top view of the 3D device model to evaluate CS on the tristate invertor.

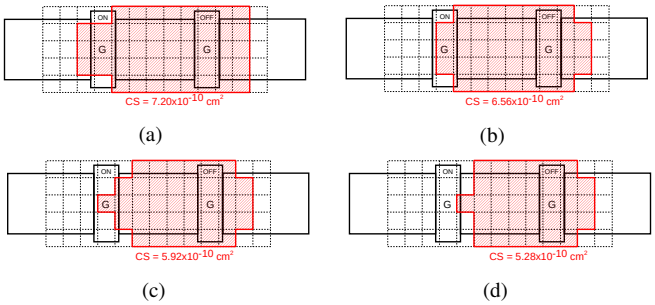


Fig. 9. Transition of CS by changing the doping concentration. (a) 1×10^{20} cm^{-3} (b) 2×10^{20} cm^{-3} (c) 3×10^{20} cm^{-3} (d) 4×10^{20} cm^{-3}

The quantities of the carriers collected in diffusion depend on those of impurity density, which affects soft-error tolerance. The larger the rate of auger recombination is, the smaller the CS becomes. We evaluated the current-voltage (Ids-Vgs) of the transistor on TCAD simulations by changing the doping concentration. The result revealed that it was almost same even if we changed the doping concentration. Our assumption is that doping concentration is dense in diffusion with LP transistors. We carried out TCAD simulations using the Synopsys Sentaurus to see how soft-error tolerance is influenced by the doping concentration. We calculated soft-error tolerance of the latch (Fig. 7) with LP transistors in the 65 nm FDSOI process at V_{dd} of 0.8 V. We set the initial value of n0 to 0 and n1 to 1. The two NMOS transistors in the tristate inverter is implemented by 3D device models. Other transistors are in the circuit level.

An Ar ion hits on the NMOS region. Figure 8 shows a top view of the 3D device model to evaluate CS on the tristate invertor. Heavy ions hit every 40 nm grid. If a heavy ion flips the latch at a point, the 40 nm $\times$ 40 nm square region around the hit point is included in CS. We evaluate the CS by changing the doping concentration from 1×10^{20} cm^{-3} to 4×10^{20} cm^{-3}.

Figure 9 shows the result of CS when Ar ions hit vertically on the NMOS region. The CS is decreasing as increasing the doping concentration. The CS by 4×10^{20} cm^{-3} doping concentration is about 25 % smaller than that by 1×10^{20} cm^{-3} doping concentration. The doping concentration is a dominant factor to fluctuate the soft-error sensibility.

V. Conclusion

We evaluated the soft-error tolerance of two chips with GP and LP transistors in a 65 nm FDSOI process by α particles and heavy ion irradiation. LP transistors are 31% higher threshold than GP transistors. At $V_{\mathrm{dd}} = 0.8\mathrm{V}$, LPDFFs were 3051x stronger against soft errors than GPDFFs by α particle. There were a few errors on LPDFFs. The average CSs of the LPDFFs are 50% and 54% smaller than those of GPDFFs by Ar and Kr ions respectively. LP transistors have smaller leakage current and stronger against soft errors than GP transistors.

The difference of the doping concentration in diffusion influences soft-error tolerance. The CS on the NMOS of 4×10^{20} cm^{-3} doping concentration becomes 27 % smaller than that of 1×10^{20} cm^{-3} doping concentration.

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Acknowledgment: The authors would like to thank to QST (National Institutes for Quantum and Radiological Science and Technology). The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC) in collaboration with Renesas Electronics Corporation, Cadence Corporation, Synopsys Corporation and Mentor Graphics Corporation. This work is supported by the Program on Open Innovation Platform with Enterprises, Research Institute and Academia (OPERA) from Japan Science and Technology Agency (JST).