A Radiation-hard Layout Structure to Control Back-Gate Biases in a 65 nm Thin-BOX FDSOI Process

Junki Yamaguchi, Jun Furuta and Kazutoshi Kobayashi†
†Graduate School of Science & Technology, Kyoto Institute of Technology

Abstract

We propose a radiation-hard layout structure to control back-gate biases for thin-BOX FDSOI. The structure with fixed back-gate bias has strongest against soft errors, while the structure with P+ and N+ diffusions under power and ground rails makes flip-flops stronger against soft errors with back-gate bias controllability than the conventional structure without P+ and N+ diffusions. The test chip was fabricated by 65 nm bulk and thin-BOX FDSOI processes. The experimental results with α sources reveals that the structure with diffusions is effective to supress soft errors on the thin-BOX process. But it is not effective on the bulk process.

I. Introduction

The decrease of reliability of semiconductor chips is very problematic by the aggressive process scaling down to nanometers. Soft errors are one of main causes to threaten the reliability [1]. Semiconductor chips are used everywhere from consumer products to infrastructures. Products with higher reliability such as automotive, aerospace and medical use must have some anti-soft-error capabilities. SOI (Silicon On Insulators) is a promising candidate to reduce soft errors as the device level [2]. In the circuit-level, redundant circuits are usually used. But redundancy increases area, delay and power overheads. The device- and layout-level approaches are better to suppress such overheads.

This paper evaluates the radiation hardness of flip-flops of three layout structures with different substrate-bias fixing methodologies for thin-BOX SOI processes. Those three structures have identical area. Due to substrate bias stability, soft-error hardness are different. We fabricated test chips by 65 nm bulk and thin-BOX FDSOI (Fully-Depleted SOI) processes [3].

Section II explains the test chip and the three layout structures. We evaluate the radiation hardness by T-CAD simulations in Sect. III. The measurement results by by α sources are described in Sect. IV. We conclude this paper in Sect. V.

II. Test Chip

Three types of layout structures are prepared to verify how the stability of substrate biases affects soft-error hardness. Fig. 1 shows these structures as follows.

SA Cell structure with fixed substrate bias.

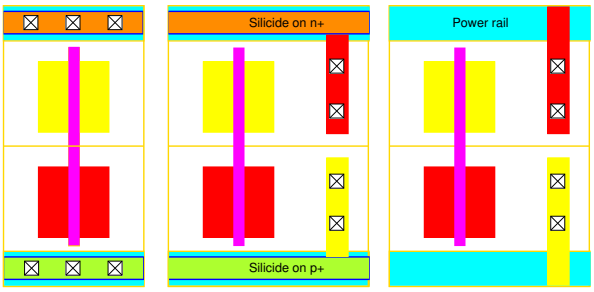

Fig. 1. Three layout structures. SA: fixed substrate bias, SB: substrate bias controlled with well-taps and silicide, SC: substrate bias controlled with only well-taps.

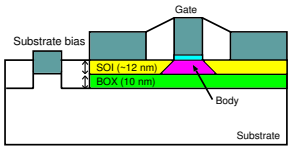

Fig. 2. Cross section of SOTB.

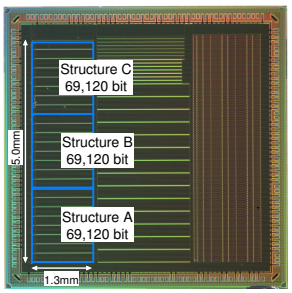

Fig. 3. Chip micrograph.

SB Substrate biases can be controlled by well-taps. N+ and P+ diffusions are placed under power and ground rails, respectively. They are connected with well and substrate taps.

SC Substrate bias can be controlled by only well-taps.

Note that these three layout structures have the identical layout area. SC is a conventional method to control back gate bias. But the well-bias controllability is not sufficient since well and substrate taps are far from transistors. In the fabricated chips, taps are inserted every 104 μm. Farthest transistors are placed over 50 μm from the nearest tap. SB is better since the back gate bias is also fixed by diffusions under power and ground rails close to transistors. The distance between transistors and P+/N+ diffusions is 0.19 μm as shown in Fig. 5. Silicide layers above P+/N+ regions decrease resistance to stabilize the well biases strongly.

Fig. 2 shows the cross section of SOTB (Silicon On Thin BOX [3]), which is one of FDSOI processes than can control back-gate biases through 10-nm thin BOX layers. The channel of MOSFETs is not doped due to less short channel effects of FDSOI. SRAM works at 0.37 V because of extremely

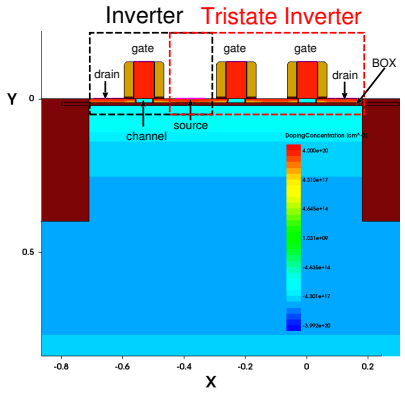

Fig. 4. 3D NMOS device model cross section.

small process variations [3], [4]. SOTB supports the deep-sleep mode by controlling back gate biases [5]. In SB, N+ and P+ diffusions under power and ground rails are formed in the body region above the thin BOX layers of 10nm. It can control the back-gate bias through the thin BOX layers.

It is possible to form the P+ and N+ diffusions through the thin BOX layers. In such structure, however, voltage sources to control back-gate bias are directly connected to substrate. It is impossible to pull the back-gate bias to forward above the voltage at which diodes between P-well and N-well turn on.

We designed and fabricated test chips by the 65 nm bulk and SOTB processes as shown in Fig. 3. Arrays of FFs with three different layout structures are placed on the left side of the chip.

III. T-CAD Simulations

We constructed latch structures of SB and SC on SOTB for T-CAD simulations. To reduce simulation time, NMOSFETs are implemented as 3D models, while PMOSFETs are as 2D models. NMOSFETs are dominant factors of soft errors because of their faster carrier (electron) mobilities. Fig. 4 shows the cross section of the latch on the SOTB for T-CAD simulations.

When Q (output of the latch) is high, each node stores a specific value as shown in Fig. 5. We compute the amount of charge collections by hitting a charged particle with LET=10 MeV·cm^2/mg perpendicular to MOSFETs on the inverter. Figs. 6 and 7 show charge collection when the reverse body bias (RBB) is applied only on NMOSFETs. By increasing RBB, the amount of charge collection is reduced since it becomes difficult to turn on parasitic bipolar transistors. The amount of charge collection of SB is half of that of SC at VDD=1.0 V and RBB=0 V. Less charge collection is equal to stronger radiation hardness. SB is strong against soft errors because of its stability of substrate biases.

IV. α Irradiation Test

We exposed the fabricated chip to a 3 MBq ^{241}Am source. All tests are done statically by (D, CLK) = (0, 0) for 60 sec. Figs. 8 and 9 shows the number of flipped FFs in the 65-nm bulk and SOTB processes. The number of errors in SOTB is

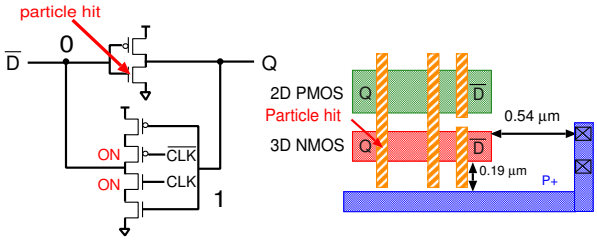

Fig. 5. Simulation conditions when D is high.

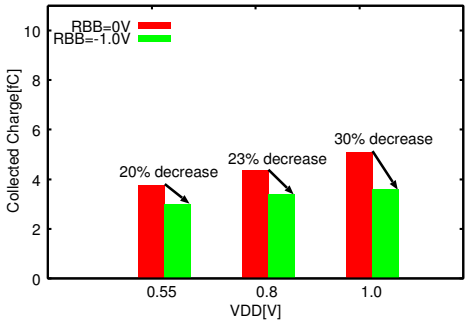

Fig. 6. Charge collection of Structure B when D is high. RBB on NMOS.

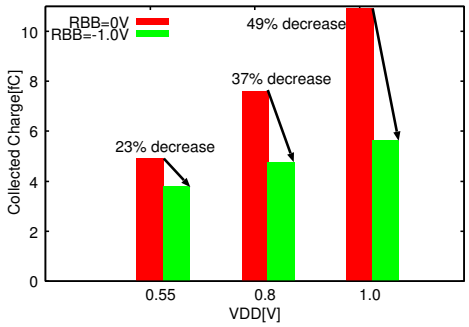

Fig. 7. Charge collection of Structure C when D is high. RBB on NMOS.

less than 10% of those in bulk. The 65 nm SOTB process has better soft-error immunity than the bulk [6].

In the bulk process, there is no distinct tendency among all structures. In the SOTB process, SA is strongest. In bulk, the main phenomenon to cause soft errors is the charge collection, which is no correlation with the stability of substrate. But in SOTB, it is the parasitic bipolar action affected by the stability of substrate. If the substrate bias is stable, it becomes hard to turn on parasitic bipolar transistors in the body region since the base terminal is stable. At VDD = 0.4 V as shown in Fig. 9, the numbers of soft errors in SB and SC is 134 and 278, respectively. SB is 2x stronger against soft errors than SC in SOTB.

We investigate the radiation hardness of SB and SC by changing substrate biases. VBP and VBN denote back gate biases of PMOS and NMOS respectively. When the back gate bias is forward, the voltage becomes positive. We put the α source on the chips for 180 sec. by the condition of Vdd = 0.55 V and (D, CLK) = (0, 1). Figs. 10 and 11 show experimental results according to the substrate biases on SB and SC.

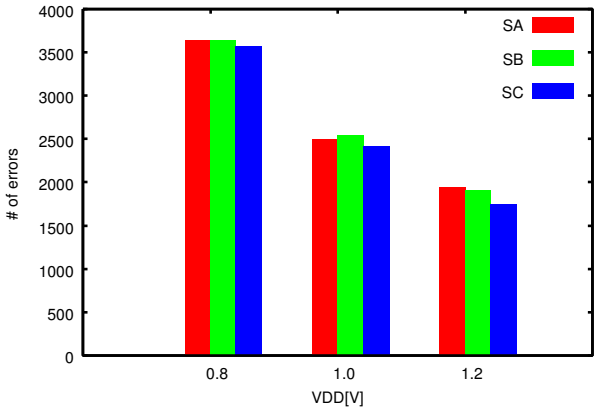

Fig. 8. Number of soft errors in bulk.

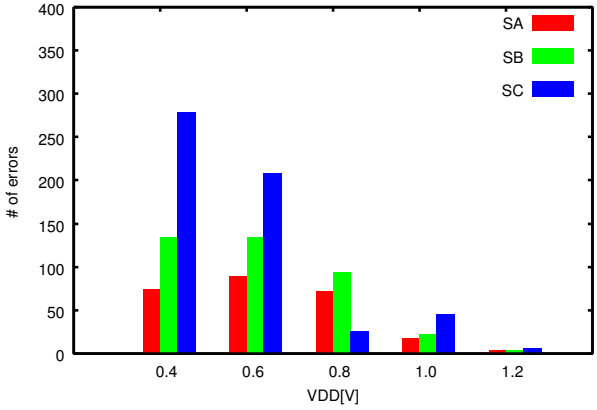

Fig. 9. Number of soft errors in SOTB.

RBB on PMOS and NMOS reduces the number of errors as almost similar to RBB on NMOS. It suggests that NMOS is the dominant factor to soft errors than PMOS. SB has the 70x soft-error hardness than SC at the RBB condition of VBN = -1.0 V. It mentions that SB can control the substrate bias better than SC. If the back-gate bias is pulled to the reverse side, the threshold voltage of transistors becomes high. Larger energy is required to turn on the parasitic bipolar transistors. It becomes hard to flip the latch.

V. Conclusions

We investigate the radiation hardness of three layout structures for the 65-nm bulk and thin-BOX FDSOI (SOTB) processes. The layout structure with the stronger back-gate bias controllability and stability has lower soft error rates on the thin-BOX FDSOI. The layout structure named SB controls back gate-biases by well taps and silicide under power and ground rails close to transistors, while SC controls back-gate biases by only well taps far from transistors. T-CAD simulations and α irradiation tests reveal that SB is stronger against soft errors than SC in the thin-BOX FDSOI process. At Vdd=0.4 V, SB is 2x stronger than SC. In the bulk process, the substrate stability is not related to soft error hardness. It is because the charge collection is the dominant factor to cause soft errors in the bulk process, while the parasitic bipolar action is dominant in the thin-BOX FDSOI process.

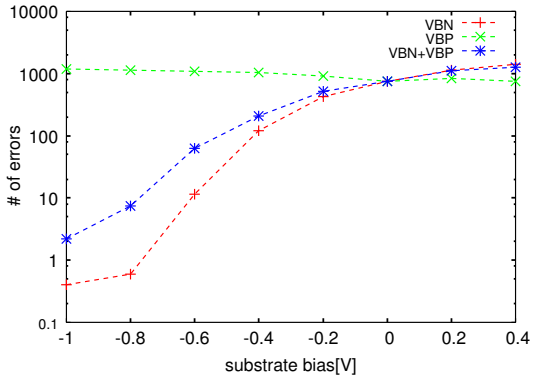

Fig. 10. Number of soft errors of SB by body biases.

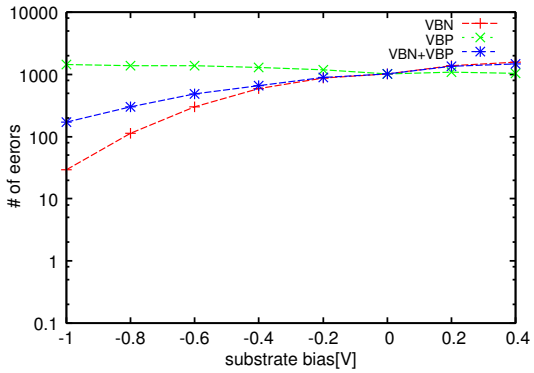

Fig. 11. Number of soft errors of SC by body biases.

Acknowledgment

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References

[1] R. Baumann, "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction," in *IEDM*, 2002, pp. 329–332.

[2] A. Makihara, T. Ebihara, T. Yokose, Y. Tsuchiya, Y. Miyazaki, Y. Satoh, H. Shindou, and S. Kuboyama, "Total ionizing dose and single event effects test results of a radiation hardness-by-design library for 0.15μm fully depleted SOI-ASIC," in *RADECS*, Sept. 2009, pp. 602–605.

[3] Y. Morita, R. Tsuchiya, T. Ishigaki, N. Sugii, T. Iwamatsu, T. Ipposhi, H. Oda, Y. Inoue, K. Torii, and S. Kimura, "Smallest vth variability achieved by intrinsic silicon on thin BOX (SOTB) CMOS with single metal gate," in *VLSI Tech. Symp.*, June 2008, pp. 166–167.

[4] Y. Yamamoto, H. Makiyama, H. Shinohara, T. Iwamatsu, H. Oda, S. Kamohara, N. Sugii, Y. Yamaguchi, T. Mizutani, and T. Hiramoto, "Ultralow-voltage operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM down to 0.37 V utilizing adaptive back bias," in *VLSI Cir. Symp.*, 2013, pp. T212–T213.

[5] K. Ishibashi, N. Sugii, S. Kamohara, K. Usami, A. Hideharu, K. Kobayashi, and P. Cong-Kha, "A perpetuum mobile 32bit CPU on 65nm SOTB CMOS technology with reverse-body-bias assisted sleep mode," *IEICE Trans. on Electronics*, vol. E98-C, no. 7, pp. 536–543, July 2015.

[6] K. Kobayashi, K. Kubota, M. Masuda, Y. Manzawa, J. Furuta, S. Kanda, and H. Onodera, "A low-power and area-efficient radiation-hard redundant flip-flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1881–1888, Aug. 2014.