Analysis of Terrestrial Single Event Upsets by Body Biases in a 28 nm UTBB Process by a PHITS-TCAD Simulation System

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Abstract

We analyze the soft-error tolerance of a latch in a 28-nm UTBB (Ultra Thin Body and BOX) process by a PHITS-TCAD simulation system. It is composed of two parts, a particle transport simulation by PHITS (Particle and Heavy Ion Transport code System) and a device simulation. The neutron induced SERs (soft error rates) can be analyzed by the simulation system. We investigate the soft errors on 28-nm UTBB process by PHITS-TCAD simulation and alpha irradiation. The soft error tolerance when VDD is 0.4V is 22.5 times weaker than when 1V. The soft error tolerance with 0.6V reverse body bias is 1.5 times weaker than that with zero body bias. The simulation results have similar tendency with the alpha irradiation experimental results.

Introduction

The impact of soft errors has been serious with process scaling of integrated circuits[1)]. Soft errors can be caused by a particle hit, since a sensitive node in drain regions collects radiation-induced charge. Reboot or reset can restore from soft errors. But highly reliable products such as super computers and avionics demand higher soft error tolerance.

Ultra Thin Body and BOX (UTBB)[2)] is one of FD-SOI (Fully Depleted Silicon on Insulator). Thin BOX layer can suppress charge collected into device. Thus, it has higher soft error tolerance than bulk structures. The gate oxide layer is composed of thicker high-k material. There is no dopant in the channel of FD-SOI. Variations of the transistors are suppressed, and the supply voltage can be decreased.

In this paper, we analyze the neutron induced soft errors on 28-nm UTBB latch by the PHITS[3)]-TCAD simulation system[4)] and alpha experiments. The simulation results reveal that the soft error tolerance of 28-nm UTBB is decreased by reducing supply voltage or applying reverse body bias. Section II shows the PHITS-TCAD simulation system. Section III describes the simulation method by PHITS-TCAD. Section IV shows the simulation results of neutron-induced SER and experimental results of alpha irradiation. Section V concludes this paper.

PHITS-TCAD Simulation System

Fig. 1 illustrates the schematic flow of soft error simulation using the PHITS-TCAD simulation system[4)]. PHITS is devoted to simulations of secondary ion generation via nuclear interaction of

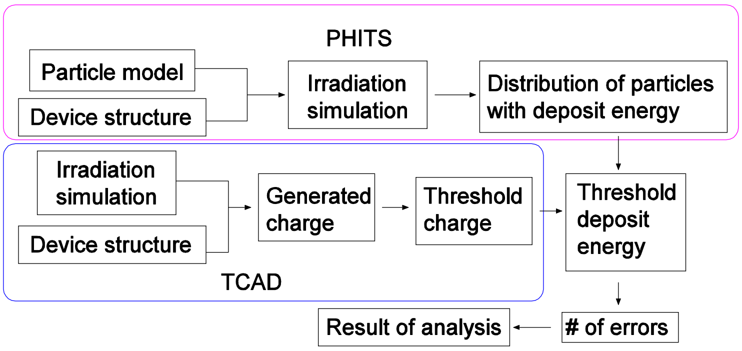


Fig. 1. Flow chart of the PHITS-TCAD simulation system.

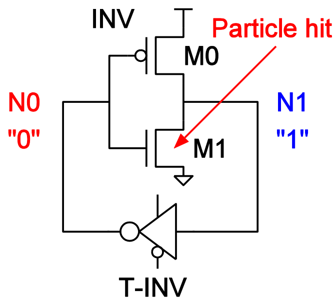


Fig. 2. A conventional latch.

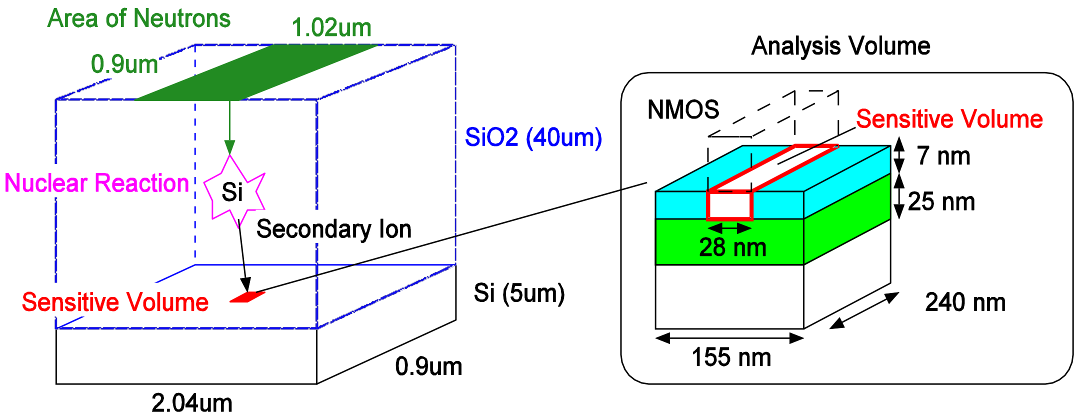


Fig. 3. Device structure used in PHITS. The sensitive volume is defined by the active area of a latch (28 nm x 240 nm) and the sensitive depth (7 nm).

incident particle with constituent atoms in a device, and the sequential charge deposition. PHITS calculates the deposit energy of a secondary ion when it gets into the sensitive volume of a device as shown in Fig. 1.

TCAD simulations calculate the generated charge (Q_{gen}) collected into a drain region by a particle hit as shown Fig. 1. An SBU (Single Bit Upset) occurs in the circuit when Q_{gen} is larger than the threshold charge (Q_{th}), which is used to calculate the threshold deposit energy. The deposit energy can be converted to the Q_{dep} . The deposit energy of 1MeV is equivalent to 50 fC Q_{dep} in this research[5].

The number of particles according to deposit energy can be also obtained by PHITS. The secondary ions, which are larger than the threshold deposit energy, can cause soft errors. Thus the total number of the secondary ions larger than the threshold deposit energy is equal to the number of SBUs.

Simulation Setup

Fig. 2 shows a conventional latch schematic. A radiation particle hits the gate of NMOS transistor of the inverter. The node N0 is set to “0”. The device structure was determined based on 1). The UTBB structure has the BOX and the SOI body with the thicknesses of 25-nm and 7-nm respectively. An ion particle hits the gate of NMOS transistor of the inverter in the UTBB in TCAD. The minimum LET of ions which can flip the value of a latch is defined as the threshold LET.

Fig. 3 shows the device structure in PHITS simulations. It shows an inverter in a latch. The SOI body under the gate of NMOS transistor of an inverter is considered as a sensitive volume. The size of the sensitive volume is 28 nm × 240 nm × 7 nm.

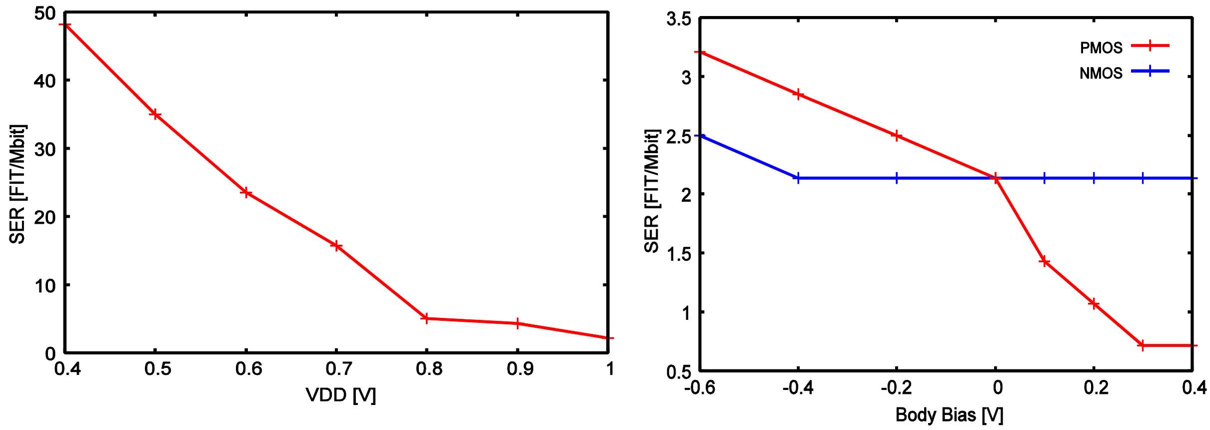
SER Analyses and Alpha Experimental Results

We analyze neutron induced soft error rates of a 28-nm UTBB structure according to supply voltages and body biases by the PHITS-TCAD simulations and alpha irradiation experiments. The simulation results are shown in this section.

Eq. (1) is used to calculate SERs by PHITS-TCAD.

$$SER[\mathrm{FIT/Mbit}] = \frac{3600 \times 10^9 \times A_{\mathrm{neutron}} \times N_{\mathrm{error}} \times Flux \times 10^6}{N_{\mathrm{neutron}}} \quad (1)$$

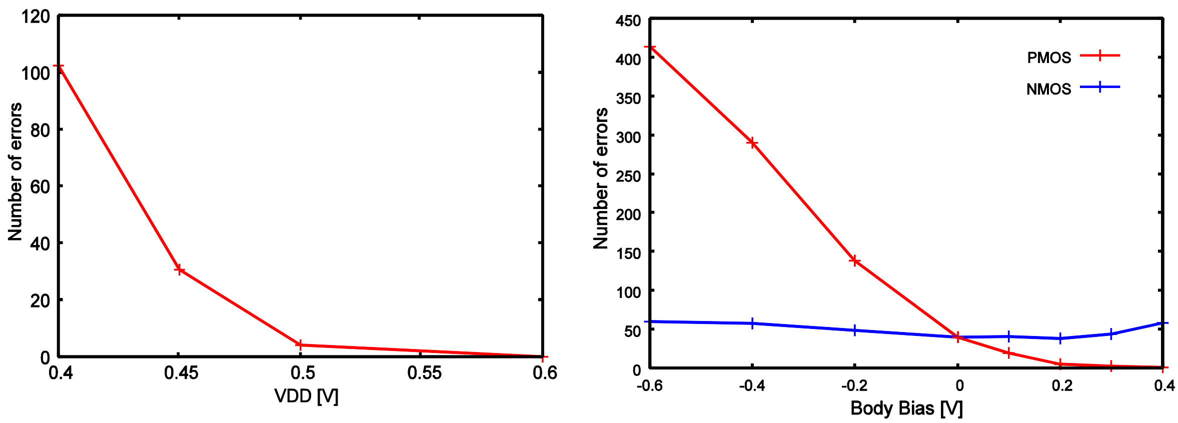
where N_{error} and N_{neutron} are the number of errors and incident neutrons, A_{neutron} is the area of neutron irradiations, and $Flux$ is the total neutron flux in the unit of $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ in PHITS calculation. The results of SER calculated with $A_{neutron} = 0.9 \times 1.02\ \mu\mathrm{m}^2$, $N_{neutron} = 10^{10}$, and $Flux = 0.108\ \mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ in Eq. (1).



(a) The SER of reducing VDD according to simulations.

(b) The SER of applying body bias according to simulations.

Fig. 4. Results of neutron induced SER by PHITS-TCAD simulations.



(a) The number of errors by reducing VDD according to alpha irradiation experiments.

(b) The number of errors by applying body bias when VDD is 0.4V according to alpha irradiation experiments.

Fig. 5. Results of alpha irradiation experiments.

Fig. 4(a) shows the SERs according to supply voltages by the PHITS-TCAD simulations. VDD is changed from 1V to 0.4V. The SERs of applying body bias by the PHITS-TCAD is also shown in Fig. 4(b).

The SER increases by reducing the supply voltage. It becomes easy to upset a latch by reducing the supply voltage. The SER increases 22.5 times by reducing the supply voltage from 1V to 0.4V. The SER when VDD is 1V increases by applying reverse body bias for the PMOS transistor M0 in Fig. 2. Applying body bias for M0 changes the soft error tolerance compared to applying body bias for the NMOS transistor M1 because M0 is in on-state but M1 is in off-state. Since the performance of M0 in on-state is changed by applying body bias, the SER decreases by increasing the PMOS body bias. The SER increases 1.5 times by applying reverse body bias from 0V to 0.6V.

There is no error in the 28-nm UTBB structure by neutron irradiation experiments. For this reason, we investigate experimental results of alpha irradiation. A 3MBq ^{241}Am alpha source is used in the experiments and the area of the alpha source is 1cm^2. The irradiation time is one minute. Fig. 5(a) shows the number of errors by reducing VDD and Fig. 5(b) shows the number of errors by applying reverse body bias for PMOS and NMOS when VDD is 0.4V. They show similar tendencies with the neutron irradiation simulations from alpha irradiation.

Conclusion

We analyze the soft error rates according to supply voltages and body biases in a 28-nm UTBB latch structure by the PHITS-TCAD simulations. We show that the SER is increased by reducing supply voltage or applying reverse body bias. The SER increases 22.5 times by reducing supply voltages from 1V to 0.4V. The SER increases 1.5 times by applying reverse body biases for PMOS transistor from 0V to 0.6V. However, there is no error by neutron irradiation experiments. The neutron irradiation simulation results are consistent with the alpha irradiation experimental results.

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