Radiation Hardness Evaluations of FFs on 28nm and 65nm Thin BOX FD-SOI Processes by Heavy-Ion Irradiation

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Abstract

Recently VLSIs have a wide range of use. A highly reliability system such as devices for aerospace and medical use must mitigate soft errors. We evaluate the radiation hardness of Flip-Flops (FFs) in 65nm silicon on thin BOX (SOTB) and 28nm ultra-thin body and BOX (UTBB) process by heavy-ion irradiation. Experimental results show that the soft error tolerance of FFs in 28nm is about 18 times higher than that in 65nm compared by SERs of the same number of FFs. If comparing soft error rates in the same circuit area, SER in 28nm is about two times stronger than that in 65nm.

Introduction

From year after year, semiconductor devices continue scaling. High degrees of integration of LSIs have a wide range of use. On the other hand, a nanometer device needs to mitigate soft errors[1,2)]. Soft errors are caused by radiation particles. Neutrons are one of main sources in the terrestrial regions, while heavy-ions are that in the outer space. Fig. 1 shows spectrums of heavy-ions at the galactic system. When a device uses in the outer space, we have to seriously consider radiation effects from heavy-ions. Especially, a high reliability system has to need a soft error tolerance for heavy-ions with the LET of 40 $\mathrm{MeV/(mg/cm^2)}$ in the outer space[2)].

We evaluate soft error tolerances of FFs in a 28nm UTBB and that in 65nm SOTB by heavy-ion irradiation. A Fully Depleted Silicon On Insulator (FD-SOI) has a high soft error tolerance in the terrestrial field. However, the scaling of FD-SOI may raise SER[3)]. From the results of heavy-ion irradiation, we found that They have higher error tolerance compared with a 65nm bulk process.

FD-SOI

Fig. 2 shows the structure of a Fully Depleted Silicon On Insulator (FD-SOI) CMOS process. This device has a layer of silicon Buried OXide (BOX). SOI has higher tolerance for soft errors. BOX layers disturb electrical charge at a drain region. If electron hole pairs are generated at the substrate region, they do not penetrate transistor (SOI) regions[4)]. Since, a transistor regions are insulated from the substrate, parasitic bipolar transistors does not turn on. Table 1 show parameters of 28nm UTBB and 65nm SOTB. The thin body regions do not contain impurities. Thus transistor variations are suppressed. Those thin BOX FD-SOI processes enable to control substrate biases in order to reduce energy consumption or increase performances[5,7)].

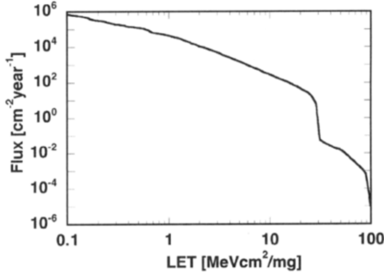


Fig. 1. Spectrums of heavy-ions at the galactic system [2].

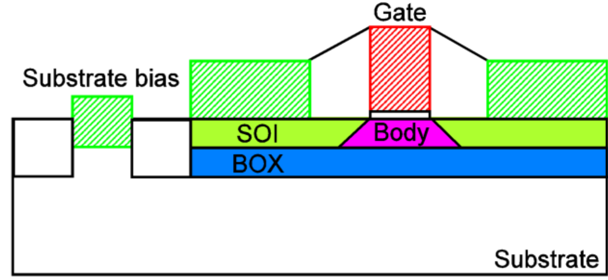
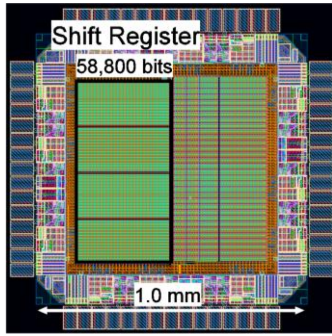
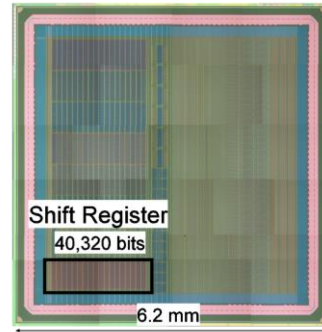


Fig. 2. FD-SOI CMOS Process.



(a) 28nm chip.



(b) 65nm chip.

Fig. 3. Floor plan of test chips.

Measurements

We evaluate the soft error tolerance of FFs on 65nm SOTB and 28nm UTBB processes by heavy-ion irradiations at the TIARA (Takasaki Ion Accelerators for Advanced Radiation Application). A shift register on 65nm has 40,320 bits, and that of 28nm has 58,800 bits. Both shift registers are composed of non-redundant DFFs (D-type Flip Flops). Floor plans of test chips are shown Fig.3.

A method of how to measure by heavy-ion irradiations are shown below.

1. Initialize all FFs in the shift register.
2. Heavy ion irradiation without applying any clock signal.
3. Read values of all FFs to count the number of upsets.

Table 2 shows Linear Energy Transfer (LET) of irradiated heavy-ions. Eq.1 is used in order to calculate cross sections.

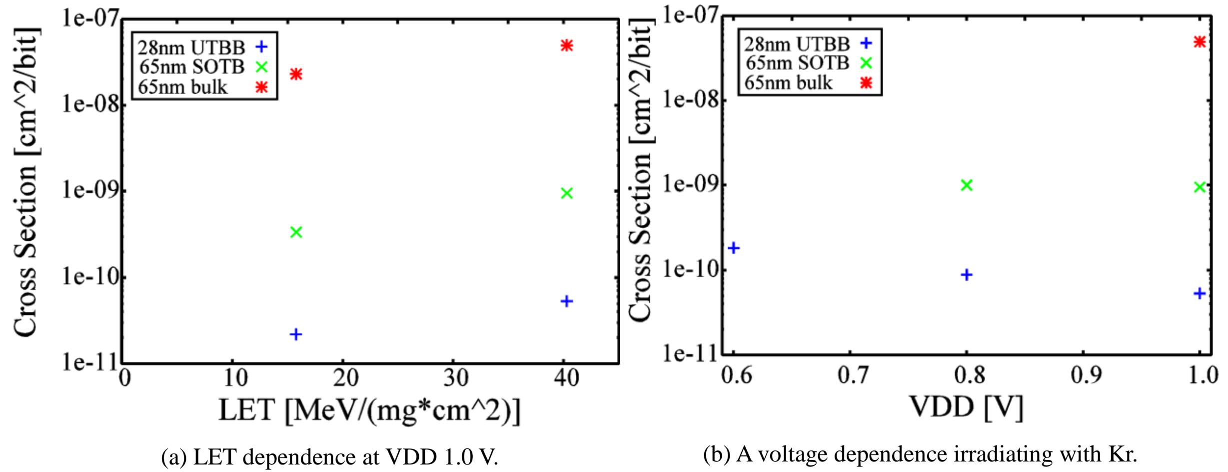
$$CS_{\mathrm{heavyion}}\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{F_{\mathrm{ion}} \times N_{\mathrm{bit}}} \quad (1)$$

Table 1. Parameters of FD-SOI

	Gate length [nm]	Body thick- -ness [nm]	BOX thick- -ness [nm]
UTBB[5]	28	7.0	25
SOTB[6]	65	12	10

Table 2. LET and Energy of heavy-ions

Heavy-ion	LET [MeV/(mg/cm²)]	Energy [MeV]
Krypton (Kr)	40.31	394
Argon (Ar)	15.76	137
Neon (Ne)	6.54	69.7



(a) LET dependence at VDD 1.0 V.

(b) A voltage dependence irradiating with Kr.

Fig. 4. Heavy-ions cross sections of FFs on 28nm and 65nm processes.

Table 3. Cross sections of experimental results.

	Cross Section $[\mathrm{cm}^2/\mathrm{bit}]$					
	28nm UTBB			65nm SOTB		65nm bulk
Heavy-ions	1.0V	0.8V	0.6V	1.0V	0.8V	1.0V
Kr	5.29×10^{-11}	8.81×10^{-11}	1.84×10^{-10}	9.65×10^{-10}	1.00×10^{-9}	5.02×10^{-8}
Ar	2.18×10^{-11}	3.34×10^{-11}	1.07×10^{-10}	3.38×10^{-10}	4.14×10^{-10}	2.32×10^{-8}
Ne	0	1.43×10^{-11}	2.51×10^{-11}			

Cross sections (CS_{heavyion}) are calculated from the number of errors (N_{error}), the number of ions per unit area (F_{ion}), and the number of bits (N_{bit}).

Experimental Results and Disscusion

Cross sections of 28nm and 65nm processes are shown in Fig. 4 Table 3 shows cross sections of experimental results. Fig. 4 (a) shows that the LET dependence when VDD is 1.0 V. Compared to latch circuits in 150nm SOI process[8)], cross sections of these process is more than one order of magnitude lower. The cross section of FFs in 65nm bulk is about 50 times higher than that in 65nm SOTB. The cross section of FFs in 65nm SOTB is about 18 times higher than that in 28nm. Fig.4 (b) shows that the voltage dependence by Kr. When FFs in 28nm process operates at 0.8 V, the cross section is about 3.5 times higher than at 1.0 V.

Fig. 5 compares SERs of FFs in 28nm UTBB with that in 65nm SOTB. The SERs of FFs in 28nm is approximately 0.13 times that in 65nm compered by cross sections of the same number of FFs. In the same circuit area, SERs in 28nm is approximately half than that in 65nm. Typically, the scaling of semiconductor devices raises SER. Since body thickness of 28nm UTBB is thinner than that of 65nm SOTB, the soft error tolerance of 28nm UTBB is stronger than that of 65nm SOTB.

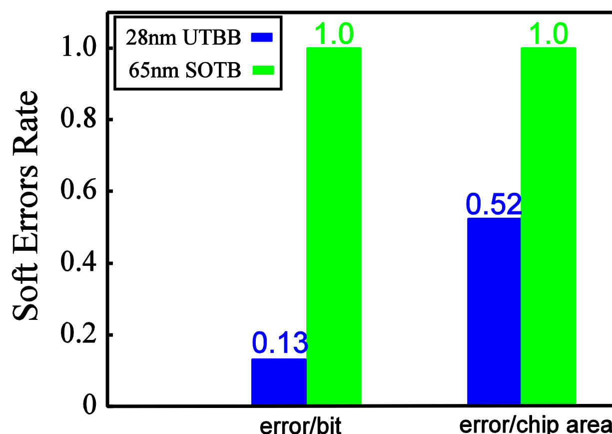


Fig. 5. Comparing SERs of FFs in 28nm UTBB with that in 65nm SOTB.

Conclusion

We evaluate the radiation hardness of FFs on 28nm UTBB and that of 65nm UTBB process by heavy-ions irradiations. According to experimental results, SOI is effective for soft errors in 65nm. The soft error tolerance of 28nm UTBB is stronger than that of 65nm SOTB. The soft error tolerance of SOI becomes strong in a process with more thinner body regions. However, it is not sufficiently strong for the outer space. These processes have to mitigate soft errors in order to keep up normal operations.

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