

Intrinsic Vulnerability to Soft Errors and Mitigation Technique by Layout Optimization on DICE Flip Flops in a 65 nm Bulk Process

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Abstract— We evaluated soft error tolerance of DFF and DICEFF in a 65 nm bulk process by heavy ions. Our experimental results showed that DICEFF produced no error up to Ar (LET : 15.4 MeV·cm²/mg) irradiation, but exhibits lower soft error tolerance by Kr (LET : 40.1 MeV·cm²/mg) irradiation. We firstly found that specific pairs of PMOS and NMOS transistors that become sensitive to soft errors by device simulations. We propose several layout structures that can improve soft error tolerance with additional 39-46% area overhead. DICEFF has so many sensitive pairs that is not adequate to highly-scaled process technologies.

I. Introduction

Reliability issues such as radiation-induced soft errors becomes more serious with technology downscaling [1]. Soft errors are one of temporal failures that upset stored values in storage elements such as flip flops (FFs) or SRAMs caused by neutrons and alpha particles in the terrestrial region and by heavy ions in outer space. When a radiated particle hits close to a logic gate, its output node is perturbed, which is called a single event transient (SET) pulse. A single event upset (SEU) occurs when an SET pulse is stored a storage element. In the circuit level, Dual Interlocked Storage Cell (DICE) [2][3], one of the redundant FFs has been proposed for effective countermeasures. It is strong against an upset on a single node, but weak to simultaneous upsets on two or more nodes. Soft error resilience highly depends on Layout structures [4]. It was shown that DICE has low radiation tolerance at a specific stored value and clock state from the measurement results [5].

In this paper, we identify the root cause of vulnerability in DICEFF to heavy ions by device simulations and propose new layout structures. Measurement results of DICEFF in a 65nm bulk process by heavy ions irradiation are shown in Section II. Section III explains analysis of an upset mechanism by device simulations. Section IV proposes a new layout structure by layout optimization. We conclude this paper in Section V.

II. Experimental Results [5]

Figure 1 shows a standard FF called the Delayed FF (DFF). It has no tolerance against soft error. Figure 2 and show 3 a schematic and a layout pattern of the DICEFF for measurement. The DICE structure mitigates soft errors by duplicating latches. The input and output signals of these half C-elements

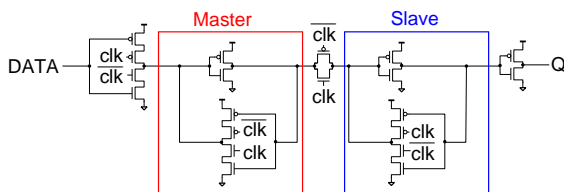


Fig. 1. Delayed flip flop (DFF).

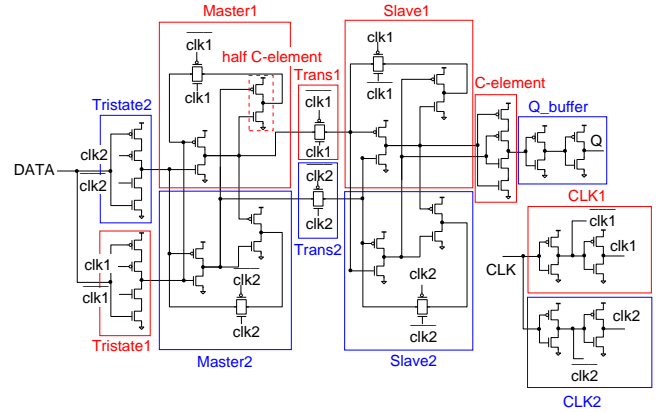


Fig. 2. Dual interlocked storage cell flip flop (DICEFF) for measurement in 2019.

(HCE) have cross-coupled connections to be automatically recovered from a flip on a single node. A test chip was fabricated in a 65 nm bulk process in order to evaluate soft error tolerance. We evaluated soft error tolerance by heavy ion irradiation. Heavy ion irradiation tests were conducted by Ar and Kr ions at Takasaki Ion accelerators for Advanced Radiation Application (TIARA) in order to investigate soft error tolerance. In outer space, most of heavy ions have Linear Energy Transfer (LET) less than 60 MeV·cm²/mg. Thus, we chose Ar (LET : 15.4 MeV·cm²/mg) and Kr (LET : 40.1 MeV·cm²/mg) for measurement. Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1) and V_{dd} was 1.2 V. Heavy ions were irradiated perpendicular to the test chip under the four DATA and CLK states. Cross Section (CS) is used in order to evaluate soft error tolerance, which means an area of upsets when a particle passes through a circuit block. The soft error tolerance becomes stronger if CS becomes smaller.

Figure 4 shows the experimental results of the CSs by Kr irradiation with error bars of 95% confidence. Note that there was no error in DICEFF by Ar irradiation. The average CS of DICEFF is 1/167 smaller than the average CS of DFF. At (DATA, CLK) = (0, 0), CS of DICEFF is only 1/7 smaller than the CS of DFF. On the other conditions, DICEFF has no error. DICEFF has errors only at (DATA, CLK) = (0, 0). However, DFF has almost equivalent error rates at all four static conditions. The layout structure of DICEFF is optimized in order to place critical transistors as far apart as possible. Therefore, DICEFF, which we used in the experiment has a fatal unknown factor of the weakness to soft error at (DATA, CLK) = (0, 0).

III. Analysis of Upset Mechanism by Device Simulation

We use a 3D transistor model constructed to match static characteristics of a SPICE simulation model provided by

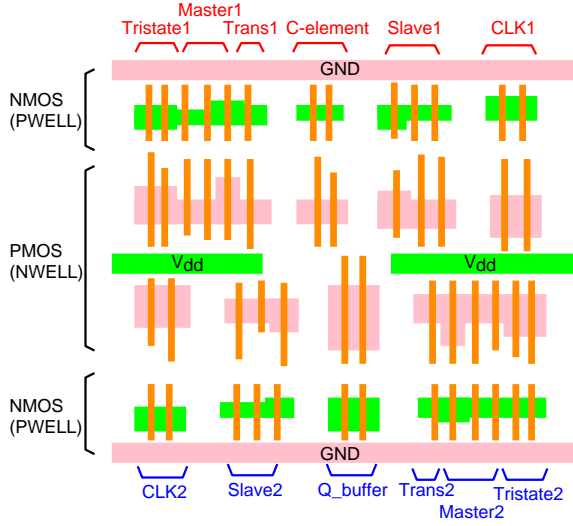


Fig. 3. Simplified layout structure of DICEFF for measurement in 2019.

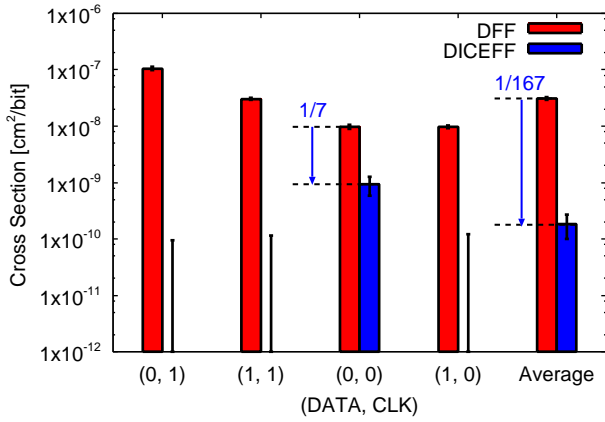


Fig. 4. Experimental results of the CSs by Kr irradiation (There is no error in DICEFF by Ar irradiation).

PDK (process design kit). Device simulations were conducted under the condition at (DATA, CLK)=(0, 0) when soft errors were observed by heavy ion irradiation. At CLK = 0, the transmission gates (Trans1 and 2) in Fig. 2 are off. An SEU only happens in the slave latch. We firstly found that the following two pairs of transistors are critical to cause an SEU by device simulation.

1. NMOS and PMOS transistors in different HCEs.
2. PMOS transistors in the transmission gate and the slave latch.

We discuss how these transistors flips DICEFF by device simulations.

A. NMOS and PMOS transistors in different HCEs in the slave latch

Figure 5 shows the device model and circuit structure used in the simulation. In the fabricated layout structure, all pairs of NMOS transistors in the four HCEs are placed as far apart as possible. But the pair of NMOS and PMOS transistors are closely placed. To reduce simulation time with keeping accuracy, the transistors inside the dotted rectangles are modeled at the device level, the other transistors are modeled at the SPICE level. The layout of the device model is consistent

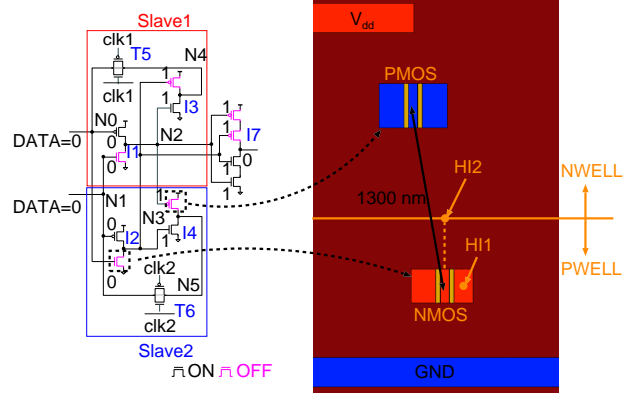


Fig. 5. Circuit diagram of the slave latch and top view of the 3D device model (NMOS and PMOS in the slave latch).

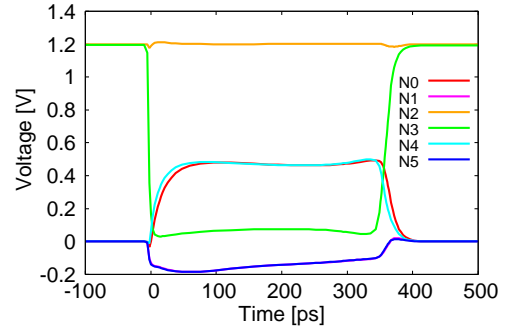


Fig. 6. Voltage waveform at each node when a heavy ion is irradiated to H1.

with the layout of the circuit used for the measurement. LET of the irradiated heavy ion is 40.1 MeV·cm²/mg, assuming Kr and its track radius (r) is computed by Eq. (1) from [6].

$$r [\text{nm}] = 7.16765 \times 10^{-3} \times \sqrt{\text{LET} [\text{MeV} \cdot \text{cm}^2/\text{mg}]} \quad (1)$$

Figure 6 shows the voltage waveforms when a heavy ion hits H1 in Fig. 5. The irradiation point, H1 is the center of NMOS drain diffusion region. In this case, the stored value does not upset as shown in Fig 7. Figure 7 shows how DICEFF is recovered by a single node upset. The high impedance node (N3) stores the upsetting node (N1) as described below. V_{inter} denotes intermediate voltage between V_{dd} and ground.

- 1) Heavy ion hits NMOS I2, $N3 = 1 \rightarrow 0$ then.
- 2) When N3 upsets to 0, $N0$ and $N4 = 0 \rightarrow V_{\text{inter}}$.
N1 and N5 go to high impedance but the stored value still sticks to 0.
- 3) The input of I1 and I2 are 0 and V_{inter} respectively.
N3 goes back to 1 and N2 remains 1.
- 4) Both of I2 and I3 inputs are 1.
N0 and N4 go back to 0.

Figure 8 shows the voltage waveforms when heavy ion hits H2 in Fig 5. The irradiation point, H2 is the intersection on the boundary between PWELL and NWELL and above the center of the NMOS gate terminal to generate electric charge in both PWELL and NWELL. In this case, the stored value upsets according to the state transition as shown in Fig 9. The same state transition occurs not only in the combination

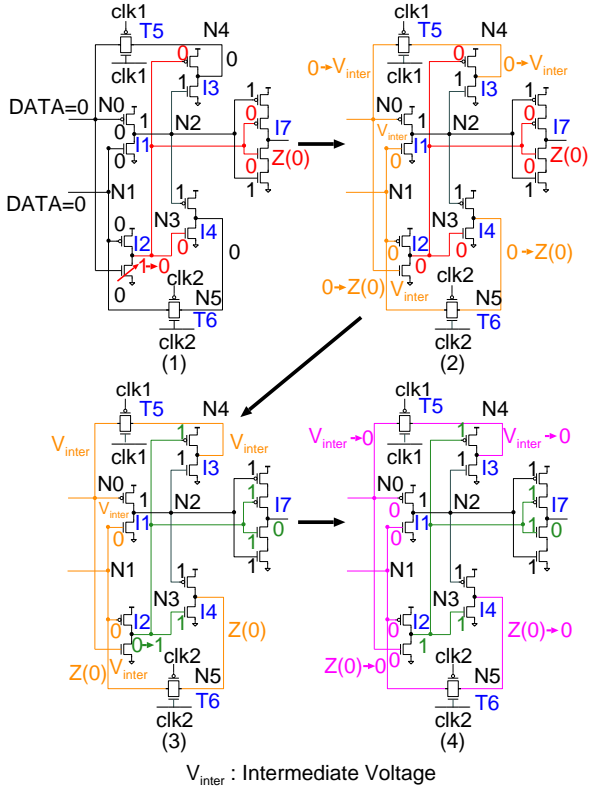


Fig. 7. State transitions when DICEFF recovers.

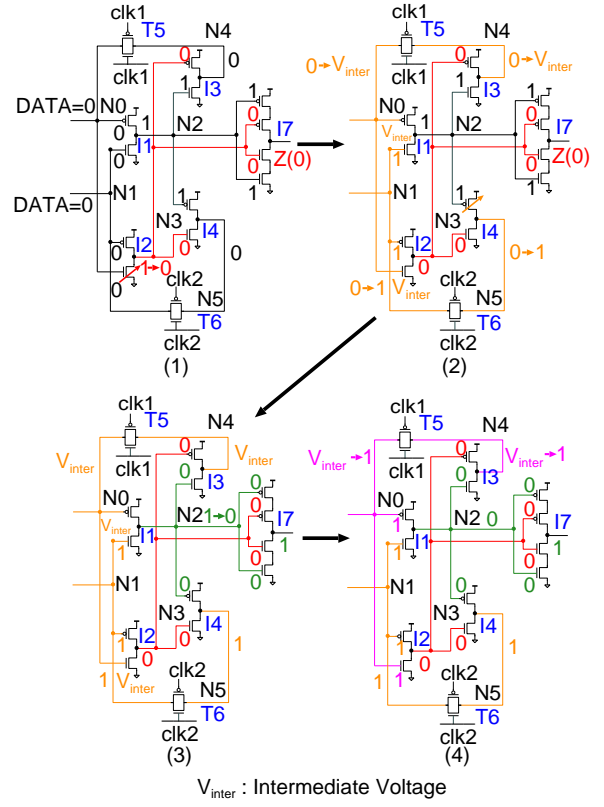


Fig. 9. State transitions when DICEFF upsets.

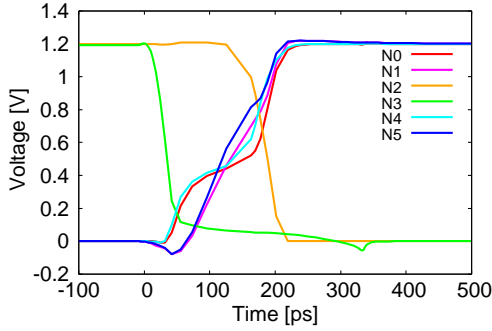


Fig. 8. Voltage waveform at each node when a heavy ion is irradiated to HI2.

of I2 NMOS and I4 PMOS, but also in the combination of I1 NMOS and I3 PMOS.

- 1) Heavy ion hits at HI2, $N3 = 1 \rightarrow 0$ then.
- 2) $N1$ and $N5 = 0 \rightarrow 1$. $N0$ and $N4 = 0 \rightarrow V_{inter}$.
- 3) The input of I1 and I2 are 1 and V_{inter} . $N2$ upsets to 0 and $N3$ remains 0.
- 4) Both of I2 and I3 inputs are 0. $N0$ and $N4$ upset to 1.

B. PMOS transistors in the transmission gate and the slave latch

Figure 10 shows the device model and circuit structure for device simulations. LET of the irradiated heavy ion is $40.1 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, assuming Kr and its track radius (r) is calculated by Eq. (1). Since drain and source terminals of the transmission gates are not directly connected to GND and V_{dd} , an SET pulse is generated only by charge collection. On the other hand, in logic gates such as an inverter, body

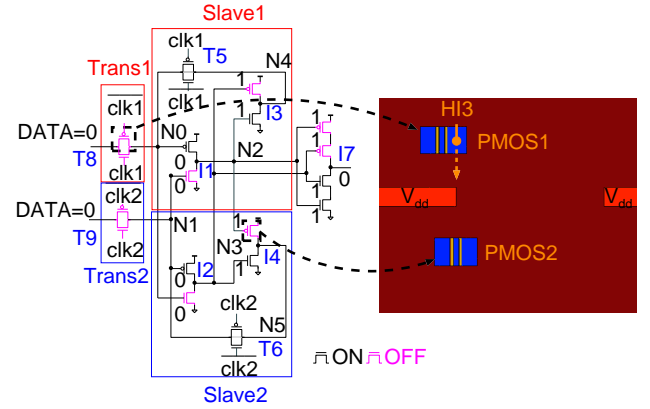


Fig. 10. Circuit diagram of the slave latch and top view of the 3D device model (PMOS in the transmission gate and slave latch).

potential is elevated by a particle hit and the parasitic bipolar transistor composed of drain, source and body terminals turns on to generate an SET pulse. The irradiation point, HI3 is the center of PMOS1 (transmission gate) drain region. Figure 11 shows irradiation angles. No upset occurs at $\phi = 0^\circ$, but an upset occurs at $\phi = 45^\circ$. Figure 12 shows voltage waveforms when a heavy ion is irradiated at $\phi = 45^\circ$. In outer space, heavy ions come from any angle. Those combinations of transistors become susceptible to cause soft errors.

When two transistors simultaneously upsets by a heavy ion hit and there is no high impedance node, an SEU easily occurs at DICEFF. The high impedance node plays an important role to soft error tolerance in DICEFF. The DICEFF that we measured becomes vulnerable to soft errors due to the

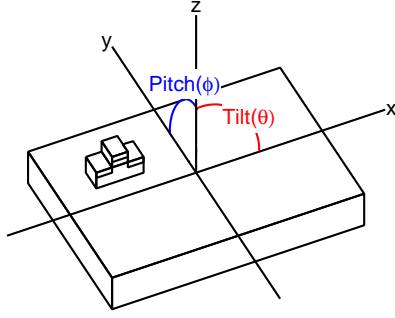


Fig. 11. Definition of irradiation angle.

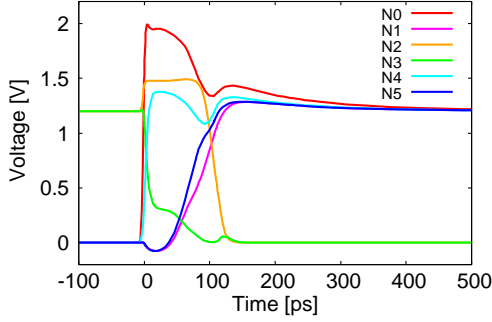


Fig. 12. Voltage waveform at each node when a heavy ion irradiated to H13 at $\phi = 45^\circ$.

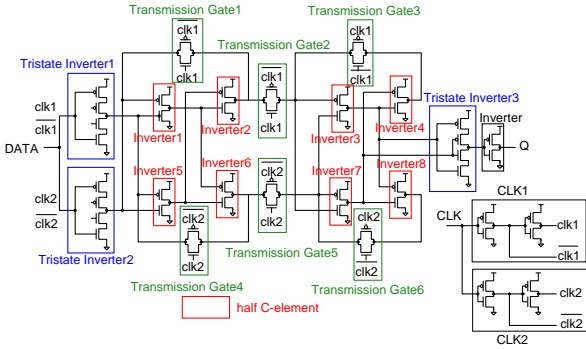


Fig. 13. DICEFF will be measured in 2020.

simultaneous 4 upsets on four nodes of NMOS and PMOS transistors in different HCEs in the slave latch or PMOS transistors in transmission gates and the slave latch by device simulations. There are 50 pairs of transistors that cause soft errors in DICEFF when they are simultaneously turned on.

IV. Examination of Countermeasures by Device Simulation

The discussion so far has been about our DICEFF (Figure 2), which we measured in 2019, and now we will discuss the newly designed DICEFF (Figure 13), which will measure next. Compared with Fig. 2, one inverter is removed by optimization. Note that the color of the STI layer in the 3D device model changed from brown to light blue.

We performed device simulations to examine radiation tolerance of different layout structures. Since the DICEFF belongs to a standard cell library, the cell height is fixed. Transistors in a critical pair can only be moved horizontally to keep the cell height.

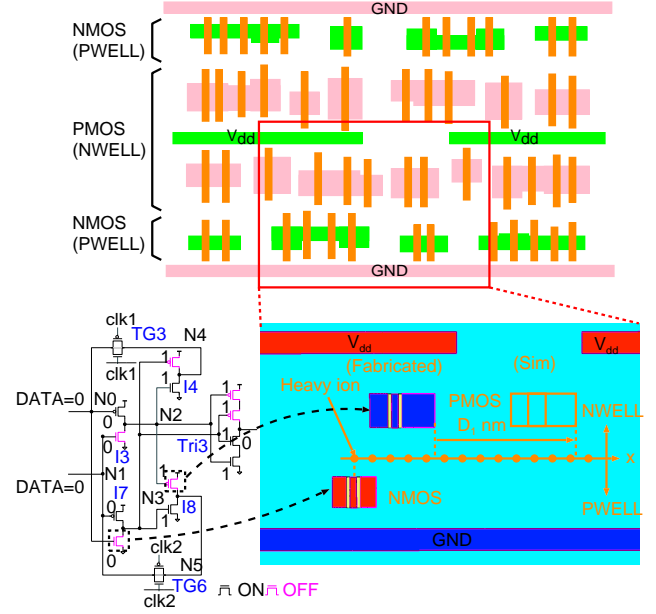


Fig. 14. Simplified layout structure, circuit diagram of the slave latch and top view of the 3D device model used horizontally separation at NMOS and PMOS transistors in different HCEs in the slave latch.

A. NMOS and PMOS transistors in different HCEs in the slave latch

The simulation is performed by horizontally shifting PMOS locations. Irradiation point is moved along the boundary between PWELL and NWELL. We find the minimum distance D_1 not to occur an upset at any irradiation point. Figure 14 shows the top view of the 3D device model. Soft error occurs in the range of $-2250 \text{ nm} < D_1 < 1250 \text{ nm}$ at vertical hit, $-2600 \text{ nm} < D_1 < 2000 \text{ nm}$ at $\theta = 45^\circ$ hit.

B. PMOS transistors in the transmission gate and the slave latch

The simulation is performed by shifting the transmission gate PMOS (PMOS1 in Fig. 15) horizontally D_2 . The irradiation point is always at the center of the PMOS1 drain region. Soft error does not occur at vertical hit and occurs in the range of $-1750 \text{ nm} < D_2 < 0 \text{ nm}$ at $\phi = 45^\circ$ hit.

C. PMOS transistors in different HCEs in the slave latch

The simulation is performed by shifting the transmission gate PMOS (PMOS1 in Fig. 16) horizontally D_3 . The irradiation point is always at the center of the PMOS1 drain region. Soft error occurs in the range of $-2200 \text{ nm} < D_2 < -750 \text{ nm}$ at $\phi = 45^\circ$ hit.

Figure 17 (a) shows a simplified block diagram of standard DICEFF as a reference. Figure 17 (b) shows a layout structure that improves soft error tolerance by separating inverters in slave latch. Figure 17 (c) shows layout that improves soft error tolerance by separating PMOS and NMOS transistors in I3, I4, I7 and I8. The sky blue arrows indicate a pair of transistors that is tolerant to soft errors up to Kr irradiation by device simulations. We designed a 6 different layout structures : 3 different well tap shapes for each of the 2 proposed layouts (DICEFF2 and DICEFF3). NG (No Guard ring) does not have a guard ring. The guard ring is an n+ diffusion layer or p+ diffusion layer path to absorb charge generated in the wells

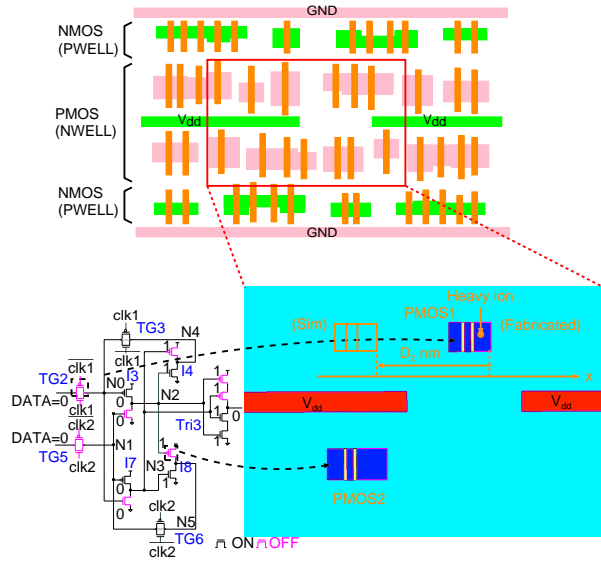


Fig. 15. Simplified layout structure, circuit diagram of the slave latch and top view of the 3D device model used horizontally separation at PMOS transistors in the transmission gate and the slave latch.

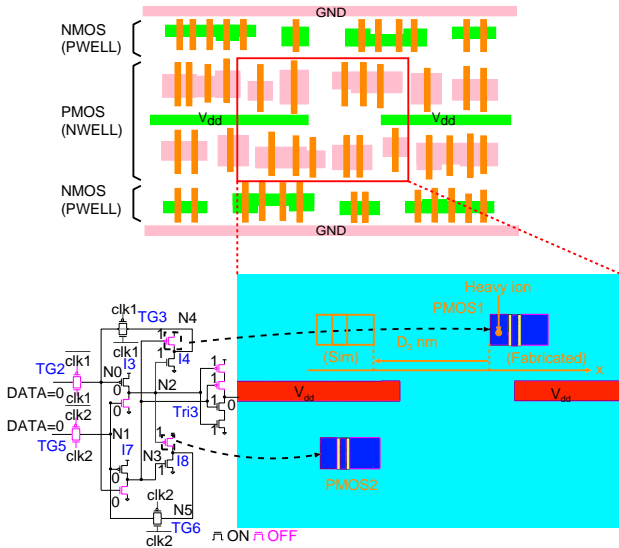
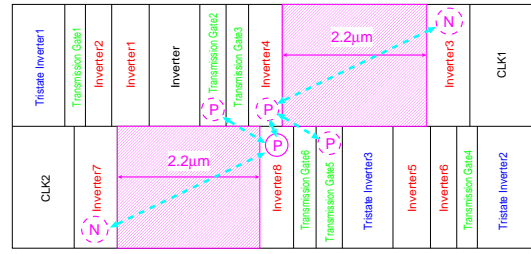


Fig. 16. Simplified layout structure, circuit diagram of the slave latch and top view of the 3D device model used horizontally separation at PMOS transistors in different HCEs in the slave latch.

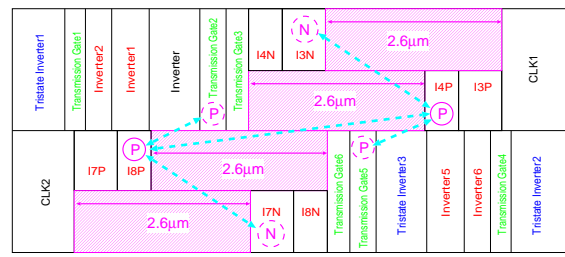
to V_{dd} or GND. It is effective for suppressing fluctuations in the substrate potential near the transistor. It is mainly for a countermeasure against latch-up, but it can also suppress the parasitic bipolar effect. PG (Partial Guard ring) has a separate guard ring only in the vertical direction. PG+ adds a well tap to the empty space in addition to PG. Figure 18 shows the layout structure of DICEFF3PG+. Table I shows the results of delay time, power consumption and area of the proposed DICEFFs considering parasitic components extracted from layout patterns by circuit simulations at V_{dd}=1.2 V. D-Q delay is the minimum delay time from D to Q including setup time before clock edge. All values are normalized to those of DICEFF1. The values in parentheses are normalized to those of DICEFF2NG. The power consumption of proposed FFs is 12-14% larger than that of DICEFF1. The delay time of



(a) DICEFF1 (standard)



(b) DICEFF2 (proposed1, NP combined)



(c) DICEFF3 (proposed2, NP separated)

Fig. 17. Simplified block of conventional and proposed layout structures.

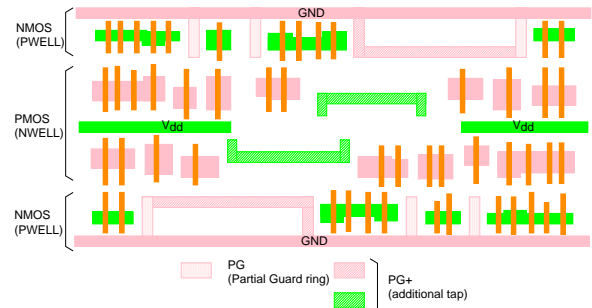


Fig. 18. Simplified layout structure of DICEFF3PG+ (Partial Guard ring + well tap in empty space).

proposed FFs is 15-16% longer than that of DICEFF1. The area of proposed FFs is 39-46% larger than that of DICEFF1. The overhead between the proposed FFs is less than 5%. We will measure soft error tolerance of those FFs this December.

V. Conclusion

We measured radiation tolerance of the DFF and DICEFF in the 65nm bulk process by heavy ions. In the experimental results, DICEFF has no error by Ar irradiation. DICEFF has 167x better soft error tolerance than DFF by Kr irradiation, but DICEFF has only 7x better soft error tolerance than DFF at (DATA, CLK) = (0, 0) while DICEFF has no error at the other three (DATA, CLK) states. We investigated the root cause of the low soft error tolerance at (DATA, CLK) = (0,

TABLE I

SIMULATION RESULTS OF AREA, D-Q DELAY, POWER AND NUMBER OF TRANSISTOR OF EACH FF AT $V_{dd} = 1.2$ V. ALL VALUES ARE NORMALIZED TO THOSE OF DICEFF1. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF DICEFF2NG.

FF	Power	D-Q delay	Area
DICEFF1	1.00	1.00	1.00
DICEFF2NG	1.12 (1.00)	1.15 (1.00)	1.39 (1.00)
DICEFF2PG	1.12 (1.00)	1.15 (1.00)	1.39 (1.00)
DICEFF2PG+	1.12 (1.00)	1.15 (1.00)	1.39 (1.00)
DICEFF3NG	1.14 (1.02)	1.15 (1.00)	1.46 (1.05)
DICEFF3PG	1.14 (1.02)	1.15 (1.00)	1.46 (1.05)
DICEFF3PG+	1.14 (1.02)	1.16 (1.01)	1.46 (1.05)

0) by device simulations. At NMOS and PMOS transistors in different HCEs in the slave latch, two nodes are upset simultaneously by a single heavy ion hit and then SEU occurs. At PMOS transistors in the transmission gate and the slave latch, no upset occurs at $\phi = 0^\circ$, but an upset occurs at $\phi = 45^\circ$. We also investigated the minimum distance that does not upset by Kr 45° hits by shifting transistors in the horizontal direction. No upset occurs by shifting critical transistors over $2\mu\text{m}$ but the area penalties are 39-46%. The distance is not scaled, which means area overhead becomes larger in more scaled process technologies. There are lots of pairs of transistors in DICEFF that must not upset at the same time. As technology downscaling, it becomes more difficult to keep all the distances between these transistors enough not to upset simultaneously. Therefore, a mitigation technique other than DICEFF is better in advanced scaled bulk processes.

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