LVDS Transmitter for Cold-Spare Systems in High Flux Environments

Takefumi Yoshikawa, Akihiro Aoyama, Tatsuya Iwata, Kazutoshi Kobayashi

***Abstract*— A high-bandwidth LVDS Transmitter (TX) has been proposed for redundant parallel connection of semiconductor devices in cold-spare systems. The cold-spare configuration is widely adopted for secure system operation of artificial satellite exposed to highly-radiated environment. For applying to the configuration in radiation hardened application, the LVDS-TX has i) off-chip driver consisting of only NMOS transistors to enhance latch-up immunity, ii) replica biasing for common mode voltage stabilization independently to off-chip loading, iii) multiple guard ring between large NMOS and N-Well areas. The proposed LVDS-TX has been fabricated by using bulk I/O and SOI core transistors in a 65 nm FDSOI process. Measurement results show over-500Mbit/sec stable data communication, and remarkable suppression of BER (Bit Error Rate) degradation compared to commercial device under $^{84}Kr^{17+}$ exposure of 322.0 MeV at flux of over $5x10^5$ count/cm^2/s.**

***Index Terms*— LVDS, transmitter, cold-spare system, radiation hardened, latch-up**

I. Introduction

HIGH speed interface technologies are utilized in advanced semiconductor devices to reduce pin count with high data bandwidth. As high speed interface, Low-Voltage-Differential-Signaling (LVDS) topology is famous and widely used in various applications because of the IEEE standard [1]. Recently, it has been applied to data transmission on systems in radiation rich environments [2, 3]. On the other hand, in such environment, cold-spare configuration is adopted to secure continuous system operation in system level. As depicted in Figure 1, redundant devices both of transmitter (TX) and receiver (RX) are prepared and parallelly connected through data bus each other.

In TX and RX, one device is activated respectively by powering their VDD. Others are in sleep state as cold devices with high impedance of I/O pins by disabling their VDD to around 0 V. When an active device is damaged by radiation exposure, the damaged device is disabled via shutting down its VDD. Consequently, one of cold devices is enabled through powering its VDD and starts to work instead of the damaged device. This redundant configuration achieves continuous system operation and enhances reliability remarkably.

To apply LVDS interface to the cold-spare system in radiation-rich environment, LVDS-TX macro in devices should comply

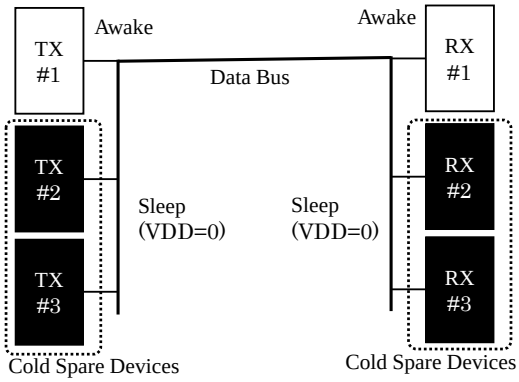

Figure 1. Cold Spare Configuration

radiation-hardened specific requirement.

Firstly, I/O pin should be high impedance during non-powered condition, then p^+ diffusion is not allowed to avoid forward biasing on non-powered N-well. Hence, PMOS transistor of output node in off-chip driver [2] can not be used in the cold-spare system. Moreover, an occurrence of latch-up in CMOS devices during normal operation must be minimal as much as possible even in cold-spare systems due to limited number of preparing devices. Normal LVDS-TX has both of large PMOS and NMOS in off-chip driver [2-4], but it may cause multiple Single Event Latch-up (SEL) in high flux environments [5].

Secondly, stable output common voltage (V_{cm}) on TX output should be guaranteed even in the cold-spare system configuration. For controlling the V_{cm} value to target voltage, common mode feedback is applied on off-chip driver [2-4,6]. However, the pole-zero compensation network of the feed-back topology becomes difficult to be configured at the cold-spare system. Because the number of parallel devices in the system is not fixed until actual implementation of the system board. Therefore, V_{cm} should be set independently to number of connected cold devices in LVDS-TX.

Lastly, off-chip driver has large NMOS transistors, i.e. large grounded n^+ diffusion exists in the driver area. Therefore, proper attention should paid to geometrical layout to avoid base-current generation on lateral parasitic bipolar transistor.

In this paper, we explicitly analyze circuit configuration of

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LVDS-TX for the cold-spare system. In section II, data driver and its bias control circuits are proposed in LVDS-TX. In this section, layout consideration is also delivered. Then, a test-chip implementation and actual measurement results of heavy-ion condition are described in Section III. In association with the measurement results, discussions are provided with showing simulation results in Section IV. Finally, the conclusion is drawn in section V.

II. Circuit Design

The LVDS-TX is designed using both of Thin-BOX FDSOI transistor (core transistor) and 3.3V bulk transistor (I/O transistor) in a 65 nm process. Almost all circuits including the off-chip driver are configured by I/O bulk transistors of PMOS and NMOS and operate in 3.3V typical VDD condition. FDSOI transistors of 1.2 V VDD are used just in signal input and level shifter to covert input signals from 1.2 V to 3.3 V swing. This section states the off-chip driver and its related circuits, which are operable in 3.3 V.

A. Driver Design

Fig. 2 represents a driver circuit of the proposed LVDS-TX. As depicted in the figure, the driver and ESD protection diodes (not illustrated) are configured by only NMOS transistors. Therefore, output nodes (OUTP/OUTN) are connected only to n+ diffusion of the NMOS transistors

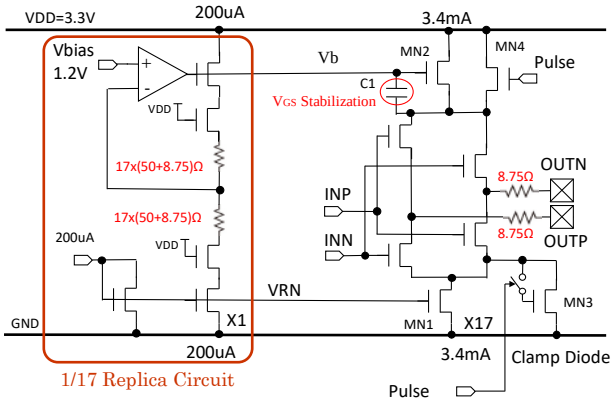

Figure 2. Driver Circuit

This configuration achieves i) pull-up biasing at off-chip output nodes because of only n+ diffusion, ii) much enhancement to latch-up tolerance because of only NMOS structure in I/O stage.

In the driver, source follower large NMOS (MN2) should work as constant current source similarly as MN1. For this purpose, relatively large capacitor (C1) is placed between its gate and source node for keeping the V_{GS} to be constant.

For pre-emphasis capability, extra NMOS (MN3, MN4) are allocated in parallel to main current sources (MN1, MN2).

Series resisters of 8.75 Ω on output nodes (OUTP/OUTN) are for enhancement ESD protection. The output common voltage level (V_{cm}) is set by control voltage (V_b) to the source-follower NMOS (MN2).

B. Replica Biasing

As depicted in left side of Fig. 2, the control voltage (V_b) for V_{cm} settlement is generated in a Replica Circuit. This Replica circuit is miniature of 1/17 for output driving system including off-chip driver, series register (8.75 Ω) and load resister (100 Ω) at receiver side (not illustrated). A bias current is also $1/17^{th}$ for driving current of 3.4 mA.

This biasing by the Replica Circuit configures feed-forward (not feedback) topology, and the common mode voltage (V_{cm}) can be set independently to output load capacitance in the cold-spare system. Therefore, system designers do not have to consider any complicated pole-zero network regardless of the number of device parallelism.

C. Layout

In layout of the LVDS-TX macro, multiple guard rings are applied on P^- substrate between large N^+ diffusion and N-Well area in the vicinity of the off-chip driver.

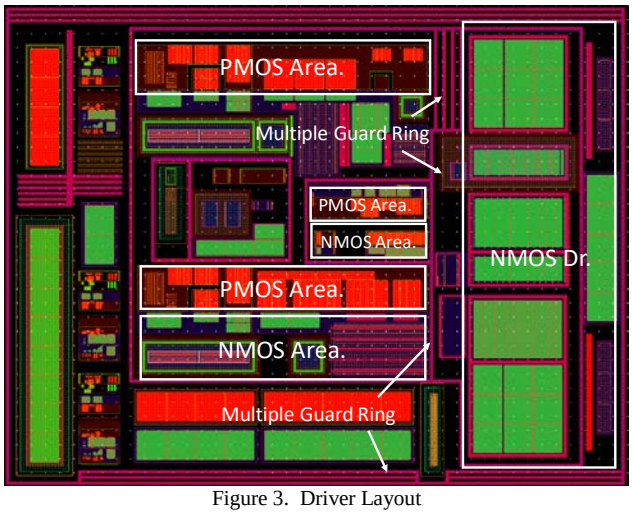

Figure 3. Driver Layout

III. Test-Chip and Measurement Results

A. Test Chip Implementation

A test-chip has been fabricated in a 65 nm process with bulk I/O and FDSOI core transistors. Layout and photo of the test-chip are shown in Fig. 3. The size of the test-chip is 1.5 mm x 2 mm. The test-chip has been assembled in a 64pin LQFP package.

B. BER Measurement under Normal Condition

To configure the cold-spare system emulation, 4 test boards are prepared and connected through 35.4 ” and 5.9 ” coaxial cables and SMA connectors as shown in Fig. 4. Then, a pair of TX and RX board are activated (Power-On) and others board are disabled as cold-spare devices. To measure Bit Error Rate (BER), Bit Error Rate Tester (BERT) is connected to active boards of TX and RX. Test data are fed to active TX from BERT and receive data of active RX are returned to BERT as comparison target. Fig. 5 depicts actual BER measurement results in various VDD of I/O transistor (VDD3) using test environments of Fig. 5 in high temperature environment (70 °C).

C. BER Measurement under Heavy Ion Exposure Condition

Fig. 6 shows a measurement board for BER and an equipment for heavy ion exposure condition. In both commercial TX and test devices, mold resin and passivation film are removed for direct ion impact to silicon chip.

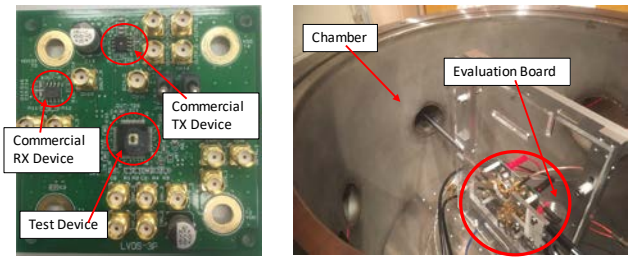

Figure 6. Measurement Board and Equipment

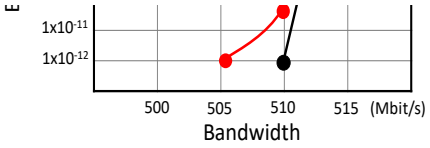

Figure 5. BER Measurement Results

In the chamber, ion beam can be focused with spot size of 20 mm in diameter. The BER measurement was performed under following conditions.

- Heavy Ion : $^{84}Kr^{17+}$
- Dose Energy : 322.0MeV
- 1 minute exposure, then measure BER
- 200Mbit/sec data rate to focus radiation tolerance

Measurement facility was heavy ion exposure system in Cyclotron and Radioisotope Center (CYRIC), Tohoku University, JAPAN.

Initially, BER was measured w/o any exposure in order to show $1x10^{-12}$ BER (No Error). Then, heavy ions are irradiated to the target device for 1minute with various flux count.

Table 1 and 2 show BER measurement results of commercial and fabricated test devices respectively. As shown these tables, the commercial device did not cause any bit error until $1.0x10^4$ flux condition. However, a bit error occurred in 3.2 $x10^4$ flux condition and the error rate reaches 10^{-2} order. The BER was not decreased even after stopping the ion exposure due to no toggle of signal output from the device. The device recovered after power off and on sequence. It means latch-up occurred by the heavy ion exposure.

In contrast, the test device showed small bit error of $3x10^{-12}$ under 1.0 $x10^4$ flux count. However, the bit error was always sporadic even in 5.0 $x10^5$ flux condition, and the BER was decreased after stopping the ion exposure in all flux condition.

Fig. 7 shows an exponential approximation curve of BER and flux count. The test device shows remarkable suppression of BER degradation in high flux environment, i.e. 10^{-10} order BER under condition of over 10 times flux count compare to the commercial device at 10^{-2} order BER.

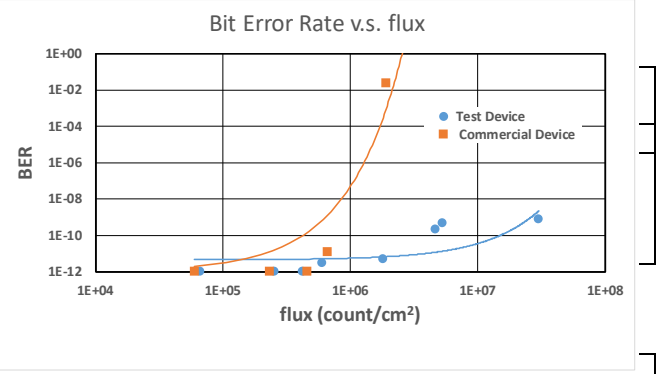

Figure 7. BER v.s. flux count

7.0 $x10^3$	No Error
<3.0 $x10^4$	BER=3.0 $x10^{-12}$, **BER decreased** after exposure termination
<7.7 $x10^4$	BER=2.2 $x10^{-10}$ order error, **BER decreased** after exposure termination
<8.8 $x10^4$	BER=4.5 $x10^{-10}$ order error, **BER decreased** after exposure termination
<5.0 $x10^5$	BER=8.0 $x10^{-10}$, **BER decreased** after exposure termination

IV. Discussion

Though the test device shows remarkable suppression of BER degradation, sporadic bit errors are occurred even in <1.0 $x10^4$ flux condition. The most likely cause of the bit error is in level

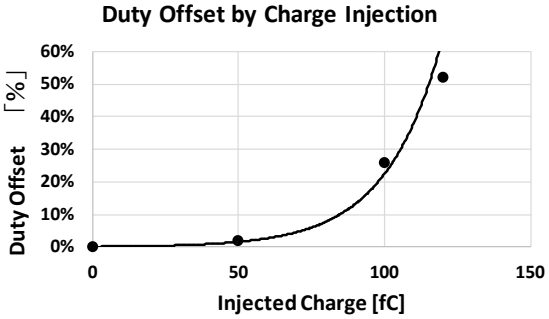

Figure 10. Simulation Results of Duty Cycle Fluctuation by Charge Injection

shifter, which is for level conversion from 1.2 V to 3.3 V. In the commercial device, no level shifter exists because of shingle 3.3 V power supply. Fig. 8 depicts simplified circuit schematic of level shifter of the TX. As shown in the figure, cross-coupled transistors are used for level conversion and signal generation of true/complement outputs, and core transistors of NMOS (SOTB NMOS) are adopted for bandwidth enhancement.

To protect the NMOS from excessive voltage, I/O transistors of NMOS are used with source follower topology. The gate voltages of the source follower NMOS are connected to Vref, which is controlled to target voltage by resister and bias current.

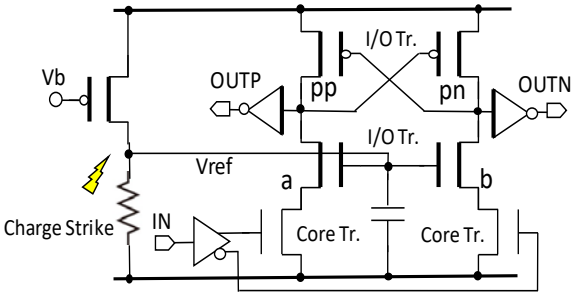

Figure 8. Level Shifter Circuit

Similar to SRAM cell, SET (Single Event Transient) pulses would be caused by charge injection due to heavy ion exposure of $^{84}Kr^{17+}$ (LET: 40 MeV·cm2/mg).

The charge injection is converted to time-transient current source by following equation, and the current source is used in circuit simulation.

$$I(t) = \frac{2Q}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}e^{-\frac{t}{T}}$$

As for T in the equation, we set T=20 ps considering Lg=0.35 um technology with reference of [7].

According to an intensive sensitivity analysis of the level shifter, Vref is the most sensitive node to the charge injection for output duty cycle fluctuation. Fig. 9 shows simulation results with the charge injection of 50fC, 100fC and 120fC onto Vref. The Charge injection causes Vref distortion, then duty offset occurs on differential output of OUTP/OUTN.

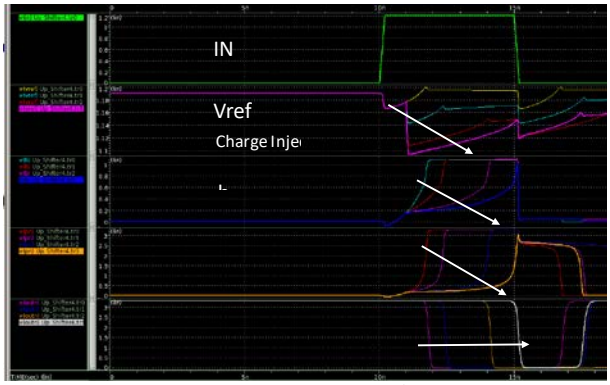

Figure 9. Simulation Waveforms

The duty offset is depicted in Fig.10, and increased rapidly at charge injection of around 100fC. The sporadic bit errors would be caused by timing margin reduction due to the duty offset, and re-design of the level shifter to remove high-impedance gate node on source follower transistors is next subject for further BER improvement.

V. Conclusion

We propose LVDS transmitter (TX) for cold-spare system to improve reliability in high flux environment of heavy ions. The proposed LVDS-TX has a unique off-chip driver and output voltage level adjustment with multiple guard rings. The test device shows over-500 Mbit/sec data bandwidth and remarkable suppression of BER degradation at 10 times higher flux condition compared to commercial device. The adaptability of the proposed LVDS-TX makes sure better communication performances in high flux environments.

Acknowledgment

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