Measuring SER by Neutron Irradiation Between Volatile SRAM-based and Nonvolatile Flash-based FPGAs

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***Abstract*— We implemented 50k-bit shift registers on SRAM-based and flash-based FPGAs to investigate their radiation hardness. As a result, soft error rates of flip flops on both FPGAs are around 40 FIT/Mbit. Mean time to failure (MTTF) in the SRAM-based one is 3.8 $\times$ 10^7 hour/failure, while MTTF in flash-based one is 5.5 $\times$ 10^9 hour/failure. Those results clearly show that in the SRAM-based FPGA must be rebooted or configuration memory must be refreshed much more frequently than the flash-based one.**

I. Introduction

Recently, the soft error becomes a significant issue to decrease reliability of electronic equipments due to downsizing of semiconductor chips. It is a phenomenon that a stored value in flip flops (FFs) or SRAMs upset by radiation effects. High energy neutrons from sky is one of the causes. In the JESD 89A standard, neutrons produced by cosmic ray impact on atomic with energy of more than 10 MeV is dominant to cause soft errors.

In the field programmable gate array (FPGA), the soft error is much more critical than application specific integrated circuit (ASIC) chips [1]. Since a configured circuit is volatile in the most frequency-used SRAM-based FPGAs. Once a configured circuit in FPGA mulfunctions due to soft errors, FPGA must reboot to refresh its configuration memory.

The reliability is compared about the difference of technology node, operating temperature and voltage [2][3]. In addition, many kind of energies particles are irradiated to FPGA to investigate its reliability [4]. The reliability of FPGAs is measured in different technology nodes, operating temperature, voltage and particle.

In this paper, we measured soft error rate (SER) in FFs and mean time to failure (MTTF) rates of SRAM-based and flash-based FPGAs. These FPGAs are introduced in Section II. Section III describes configured circuit structures for neutron irradiation and measurement setups. Section IV shows experimental results and discussions. Finally, Section V concludes this paper.

II. Volatile SRAM-based FPGA and nonvolatile flash-based FPGA

We compared radiation tolerance between volatile SRAM-based and nonvolatile flash-based FPGAs as shown in Table I. The SRAM-based FPGA was fabricated in a 28 nm technology node and its standard operating voltage is 1.0 V. It contains 65,200 FFs on a chip. The configuration memory consists of SRAM. A configured circuit is vanished after turning off and then it must be restored from an external nonvolatile memory on a PC.

The nonvolatile flash-based FPGA was fabricated in a 28 nm Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) technology. SONOS is usually used to integrate flash memory in standard ASICs. Once it is configured, a configured circuit is not erased even after turning off. The configured circuit can instantly operate after turning on. Its standard operating voltage is 1.0 V. It embeds 300,000 FFs on a chip.

TABLE I
FEATURES OF TWO TYPES OF FPGA.

FPGA	SRAM-based (XC7S50-1CSGA324C)	Nonvolatile (MPF300TS-1FCG-484)
Technology node	28 nm	28 nm SONOS
Configuration memory	SRAM	flash memory
Operating voltage	1.0 V	1.0 V
FFs	65.2k	300k

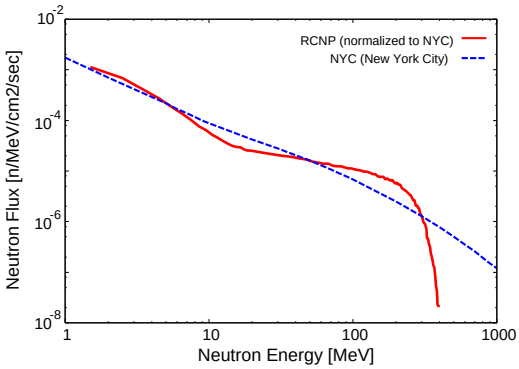

Fig. 1. Normalized energy spectrum of spallation neutron beam at RCNP and neutron at the sea level of NewYork City.

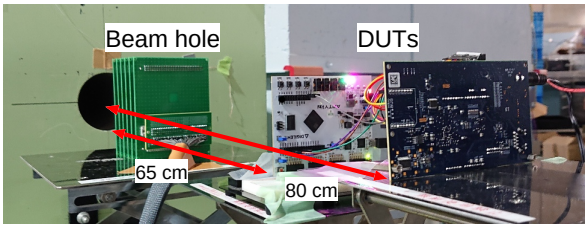

Fig. 2. Experimental setup for neutron beam irradiation.

III. Experimental Setup

We conducted neutron spallation irradiation tests at Research Center for Nuclear Physics, Osaka University (RCNP) [5]. Figure 1 shows the normalized neutron beam spectrum in comparison with the terrestrial neutron spectrum at the sea level in New York City (NYC). The average acceleration factor (AF) during our measurement is 4.17 $\times$ 10^8 in average compared with the sea level in NYC.

Figure 2 shows the measurement setup. An SRAM-based FPGA board was placed at 60 cm far apart from the beam hole and a flash-based FPGA was placed at 85 cm from the

TABLE II

TOTAL IRRADIATION TIME FOR EACH INTERVAL BETWEEN SHIFT READ & WRITE OPERATION TO SHIFT REGISTER.

Irradiation time [min]	Number of measurements	Subtotal time [min]
0.5	227	113.5
1	95	95
2	118	236
3	67	236
5	21	105
10	21	210
Total irradiation Time [min]		960.5

TABLE III

NUMBER OF ERRORS IN SRAM-BASED FPGA.

Shift Interval [min]	Stuck-at 0 [%]	Stuck-at 1 [%]	Repeating Burst Error [%]	Error Probability [%]
0.5	16 (7.05)	15 (6.61)	5 (2.20)	15.9
1	5 (5.26)	3 (3.16)	3 (3.16)	11.6
2	13 (11.0)	12 (10.1)	11 (9.32)	30.5
3	18 (26.9)	10 (14.9)	6 (8.96)	50.8
5	7 (33.3)	4 (19.0)	1 (4.76)	57.1
10	12 (57.1)	6 (28.6)	2 (9.52)	95.3

beam hole.

Figure 3 depicts the whole measurement setup. Those two FPGA boards are configured by the PC. Input signals are generated by the signal generator and the logic analyzer captures output signals. When a configured circuit mulfunctions, the outlet box controlled by the PC turns off and on the power supply of each FPGA board. The USB interface on the PC is extended by the two USB extenders connected through the CAT5 cable. The PC is placed in the observation room outside of the measurement room to protect it from soft errors.

50,000 bit shift registers are configured to the two FPGAs. In case of the volatile SRAM-based FPGA, configuration is stored in nonvolatile flash memory on the measurement board. In case of the nonvolatile flash-based FPGA, configuration is stored in an embedded flash memory. No configuration upset was observed on the nonvolatile flash-based FPGA. We assumed that the external flash memory for the SRAM-based FPGA is also strong against soft errors [6]. Furthermore, these FPGAs are automatically reconfigured after turning on. In the flash-based FPGA, configuration is nonvolatile. However, if a configured circuit mulfunctions, configuration memory must be refreshed.

The configured shift registers are periodically shifted through the PC to see soft errors in FFs because the possibility to cause multiple errors in a short period is very low and upsets in a configuration memory becomes dominant as measurement period becomes long. If errors besides an SBU is happened, it is regarded as an error occurring outside of the FFs in the shift register. Measurement is conducted as the following procedure.

1) Initialize the shift registers with a checker board pattern, in which stored data is flipped every 500 bit.
2) Read out the shift registers through the logic analyzer.
3) Repeat 1)-3).

Table II shows irradiation time for each interval between shift operation.

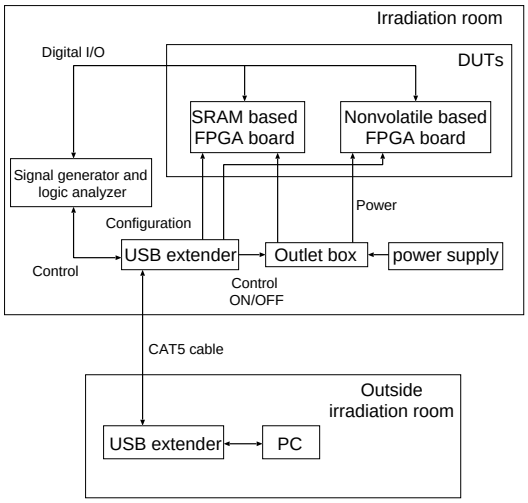

Fig. 3. Block diagram of the measurement setup at RCNP.

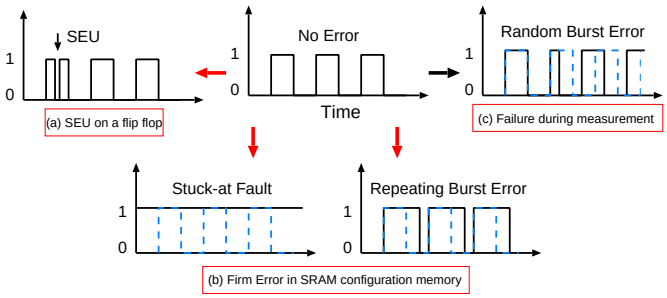

Fig. 4. Measured error patterns.

IV. Measurement Results

Figure 4 shows typical measured error patterns. We observed four anomalous patterns. Figure 4 (a) is when an SBU happens in a FF in the shift register. Figure 4 (b) depicts two error patterns that cannot be fixed without reconfiguration. We call those errors firm errors. The left one is so-called stuck-at fault at which output data is fixed to 0 or 1. In the right one, the length of continuous 1 prolongs to a specific period every time the stored data is read out. It is called a repeating burst error. We regarded these two patterns are caused by errors in a configuration memory. The pattern in Fig. 4 (c) is fully random, which is considered as errors in the signal generator or in the logic analyzer. The stuck-at fault can be happened if the input of a FF in the shift registers is mis-connected by a bit flip in a configuration memory.

Firm errors cannot be fixed until correct configuration data is loaded to the FPGAs. Table III shows the number of errors categorized to the firm errors in Fig. 4 (b). In each condition, the stuck-at 0 is the major error pattern. The number of firm errors increases in proportion to the measurement time. In order to improve the tolerance of SRAM-based FPGA, error correction code (ECC) must be adopted to correct SBU on configuration memory and errorneous configuration data.

We use MTTF (mean time to failure) to figure out how long those FPGAs are able to keep on running without refreshing their configuration in the terrestical region. Equation 1 is used to calculate MTTF.

TABLE IV

COMPARISON CS OF CRAM BETWEEN OUR MEASUREMENT RESULT AND MANUFACTURER MEASUREMENT RESULT

	Configuration memory	CS [/bit]
Our measurement results (static)	Volatile-SRAM	$6.68\times\ 10^{-15}$
	Nonvolatile	0
Vendor's test results (dynamic) [7]	Volatile-SRAM	$6.99\times\ 10^{-15}\pm 18\%$

TABLE V

NUMBER OF SBUS IN FFS ON EACH FPGA.

Measurement Time (min)	SBU	
	SRAM-based	Flash-based
0.5	0	0
1	2	1
2	3	3
3	1	3
5	0	1
10	0	1

TABLE VI

COMPARISON OF SERS OF FFS BETWEEN OUR MEASUREMENT RESULTS AND VENDOR'S MEASUREMENT RESULTS

	Configuration memory	SER [FIT/Mbit]
Our measurement results (static)	Volatile-SRAM	28.2
	Nonvolatile	34.5
Vendor's test results (dynamic) [8]	Nonvolatile	460
Vendor's test results (dynamic,slowed-down) [8]	Nonvolatile	230

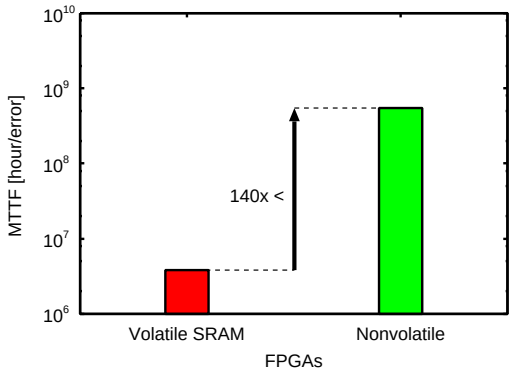

Fig. 5. MTTF of CRAM in each FPGA.

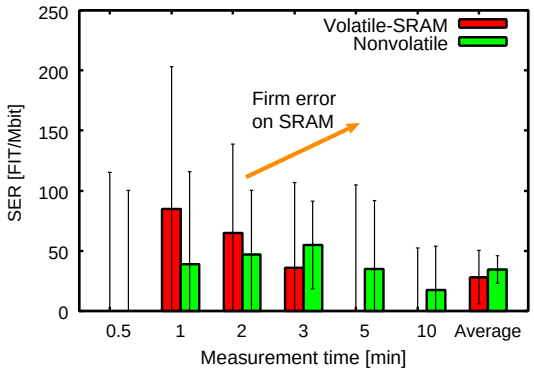

Fig. 6. Experimental results of neutron-induced SER and averaged SER of two type FPGAs.The error bars are within 95.4% confidence intervals.

$$MTTF\ [\text{Failure/hour}] = \frac{N_{\text{error}} \times AF}{t_{\text{mt}}} \tag{1}$$

MTTF is calculated from the number of errors (N_{error}), AF and the total measurement time (t_{mt}). AF is taken into account the attenuation the distance of each FPGA board from the beam hole.

Figure 5 compares MTTF of both FPGAs. No error besides SBU was observed in the flash-based FPGA. MTTF of the flash-based FPGA is calculated from the assumption that only an error was observed throughout the measurement.

MTTF of the SRAM-based FPGA is $3.8\ \times\ 10^7$ hour/failure, while that of the flash-based FPGA is $5.5\ \times\ 10^9$ hour/failure. The tolerance of flash-based FPGA is 140x stronger than that of the SRAM-based one. A memory cell in the SONOS structure must be erased or written by higher voltage than the nominal voltage of 1 V. In contrast, an SRAM cell can be flipped easily by generated charge by secondary particles from a neutron hit.

Table IV shows the cross sections (CS) of our measurement results and vendor's results. Equation 2 is used in order to calculate CS.

$$CS\ [/\text{bit}] = \frac{N_{\text{error}}}{N_{\text{bit}} \times AF \times t_{\text{mt}}} \tag{2}$$

CS is calculated from the number of errors (N_{error}), the number of essential bits (N_{bit}), AF and the total measurement time (t_{mt}). The essential bit defined here is the number of bits in the configuration memory associated with the circuitry of the design. If an essential bit is upset, the configured circuitry is changed. However, the upset does not always affect the functionality of the design [9].

According to Xilinx Device Reliability Report, CS of CRAM is $6.99\times\ 10^{-15}\pm 18\%$ per bit [7]. CS of the nonvolatile FPGA from the measurement was no error. The number of the essential bits for the shift register is 3,326,260 bits and the CS of the SRAM-based one from the measurement results is $6.68\times\ 10^{-15}$ per bit. The number of the essential CRAM bits is calculated by the VIVADO tool from Xilinx. Our measurement result is within error bar of the vendor's one. To improve CRAM cross section needs to use ECC scrubbing CRAM periodically.

Table V shows the number of SBUs in FFs on each FPGA. Only a few SBUs were observed in each measurement. Equation 3 is used in order to calculate SER.

$$SER\ [\text{FIT/Mbit}] = \frac{N_{\text{error}} \times 10^9 \times 1024^2}{t/60 \times AF \times N_{\text{FF}}} \tag{3}$$

SER is calculated from the number of errors (N_{error}), the measurement time in minutes (t), AF and the number of FFs (N_{FF}).

Figure 6 shows neutron-induced SERs according to the irradiation time. The averaged SER of both FPGAs are almost equivalent within the error bars.

Table VI shows difference of SERs between our results and vendor's results. According to the Microsemi test reports [8], the averaged SERs of FFs on the nonvolatile FPGA are 460 FIT/Mbit and 230 FIT/Mbit under a checkerboard pattern and slowed-down checkerboard pattern. However, they measured a 4,000-bit shift register chain compared the output and a golden

functional model on a master chip operating by 10 MHz. On the other hand, our our shift register includes 50,000 bit and its FIT rate is 34 FIT/Mbit.

This discrepancy is caused by the difference of measurement conditions. They measured dynamically, while we measured statically. Dynamic measurement observes more errors than static measurement. The dynamic measurement is susceptible to an SET pulse because a clock signal and FFs are dynamically working. Whereas, in the static test a clock signal and FFs only work during shift operations to initialize and read flipped bits. From the above reasons, it seems that there was a difference of one magnitude among the measurement results.

To improve soft error tolerance of FFs it is mandatory to equip radiation-hardened FFs or to implement a redundant circuit [10].

V. Conclusion

We compared radiation tolerance between the volatile SRAM-based and nonvolatile flash-based FPGAs by neutron irradiation. The SER of FFs is almost equivalent regardless of the type of configuration memory. This is because that FFs on both FPGAs do not have a radiation-hardened structure. The MTTF of the flash-based FPGA is at least 140x longer than that of the SRAM-based one.

The simple circuit like the shift register is hard to flip by a neutron strike even if the essential bit is flipped. The flash-based FPGA can keep on running without reconfiguration for a long time in the terrestrial region, while the SRAM-based one must be rebooted frequently to refresh its configuration memory. It is because the radiation tolerance of the SONOS structure used in the flash-based FPGA is stronger than SRAM. To mitigate SBUs on a configuration memory of SRAM-based FPGAs, periodic reconfiguration is mandatory or an SBU on configuration memory must be corrected by ECC provided by Soft-Error Mitigation (SEM) core [11].

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