# Evaluation of Soft-Error Tolerance by Neutrons and Heavy Ions on Flip Flops with Guard Gates in a 65 nm Thin BOX FDSOI Process

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***Abstract*— We evaluated soft-error tolerance by neutrons and heavy ions on four types of flip flops (FFs) called transmission-gate FF (TGFF), guard-gate FF (GGFF), feedback recovery FF (FRFF) and dual FRFF (DFRFF) in a 65nm thin BOX FDSOI. FRFF has a guard-gate structure only in the master latch. GGFF and DFRFF have the guard-gate structure in both of master and slave latches. The guard-gate structure resolves an SET pulse by delaying it through the guard gate. FRFF and DFRFF have smaller area and shorter delay overheads than GGFF. We revealed that the guard-gate structure has high soft-error tolerance by low-LET heavy ions, but the larger-LET ions over 40 MeV-cm$^2$/mg cause upset even in the guard-gate structures. We revealed that longer delay in the guard-gate can resolve these issues by circuit simulations.**

## I. Introduction

Reliability issues have become a significant concern due to soft errors with technology downscaling [1]. Soft errors are one of temporal failures that flip stored values in storage elements such as flip flops (FFs) or SRAMs by neutrons and heavy ions from cosmic rays. When a radiated particle hits transistors, the perturbation in the output node voltage is generated ,which is called a single event transient (SET) pulse. A SET pulse will cause a single event upset (SEU).

In the device level, fully-depleted silicon on insulator (FDSOI) processes have 50-100x higher soft-error tolerance than conventional bulk processes without any performance overhead. It is because the buried oxide (BOX) layer prevents charge from being collected from substrate [2]. In the circuit level, several redundant FFs such as triple modular redundancy (TMR) [3] and dual interlocked storage cell (DICE) [4][5] have been proposed for effective countermeasures. However, they have longer delay time, larger area and power consumption than conventional standard FFs. Therefore, FFs with lower overhead and higher radiation hardness must be required. A stacked FF in [6] was proposed as one of non-redundant FFs. It has high soft-error tolerance, smaller area and power consumption compared with redundant FFs. However, even the stacked FF has longer delay time, larger area and power consumption than conventional standard FFs.

In this paper, we measured radiation tolerance of several FFs including conventional and proposed FFs.

We explain several types of radiation-hard flip flops evaluated soft-error tolerance in a 65 nm FDSOI process in Section Ⅱ. Section Ⅲ explains experimental setups. Section Ⅳ explains experimental results by neutrons and heavy-ion irradiation and discussion. We conclude this paper in Section V.

## II. Flip Flops to evaluate soft-error tolerance

### Standard Transmission-Gate Flip Flop

Figure 1 shows a standard FF called the transmission-gate FF (TGFF). It has no tolerance against soft errors.

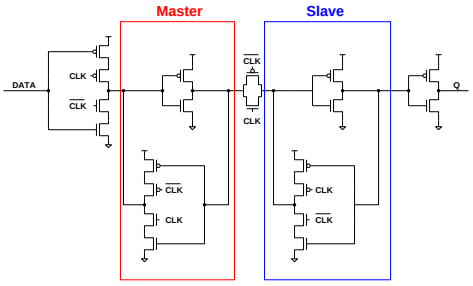



Fig. 1. Transmission-gate flip flop (TGFF)

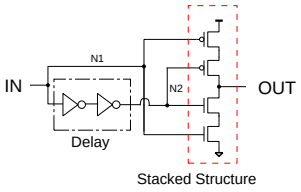



Fig. 2. Guard-gate structure

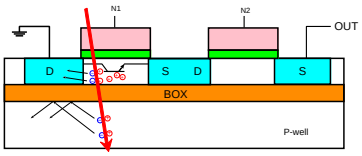



Fig. 3. Stacked structure to suppress a simultaneous upset of the series-connected structure

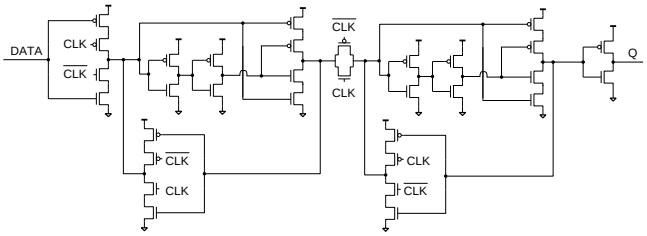



Fig. 4. Gurad-gate flip flop (GGFF)

### Guard-Gate FF

Figure 2 shows the guard-gate structure that consists of a delay element including two inverters and a C-element [7]. The guard gate eliminates all SET pulses which are shorter than the delay of two inverters since one input in the C-element is delayed. When two input values are different, the C-element keeps a previous correct input value. The C-element is intrinsically composed of the stacked structure that is strong against soft errors in the SOI process. Series-connected stacked NMOS and PMOS transistors (Fig. 3) are rarely flipped at the same time because their body layers are fully separated by diffusion and the BOX layer [6]. Therefore, the probability of SET pulses from the C-element becomes smaller.

Figure 4 shows the guard-gate FF (GGFF) [8]. GGFF has the guard-gate structure in the master and slave latches to prevent an SEU. However, it has larger area and delay overheads than standard FFs because 12 more transistors are added to TGFF.

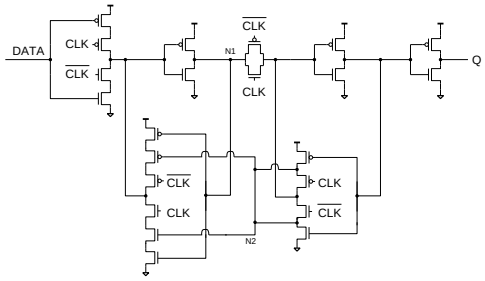



Fig. 5. Feedback recovery flip flop (FRFF)

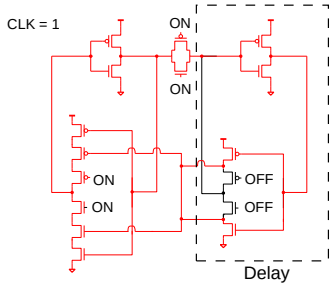



Fig. 6. Latch state at CLK = 1

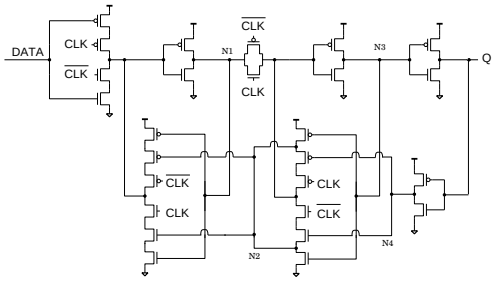



Fig. 7. Dual feedback recovery flip flop (DFRFF)

### Feedback Recovery FF

Figure 5 shows the feedback recovery flip flop (FRFF) composed of two more inverters than TGFF [9]. FRFF has high soft-error tolerance only in the master latch because it embeds the guard-gate structure only in the master latch. Figure 6 shows the latch state at CLK = 1 when the slave latch works as a delay element.

### Dual FRFF

Figure 7 shows the dual feedback recovery flip flop (DFRFF) composed of four more inverters than TGFF [9]. DFRFF has high soft-error tolerance in both of the master and slave latches because the guard-gate structure is also embedded in the slave latch. In the slave latch, the output inverter and the feedback inverter work as the delay element of the guard-gate structure.

Table I shows the results of delay time, power consumption at 10% data activity and area of TGFF, GGFF, FRFF and DFRFF using circuit simulations at supply voltage ($V_{\rm dd}$) = 1.2 V quoted from [9]. The results include parasitic resistance and capacitance. D-Q delay is the time taken from D to Q in a FF. All values are normalized to those of TGFF. The values in parentheses are normalized to those of GGFF. The delay time and the area of GGFF are 2.2x longer and 1.4x bigger than those of TGFF, but the delay time and the area of FRFF are 52% shorter and 28% smaller than those of GGFF. The delay time and the area of DFRFF are 51% shorter and 20% smaller than those of GGFF.

TABLE I

SIMULATION RESULTS OF AREA, D-Q DELAY, POWER AND NUMBER OF TRANSISTOR OF EACH FF AT $V_{\rm DD}$= 1.2 V. ALL VALUES ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF GGFF [9].

| FF | D-Q delay | Area | Power | # of Tr. |
|---|---|---|---|---|
| TGFF | 1 | 1 | 1 | 24 |
| GGFF | 2.20 (1) | 1.47 (1) | 1.06 (1) | 36 |
| FRFF | 1.06 (0.48) | 1.06 (0.72) | 1.03 (0.97) | 26 |
| DFRFF | 1.08 (0.49) | 1.18 (0.80) | 1.02 (0.96) | 30 |

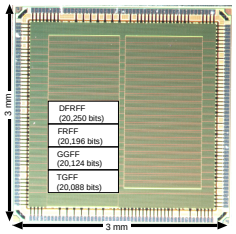



Fig. 8. Chip micrograph that contains 20,088 bit standard TGFFs, 20,124 bit GGFFs, 20,196 bit FRFFs and 20,250 bit DFRFFs.

## III. Experimental Setup

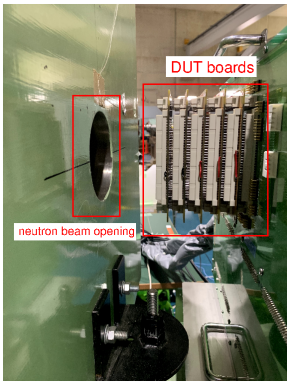
A test chip was fabricated in a 65 nm thin BOX FDSOI process in order to evaluate soft-error tolerance [10]. Figure 8 shows the chip micrograph that contains 20,088 bit standard TGFFs, 20,124 bit GGFFs, 20,196 bit FRFFs and 20,250 bit DFRFFs. All FFs are connected in series to form a shift register. We evaluated soft-error tolerance by neutrons and heavy ions.

Spallation neutron tests were conducted at the research center for nuclear physics (RCNP), Osaka University, Japan [8]. Figure 9 (a) shows the experimental setup of neutron irradiation tests. Figure 10 shows the normalized neutron beam spectrum in comparison with the terrestrial neutron spectrum at the sea level in New York City (NYC). The average acceleration factor (AF) is $3.77 \times 10^8$ compared with the sea level in NYC. In order to increase the number of upset FFs within a limited time, five stacked DUT boards each of which includes two test chips were exposed to the neutron beam. As a result, 10 chips were measured simultaneously. Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). $V_{\rm dd}$ was 0.6 V at neutron irradiation and stored values were shifted every 300 second. Soft-error rates (SERs) are calculated using Eq. (1).

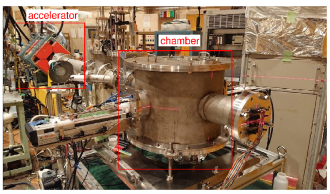
$$SER\ [\mathrm{FIT/Mbit}] = \frac{N_{\rm error} \times 10^9\ \mathrm{h} \times 1024^2\ \mathrm{bit}}{300\ \mathrm{sec}/3600\ \mathrm{sec} \times AF \times N_{\rm FF}} \quad (1)$$

$N_{\rm error}$ is the number of errors, and $N_{\rm FF}$ is the number of FFs.

Heavy-ion irradiation tests were conducted by Ar and Kr at Cyclotron and Radioisotope Center (CYRIC), Tohoku University, Japan. Figure 9 (b) shows the experimental setup of the heavy-ion irradiation tests. Device under tests (DUTs)




(a) Neutron irradiation setup.




(b) Heavy-ion irradiation setup.

Fig. 9. Measurement setup.

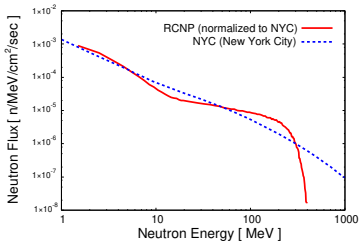



Fig. 10. Normalized energy spectrum of spallation neutron beam at RCNP and neutron at the sea level of NYC.

TABLE II
LET, ENERGY AND FLUENCE OF HEAVY IONS.

| Ion | Ar | Kr |
|---|---|---|
| LET [MeV-cm$^2$/mg] | 17 | 40 |
| Energy [MeV] | 150 | 322 |
| Fluence [n/cm$^2$] | $1.07 \times 10^6$ | $9.6 \times 10^5$ |

are sealed in the chamber in order to keep ion energy. Table II shows linear energy transfer (LET), energy and average fluences of heavy ions.

Irradiation tests were done at the static conditions of (DATA, CLK) = (0, 0), (0, 1), (1, 0), and (1, 1). $V_{\rm dd}$ was 0.8 V and 1.2 V at heavy-ion irradiation. Each irradiation time was for 30 second.

Cross Section (CS) is used in order to evaluate soft-error tolerance, which means an area of upsets when a particle passes a circuit block. The soft-error tolerance becomes stronger if CS becomes smaller. Equation (2) is used in order to calculate CS [11].

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\rm error}}{N_{\rm ion}\ N_{\rm FF}} \qquad (2)$$

$N_{\rm ion}$ is the effective heavy-ion fluence per $\mathrm{cm}^2$.

## IV. Experimental Results and Discussion

### A. Neutron Results

Figure 11 shows the experimental result of the SERs by neutrons irradiation with error bars of 95% ($2\sigma$) confidence. There was no error on GGFF at all static conditions. The average SERs of FRFF and DFRFF are 1/3 and 1/5 smaller than that of the standard TGFF respectively.

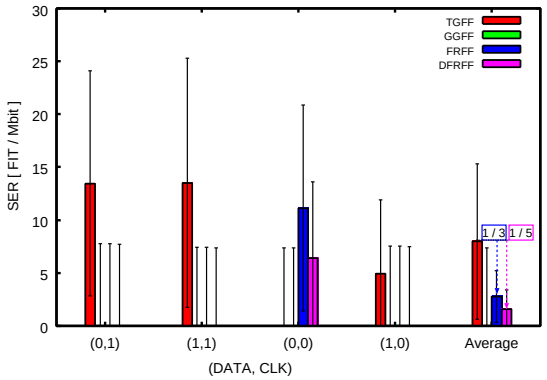



Fig. 11. Experimental results of the SERs by neutron irradiation.

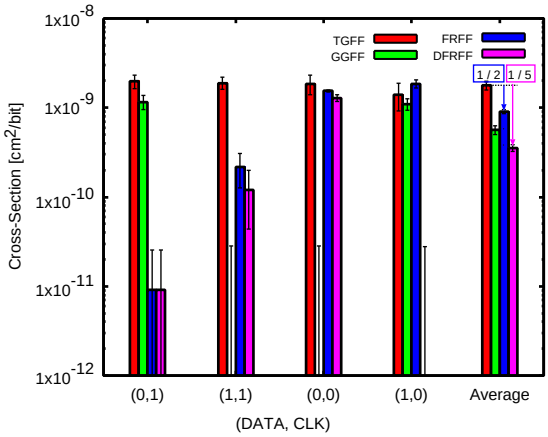



Fig. 12. Experimental results of the CSs by Ar irradiation at $V_{\rm dd}$ of 0.8 V.

### B. Heavy-ion Results

Figures 12 and 13 show the experimental results of the CSs by Ar and Kr at $V_{\rm dd}$ of 0.8 V with error bars of 95% confidence. The average CSs of FRFF are 1/2 smaller than those of the standard TGFF by Ar and Kr. The average CSs of DFRFF are 1/5 and 1/3 smaller than those of the standard TGFF by Ar and Kr respectively.

Figures 14 and 15 show the experimental results of the CSs by Ar and Kr at $V_{\rm dd}$ of 1.2 V with error bars of 95% confidence. The average CSs of FRFF are 1/3 and 1/2 smaller than those of the standard TGFF by Ar and Kr respectively. The average CSs of DFRFF are 1/20 and 1/6 smaller than those of the standard TGFF by Ar and Kr respectively.

The tendency of the results is same even if $V_{\rm dd}$ decreases. The smaller $V_{\rm dd}$ is, the longer the delay time becomes. However, lower $V_{\rm dd}$ makes an SET pulse longer [9]. Therefore, the smaller $V_{\rm dd}$ is, the larger CSs becomes.

### C. Discussion

NMOS transistors are weaker against soft errors than PMOS transistors mainly due to the difference of the mobility [8] [12]. From Fig. 12 to Fig. 14, FRFF is stronger against soft errors at CLK = 1 than at CLK = 0. These results revealed that the guard-gate structure has high soft-error tolerance. However, CSs on DFRFF only becomes large at (DATA, CLK) = (0, 0). Figure 17 shows the inverter affected by radiation at (DATA, CLK) = (0, 0), (1, 1). We should evaluate the delay time composed of guard-gate structure because soft-error tolerance of an FF with guard-gate structure depends on the delay.

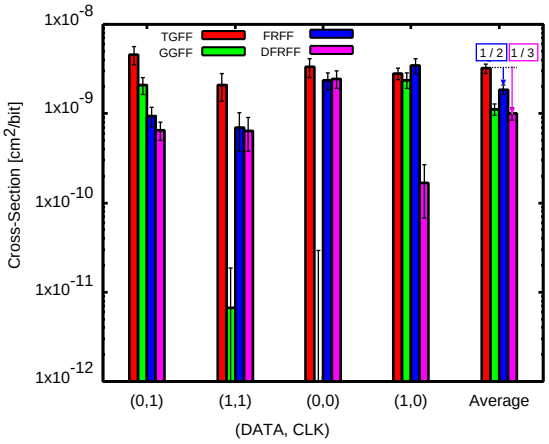



Fig. 13. Experimental results of the CSs by Kr irradiation at $V_{\rm dd}$ of 0.8 V.

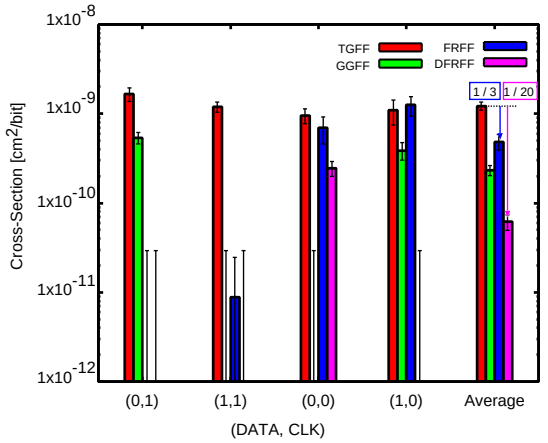



Fig. 14. Experimental results of the CSs by Ar irradiation at $V_{\rm dd}$ of 1.2 V.

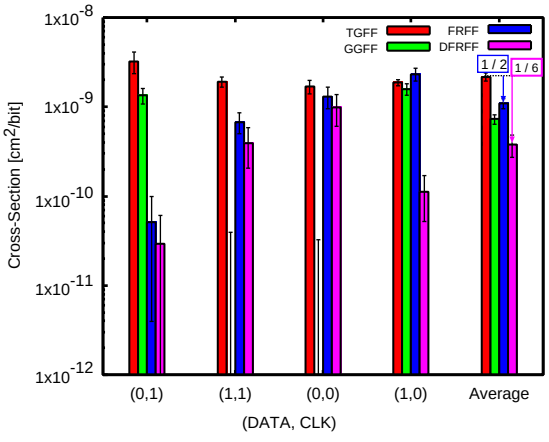



Fig. 15. Experimental results of the CSs by Kr irradiation at $V_{\rm dd}$ of 1.2 V.

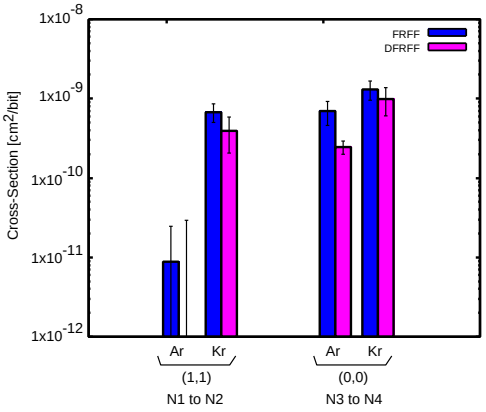
The delay times from N1 to N2 in Figs. 5, and 7 are evaluated by circuit simulations when the radiated particle hits the NMOS of FRFF and DFRFF at (DATA, CLK) = (1, 1) as shown in Fig. 17. The delay time from N3 to N4 in Fig. 7 is also evaluated when the radiated particle hits the NMOS of DFRFF at (DATA, CLK) = (0, 0). Table III shows the results of the delay time at $V_{\rm dd}$ = 1.2 V. Figure 16 (a) compares CSs and delay time at $V_{\rm dd}$ = 1.2 V. Netlists with parasitic components are used on circuit simulations.

Table III revealed that the delay time on DFRFF at (DATA, CLK) = (0, 0) is shortest and the delay time on DFRFF at (DATA, CLK) = (1, 1) is longest. DFRFF has the guard gate

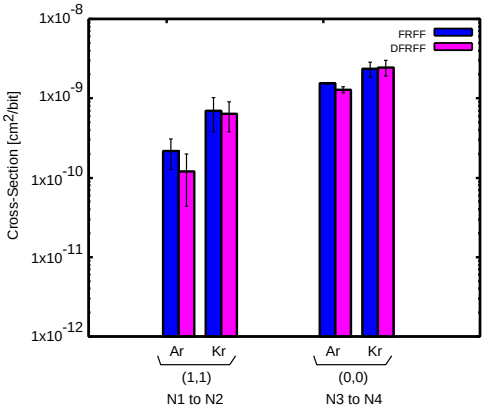
TABLE III

DELAY TIME COMPOSED OF GUARD-GATE STRUCTURE AT $V_{\rm dd}$ = 1.2 V.

| | | N1 to N2 [ps] | N3 to N4 [ps] |
|---|---|---|---|
| 1.2 V | FRFF | 73.3 | n/a |
| | DFRFF | 76.9 | 25.7 |
| 0.8 V | FRFF | 159.3 | n/a |
| | DFRFF | 163.7 | 51.2 |




(a) $V_{\rm dd}$ = 1.2 V.




(b) $V_{\rm dd}$ = 0.8 V.

Fig. 16. Comparison with CSs and delay time.

composed of the output inverter at (DATA, CLK) = (0, 0), and the transistor size of the output inverter is large. The larger the transistor size is, the shorter the delay time becomes. The guard-gate structure can eliminate longer SET pulses caused by a radiated particle as the delay time is longer. The longer the delay time is, the higher soft-error tolerance becomes. Therefore, DFRFF at (DATA, CLK) = (1, 1) is strongest against soft errors among FRFF at (DATA, CLK) = (1, 1) and DFRFF at (DATA, CLK) = (0, 0). DFRFF is weakest against soft errors at (DATA, CLK) = (0, 0). In Fig. 14, there was no error on DFRFF at (DATA, CLK) = (1, 1). The delay time composed of guard-gate structure is 76.9 ps as shown in table III. It can be seen that SET pulses caused by a radiated particle with 17 MeV-cm$^2$/mg are shorter than 76.9 ps. The tendency of the results are same as measurement results in Figs. 12 and 14.

From Fig. 12 to Fig. 15, FRFF and DFRFF are stronger against soft errors than TGFF, while they are weaker against soft errors as the LET becomes larger. The larger LET is, the longer SET pulse becomes. The guard-gate structure could

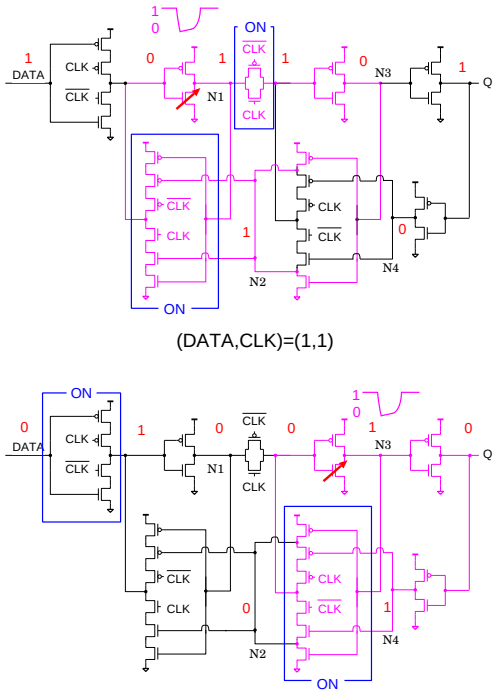



Fig. 17. NMOS transistors sensitive to a heavy-ion hit at (DATA, CLK) = (0, 0), (1, 1).

not resolve SET pulses because it has longer than the delay of two inverters.

Since FRFF has no guard-gate structure, it has no soft-error tolerance at (DATA, CLK) = (0, 0). However, in Figs. 12 and 13, we could not see the difference of CSs on DFRFF and FRFF at this condition. Table III shows the results of the delay time at $V_{\rm dd}$ = 0.8 V. Figure 16 (b) compares CSs and delay time at $V_{\rm dd}$ = 0.8 V. The results include parasitic capacitance. In table III, the delay time of DFRFF is shortest at (DATA, CLK) = (0, 0). The smaller $V_{\rm dd}$ is, the longer SET pulses becomes. Therefore, SET pulses generated a particle hit are longer than 51.2 ps.

In [9], TCAD simulations revealed that the master latch of FRFF has soft-error resilience against a radiated particle up to 60 MeV-cm$^2$/mg. DFRFF has soft-error resilience against a radiated particle up to 60 MeV-cm$^2$/mg at all the static conditions. However, experimental results revealed that the stored values of FRFF and DFRFF were flipped even by a radiated particle with 17 MeV-cm$^2$/mg. It is necessary to increase the delay time of the guard-gate structure to eliminate soft errors.

## V. Conclusion

We measured radiation hardness of the standard TGFF, GGFF, FRFF and DFRFF in the 65nm thin BOX FDSOI by neutrons and Ar and Kr ions. FRFF has the guard-gate structure only in the master latch. GGFF and DFRFF have the guard-gate structures in both of the master and slave latches. In the experimental results, the guard-gate structure is strong against soft errors by neutrons and heavy ions with LET below 17 MeV-cm$^2$/mg. However, the larger LET is, the weaker the guard-gate structure becomes against soft errors because higher-LET particles generate longer SET pulses. The guard-gate structure could not resolve SET pulses because the delay time of the two inverters as a delay element is shorter than SET pulses by higher-LET particles. We concluded that the delay in the guard-gate structures in both of FRFF and DFRFF is shorter than SET pulses generated by higher-LET particles. In [9], TCAD simulations revealed that the guard=gate structure has soft-error resilience against a radiated particle up to 60 MeV-cm$^2$/mg. However, experimental results showed that the stored values of FRFF and DFRFF were flipped even by a radiated particle with 17 MeV-cm$^2$/mg. It is necessary to increase the delay time composed of guard-gate structure to eliminate soft errors.

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