Radiation-Hardened Structure to Reduce Sensitive Range of a Stacked Structure for FDSOI

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***Abstract*— Flip-flops (FFs) with stacked transistors have high radiation tolerance in fully-depleted silicon on insulator (FDSOI) process. However, it is weak against a radioactive particle hit with high liner energy transfer (LET) and from high incident angles. We propose a radiation-hardened structure to reduce sensitive range (RSR) of a stacked structure for FDSOI. We evaluated radiation hardness of FFs with the proposed RSR structure by TCAD simulations and heavy-ion irradiation on the fabricated chip in 65 nm. The heavy-ion irradiation results show that soft-error rates of the proposed FFs are at least 1/14 smaller than those of the stacked FF.**

I. Introduction

According to technology downscaling, soft errors become a significant issue to threaten the reliability of semiconductor chips. The soft error is a phenomenon that stored values in flip-flops (FFs) or SRAMs upset by radiation effects. It is caused by heavy ions in outer space.

Devices in advanced technologies for outer space must be designed for radiation-hard to achieve high reliability. Triple modular redundancy (TMR) [1] and dual interlocked storage cell (DICE) [2][3] are widely used for reliable chips. However, they have larger delay, area and power than conventional FFs. Thus, radiation-hardened FFs with small overheads are indispensable. Stacked structures on fully-depleted silicon on insulator (FDSOI) mitigate soft errors with small area and power penalty [4][5][6].

It is reported that neutron-induced soft error rates (SERs) on 90 nm DICE latches are more than 10x higher than that of non-redundant latch [7]. In contrast, the neutron-induced SER of the DICE FF is almost half of that of the DFF on 40 nm technology. This is because narrow spacing between transistors results in charge collection on multiple nodes when an ion hits on them. Similarly, we observed the stacked structures on FDSOI were influenced by charge sharing when heavy ion has high liner energy transfer (LET) [8]. The cross section (CS) on the stacked structures in a 65 nm FDSOI process is shown in Fig. 1. The CS of the stacked latch is 1/11 than that of the conventional unstacked one even by heavy ions with LET of 40.9 MeV-cm^2/mg. But the CS of the stacked latch gradually approaches to that of the unstacked one.

In this paper, we propose a radiation-design to eliminate soft errors on the stacked structures for FDSOI even by heavy ions over 40.9 MeV-cm^2/mg. We evaluated the radiation-hardness of the FFs with the proposed radiation-design by TCAD simulations and heavy-ion irradiation on fabricated test chips in a 65 nm FDSOI process. Section II explains proposed radiation-design and TCAD simulations results. Section III explains proposed FFs using the radiation-design. Section IV shows the test chip structure and experimental results by heavy-ion irradiation. Section V concludes this paper.

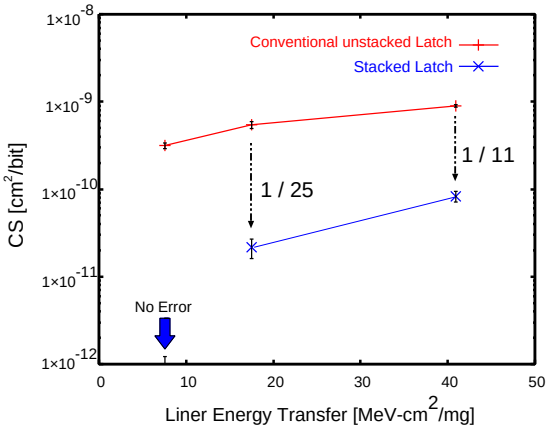


Fig. 1. Measured results of heavy-ions-induced CS on latches in a 65 nm FDSOI process. [8]

II. Radiation-Hardened Structure

FDSOI processes suppress radiation-effects because it prevents charge collection under the buried oxide (BOX) layer. Whereas, the parasitic bipolar effect (PBE) is dominant to cause soft errors in FDSOI devices [9]. Generated holes in a channel rise the potential of the body layer. Then, a parasitic bipolar transistor which is composed of the drain, body and source terminals turns on. The stacked structure was proposed to suppress the PBE in FDSOI [4]. Fig. 2 shows the stacked inverter composed of two series-connected NMOS and PMOS transistors. Diffusion layers between two series-connected transistors are shared to minimize area. When a radiation particle hits NMOS transistors of the stacked inverter, its output does not flip unless both of them turn on at the same time. However, the radiation hardness of the stacked structure decreases as the LET of heavy ions increases. Heavy ions with high LET influence both of two stacked transistors when they pass near the stacked transistors.

A. Proposed Radiation-Hardened Structure

Fig. 3 shows the proposed reduction sensitive range (RSR) inverter. The diffusion layers between two series-connected NMOS and PMOS transistors in the RSR inverter are shorted by a metal wire. The RSR inverter is more stronger than the stacked inverter because generated holes and electrons by heavy ions are wiped out through the metal.

Radiation-hardness of the RSR inverter is evaluated by three-dimensional TCAD simulations at supply voltage (V_{DD}) = 0.8 V using the Synopsys Sentaurus. Fig. 4 depicts the latch composed of an RSR inverter and a conventional inverter and the cross section view of stacked NMOS transistors in the RSR inverter. Heavy ions up to 60 MeV-cm^2/mg LET is injected to the RSR inverter considering the outer space usage [10]. The spatial distribution of charge cloud is defined as a Gaussian function with the standard deviation of

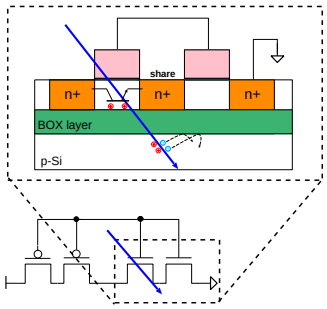


Fig. 2. Stacked inverters.

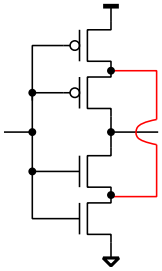


Fig. 3. Proposed reduction sensitive range inverter.

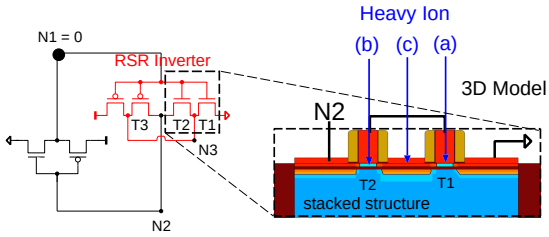
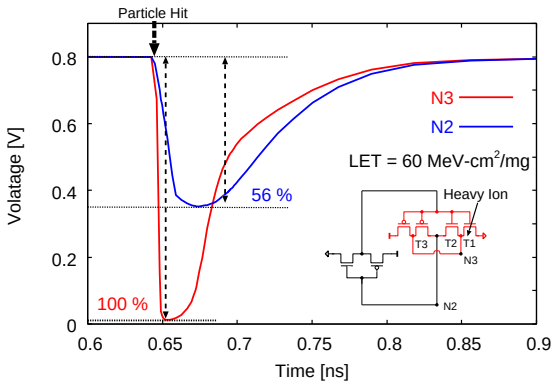
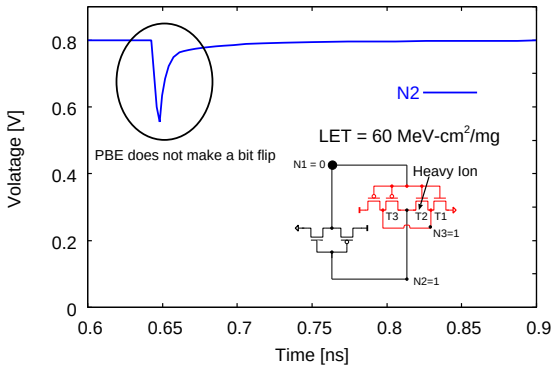


Fig. 4. Schematic diagrams and cross section view of 3D models used for TCAD simulations. By setting the initial value of N0 to 0 V, a heavy ion hits at the NMOS transistor at V_{DD} = 0.8 V.



(a) Particles hit at T1 transistor. N2 and N3 are influenced by a particle.



(b) Particles hit at T2 transistor. PBE is not significant.

Fig. 5. Simulation results of voltage waveforms caused by heavy ion. Latch in Fig. 4 does not upset up to LET = 60 MeV-cm^2/mg.

30 nm [11]. Particle hits on NMOS transistors are evaluated because NMOS transistors are more vulnerable to particle hits than PMOS transistors [8].

(a) Particles hit at T1 transistor: The stored value of the latch does not upset even though a particle has the LET of 60 MeV-cm^2/mg. Voltage waveforms of N2 and N3 are shown in Fig. 5 (a). The SET pulse is attenuated by 44% after passing through the PMOS pass-transistor (T3). This is because the PMOS pass-transistor cannot pass signals below the threshold voltage.

(b) Particles hit at T2 transistor: The stored value of the latch does not upset even though a particle has the LET of 60 MeV-cm^2/mg as shown in Fig 5 (b). Parasitic bipolar transistor turn on in the T2 transistor. Although, the PBE induces current flow, soft error rates does not increase because the voltage of drain and source on T2 is must be equal due to the shorted wire.

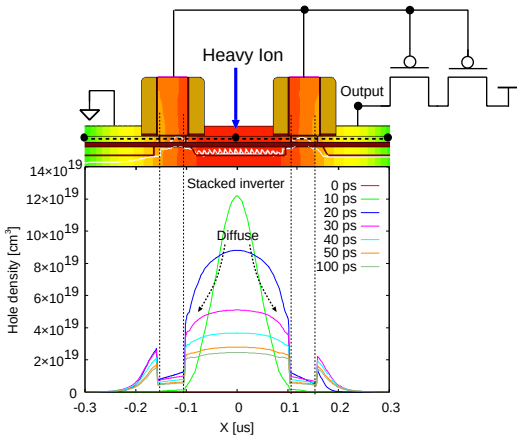
(c) Particles hit at the center of drain region between T1 and T2 transistors: The stored value of the latch does not upset even though a particle has the LET of 60 MeV-cm^2/mg. It is 10x larger than the threshold LET (the minimum LET value at which the latch upsets) of the latch composed of the stacked inverter instead of the RSR inverter.

In order to explain the difference of the radiation-hardness between the stacked and the RSR inverters, hole density generated by a heavy ion strike is calculated using TCAD simulations. Holes forcedly turn on the parasitic bipolar transistor. Fig. 6 shows transient hole densities in the body layer of the stacked transistors after a heavy ion strike. In Fig. 6 (a), generated holes remain in both channel regions even after 100 ps at the density of 2×10^{19} cm^3. As a result, a stored value is flipped when a heavy ion hits on the stacked inverter. However, in Fig. 6 (b), generated holes decrease below 0.8×10^{19} cm^3 after 10 ps. This is because generated holes are recombined with electrons flowing through the wire on N3. Fig. 7 shows transient hole and electron current through the wire on N3 after a heavy ion strikes on the RSR inverter. Thus, the RSR inverter is more stronger than the stacked inverter.

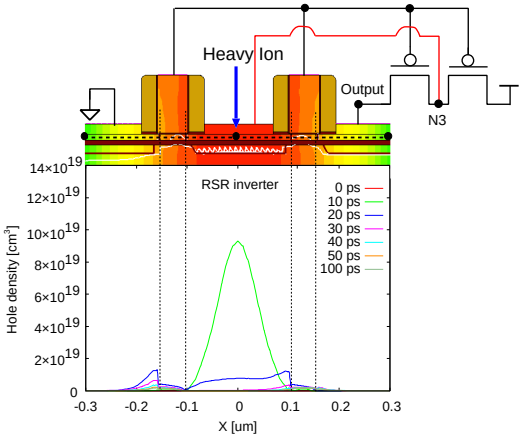
III. Radiation-Hardened Design in Flip-Flop

Fig. 8 shows a conventional DFF called Transmission Gate FF (TGFF). It has the master and slave latches composed of a tristate inverter and an inverter. It is not tolerant against soft errors. Fig. 9 shows the stacked FF. It has the master and slave latches composed of a stacked tristate inverter and a stacked inverter. Although the overheads of delay time and area of the stacked FF are bigger than TGFF, the stacked FF is strong against soft errors as shown in Fig. 1.

Fig. 10 shows the RSRFF. It has the master and slave latches composed of the RSR tristate inverter and the RSR inverter in master and slave latches. The RSRFF has long delay as the stacked FF due to the stacked structures. We propose a radiation-hardened FF using the RSR structure with short delay time. In Fig. 11, the proposed FF named RSR with low delay overhead FF (RSRLDFF) is shown. Transmission gate (TG) in the RSRFF is replaced by the tristate inverter directly connected to the output inverter. Thus, the RSR structure in the slave latch has a small impact on delay time. In addition, the RSR inverter in the master latch and the TG is connected to N3 instead of N2 as shown in Fig. 11. Through this connection, the tristate inverter between the master and slave latches is driven by T1 and T4 transistors directly connected to power or ground rails while maintaining



(a) Stacked inverter



(b) RSR inverter

Fig. 6. Simulated transition of hole density in the body layer when a heavy ion with LET of 60 MeV-cm^2/mg passes through the center of drain region between two series-connected NMOS transistors at 0 ps.

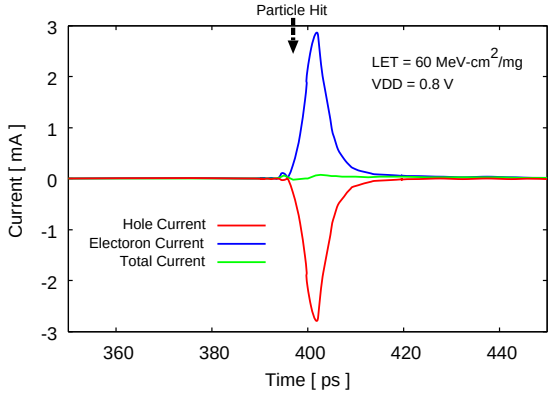


Fig. 7. Simulated transition of hole and electron current through wire on N3 when a heavy ion with LET of 60 MeV-cm^2/mg hit on RSR inverter.

the RSR structure. Therefore, the RSRFF achieves smaller D-Q delay time than the stacked FF.

Table I indicates the simulation results of delay time, power at 10% data activity and area at V_{DD} = 0.8 V. All values are normalized to those of the TGFF. The values in parentheses are normalized to those of the stacked FF. The delay time of the stacked FF is 1.8x longer than that of the TGFF because the stacked inverters worsen its delay time. The delay time of the proposed RSRFF is 2.2x longer than that of the TGFF. However, the proposed RSRLDFF is 30% faster than that of the stacked FF because the stacked structure with the

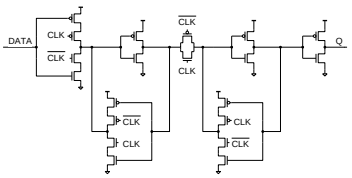


Fig. 8. Transmission-gate FF (TGFF).

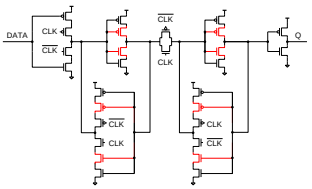


Fig. 9. Stacked FF.

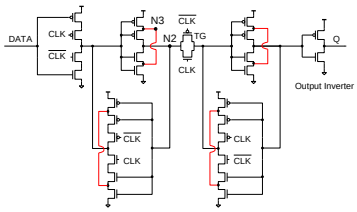


Fig. 10. Reduction Sensitive Range FF (RSRFF).

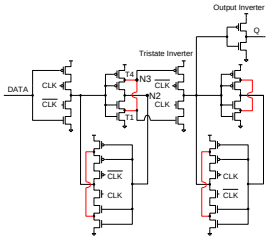


Fig. 11. RSR with low delay overhead FF (RSRLDFF).

TABLE I

SIMULATION RESULTS OF D-Q DELAY, POWER, AREA OF EACH FF WHEN V_{DD} = 0.8 V. ALL VALUES ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF STACKED FF.

FF	D-Q delay	Power	Area
TGFF	1	1	1
Stacked FF	1.76 (1)	1.05 (1)	1.24 (1)
RSRFF	2.16 (1.23)	1.07 (1.04)	1.24 (1.00)
RSRLDFF	1.25 (0.71)	1.08 (1.05)	1.35 (1.08)

TABLE II

NUMBER OF EMBEDDED FFS IN THE CHIP.

FF	# of FF
TGFF	25,200
Stacked FF	25,500
RSRFF	25,500
RSRLDFF	25,200

shorted wire in the RSRLDFF has small influence on its delay time. The power consumption is almost same as that of the stacked FF and TGFF. The area of the RSRLDFF is bigger than that of the stacked FF. This is because the RSRLDFF has two additional transistors.

IV. Experimental Results by Heavy-Ion Irradiation

The TGFF, stacked FF and proposed FFs were fabricated in a 65 nm FDSOI process with thin BOX layers [12]. Table II indicates the number of embedded FFs in the chip.

Heavy-ion irradiation test was carried out at the takasaki ion accelerators for advanced radiation application (TIARA), Japan. We measured the number of upsets caused by heavy ions at V_{DD} = 0.8 V. Test chip were exposed to heavy ions at the static conditions for 30 s. Measurements were repeated five times per condition by Xe ion (LET of 67.2 MeV-cm^2/mg) from the normal angle under four DATA and CLK states. In addition, we examined Xe ion-induced CSs depending on incident angles at V_{DD} = 0.8 V when (DATA, CLK)=(0,1).

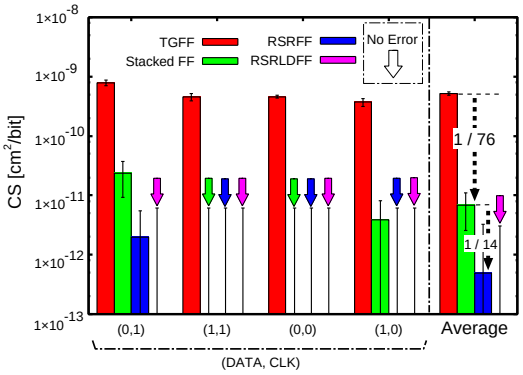


Fig. 12. Experimental results of heavy-ion-induced cross sections from the normal angle under four DATA and CLK states and averaged CSs. The error bars are within 95.4% confidence. Down arrows mean no error.

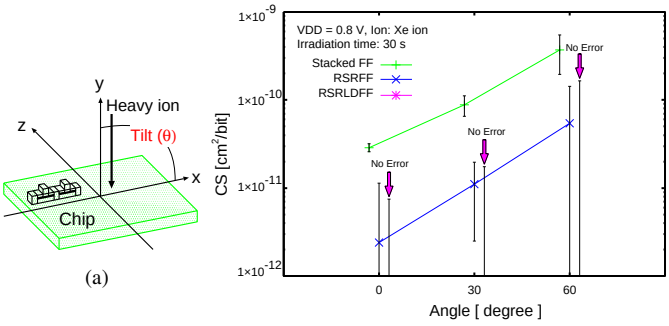


Fig. 13. (a) shows tilt angles of chip. (b) shows experimental results depending on tilt angles when (DATA, CLK)=(0,1). The error bars are within 95.4 % confidence intervals. Down arrows mean no error.

Experiments were carried out from 30° and 60° tilt angles. The tilt angle (θ) of the chip is defined as shown in Fig. 13 (a).

The CS is used in order to evaluate soft-error tolerances. Eq. 1 is used in order to calculate the CS [13].

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}} \cos\,\theta\ N_{\mathrm{FF}}} \tag{1}$$

CS is calculated from the number of errors (N_{error}), the effective heavy ion fluence at θ ($N_{\mathrm{ion}} \cos\,\theta$), and the number of FFs (N_{FF}).

Fig. 12 shows heavy-ion-induced CSs under four static conditions and the averaged CSs when V_{DD} = 0.8 V. The averaged CS of the stacked FF is 1/76 smaller than that of the TGFF. The stacked structure suppresses soft error but there are still 14 errors in the stacked FF. The averaged CS of the RSRFF is 1/14 smaller than that of the stacked FF. There is only 1 error in the RSRFF. The RSR structure eliminates soft errors in the stacked structure. There is no error in the RSRLDFF, which is strongest of all.

Fig. 13 (b) shows the heavy-ion-induced CSs depending on tilt angles. The CSs of the RSRFF at tilt angles of 30° and 60° are 1/8 smaller than that of the stacked FF. There are 16 errors in the stacked FF at tilt angle of 60°. While, there are two errors in the RSRFF at tilt angle of 60°. There is no error in the RSRLDFF at all angles. The proposed FFs are strong against soft errors even at higher tilt angles.

V. Conclusion

We propose a radiation-hardened structure has a shorted wire between series-connected PMOS and NMOS transistors to reduce sensitive range of the stacked structure for FDSOI. In addition, we propose a radiation-hardened FF with small delay overhead. The proposed RSRLDFF has 30% shorter delay and 10% area overheads than the conventional stacked FF. We investigated their radiation hardness by TCAD simulations and heavy-ion irradiation. There is no error in the RSRLDFF at incident angles of 0°, 30° and 60° even at LET of 67.2 MeV-cm^2/mg. The proposed structure is strong against soft errors even by increasing incident angles and particle energy.

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