Evaluation of Heavy-Ion-Induced SEU Cross Sections of a 65-nm Thin BOX FD-SOI Flip-Flops Based on Stacked Inverter

Jun Furuta, Kentaro Kojima and Kazutoshi Kobayashi
Graduate School of Science & Technology, Kyoto Institute of Technology

***Abstract*—Cross sections to cause single event upsets by heavy ions are sensitive to dopant concentration in diffusion and the structure of the raised layer especially in FDSOI. Due to the parasitic bipolar effect, radiation-hardened FFs using the stacked structure in FDSOI are not free from soft errors, which is consistent with measurement results by heavy-ion irradiation. Device-simulation results show that the cross section is proportional to the silicon thickness of the raised layer and inversely proportional to the doping concentration in drain.**

***Index Terms*—single event effect, soft error, heavy ion irradiation, FD-SOI, flip flop, device simulation.**

I. Introduction

Radiation-induced soft error is a significant concern for medical devices, aerospace, and high-performance super computers. For super computers, continuous operation time is limited by soft errors since over 800,000 processors are operated simultaneously [1]. Radiation-hardened designs are mandatory to achieve high reliability with small overhead of performance. Flip flops (FFs) or latches must be protected from soft errors [2], [3]. Redundant FFs achieve high soft error mitigation, while they have large power and area overhead. In addition, multiple node charge collection becomes a critical issue for redundant FFs to keep the same amount of soft-error resilience in more advanced technology nodes [4], [5].

For the device-level radiation-hardened technology, silicon on insulator (FDSOI) transistors have smaller sensitive volume than bulk transistors, which is highly correlated with soft-error resilience [6], [7]. SOI transistors have a buried oxide (BOX) layer inserted under transistors. Especially, the fully-depleted SOI (FDSOI) technology makes the transistor layer thinner with smaller sensitive volume than the partially-depleted SOI (PD-SOI) technology. The BOX layer can block charge collection by drift and funneling. Radiation-induced current glitches on FDSOI transistors are smaller than those on bulk transistors. However, the FDSOI process does not have enough soft error immunity for mission-critical electrical equipments [8], [9]. It is because the floating body region inside the transistor layer turns on the parasitic bipolar transistor. It amplifies collected charge induced by a radiation strike [10]. Stacking transistors make the soft error tolerance stronger not on bulk but on FDSOI. Soft errors on the stacked latch in FDSOI may happen only when stacked transistors are simultaneously influenced by a particle strike. In order to investigate sensitivity to soft errors by changing device parameters or structures, it is convenient to utilize device simulations without chip fabrication.

The drain-source surface on MOSFETs is covered by silicide to reduce resistance. When silicide reaches the boundary between the diffusion layer and the channel, a Schottky connection is generated to prevent current flow. silicon layer is formed by deposition to separate silicide and the channel, which is called a raised layer. The structure of the raised layer severely affects the amount of charge generated by a particle strike.

In this paper, cross sections of a standard flip-flop (FF) and a radiation-hardened FF based on the stacked inverter in an 65 nm FDSOI process are estimated by device simulations. Radiation hardness of the standard and stacked latches were measured by heavy-ion irradiation to confirm simulation results.

This paper is organized as follows. Section II shows device simulation results of cross sections in a 65 nm FDSOI process. In Section III, Heavy-ion test results are described on FFs in order to compare simulation results with test results. Soft error mitigation technique by controlling dopant concentration is discussed in Section IV. Finally, we conclude this paper.

II. Evaluation of Cross Section in a 65 nm FDSOI Process by TCAD Simulations

In this section, Cross sections are evaluated using a commercial TCAD simulation tool, Synopsys Sentaurus in order to examine how soft errors occurs in a FDSOI process

A. Soft Errors in FDSOI Process

In the bulk process, charge collection is a dominant source to cause soft errors, while in the FDSOI process, the parasitic bipolar effect (PBE) is dominant. PBE arises due to an increase of hole density in the channel region. Fig. 1 shows how holes are generated in diffusion and collected to the channel region. PBE turns on the parasitic bipolar transistor under the channel to cause a flip of memory storage cells such as an SRAM cell or a latch. In the FDSOI process, charge is collected only above the BOX layer. Charge generated inside silicon in the raised layer formed on the top of the diffusion layer also causes a soft error.

The stacked structure in FDSOI is strong against soft errors since it is hard to turn on the stacked transistors at the same

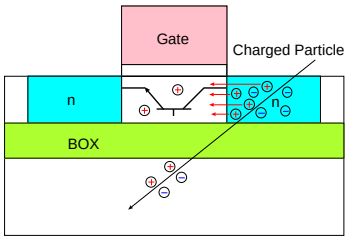


Fig. 1. Holes generated in the diffusion region are collected in the channel region and then drain-body-source parasitic bipolar transistor turns on.

time. However, in bulk charge generated in the body region is collected to both transistors. The stacked structure is not effective to suprress soft errors in bulk.

B. Simulation Setup

Two 3D models for TCAD simulations are constructed to evaluate cross sections of flip-flops in a 65 nm FDSOI. Fig. 2 shows cross-sectional views of the 3D models and the schematic diagrams of a standard clocked latch and a radiation-hard latch used in device- and transistor-level mixed-mode simulations. In the standard clocked latch, one of the stacked transistors turns on to keep a stored value, while in the radiation-hard latch both stacked transistors turn off. The radiation-hard latch consists of two stacked inverters. The stacked structure drastically suppresses PBE caused by a radiation strike [11].

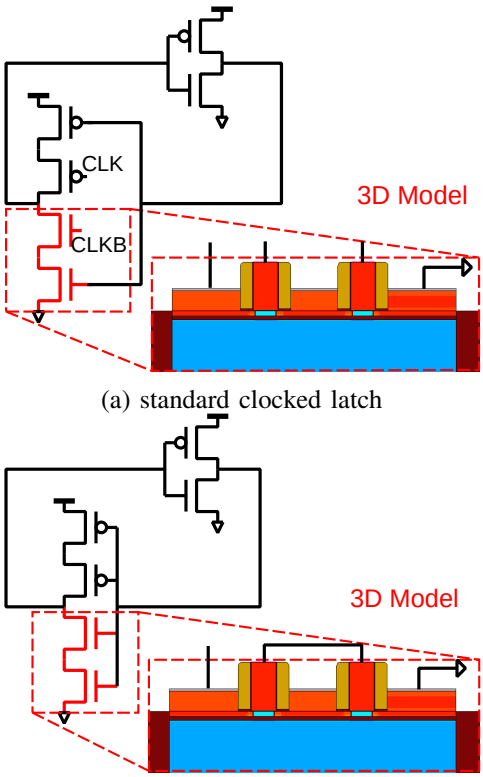
A normal-incident heavy ion with linear energy transfer (LET) of 15.7 MeV-cm^2/mg strikes the 3D-model transistor. Heavy ion strikes are modeled as a Gaussian distribution along the ion track. The track radius is set to 20 or 40 nm. Heavy ions are irradiated on a standard latch and a radiation-hardened latch with the stacked structure in a 65 nm FDSOI process.

In order to evaluate cross sections, heavy ions are irradiated every 20 or 40 nm grid as shown in Fig. 3. The shape and area of cross sections are obtained from each ion strike as same as the heavy-ion microbeam test [12].

C. Simulation Results

Figure 4 shows cross sections caused by a heavy ion with LET of 15.7 MeV-cm^2/mg. The cross section of the standard latch covers the channel region and almost the entire drain region. Single event upsets (SEUs) also arise in the stacked latch even when heavy ions strike from the normal incidence. It is hard for particles from the normal incident to generate charge that affect both stacked transistors. Thus the cross section in the stacked latch is mainly in the diffusion region between two stacked transistors and does not fully cover the channel region.

In order to consider the error mechanism in the FDSOI process, hole density generated by a heavy ion strike is examined through device simulations. Generated holes elevate well potential and then turn on the parasitic bipolar transistor. Fig. 5 shows transient hole density in the body layer of the stacked latch after a heavy ion strike. At 0 ps, a heavy ion



(a) standard clocked latch

(b) radiation hardened latch with stacked structure

Fig. 2. Schematic diagrams with the cross-sectional view of 3D models used for mixed-mode simulations. (a) Standard clocked latch, (b) Radiation-hard stacked latch.

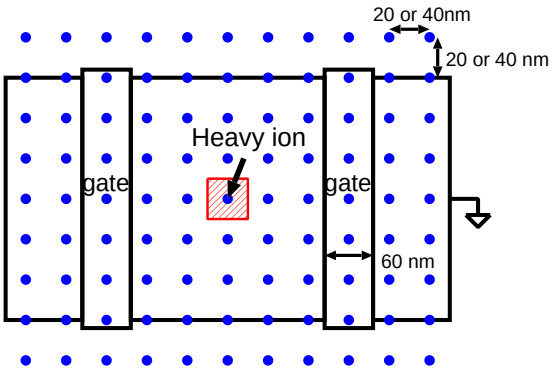


Fig. 3. Simulation setup to evaluate cross sections induced by a heavy ion with LET of 15.7 MeV-cm^2/mg. Radiation particles strike at the blue dots.

incidents at the center of the two stacked NMOS transistors. As can be seen from the figure, most holes stay within 0.1 μm from the incident point at 10 ps. Holes are diffused to the channel regions in 30 ps and 50 ps. In either state, generated holes are diffused to the channel region. The distribution of generated holes is extremely low below the channel region. Generated holes diffuse to the channel region and both of the parasitic bipolar transistors simultaneously turn on. As a result, a stored value can be flipped. These simulation results show that hole diffusion in the drain region affects the soft error

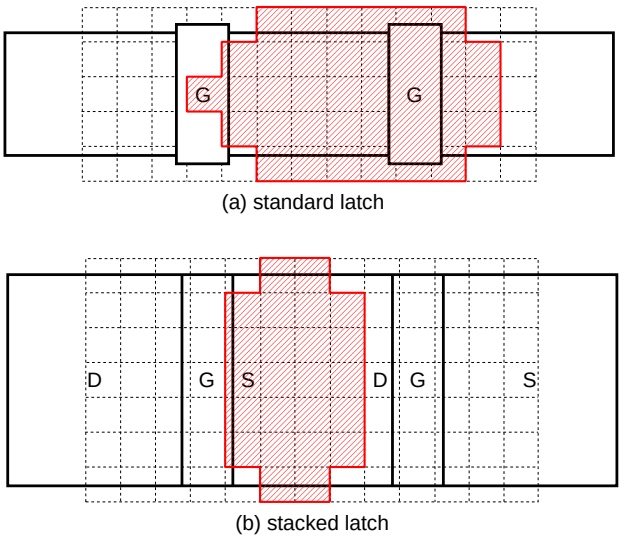


Fig. 4. Shape of cross sections in (a) standard latch and (b) stacked latch by heavy ions with LET of 15.7 MeV-cm^2/mg.

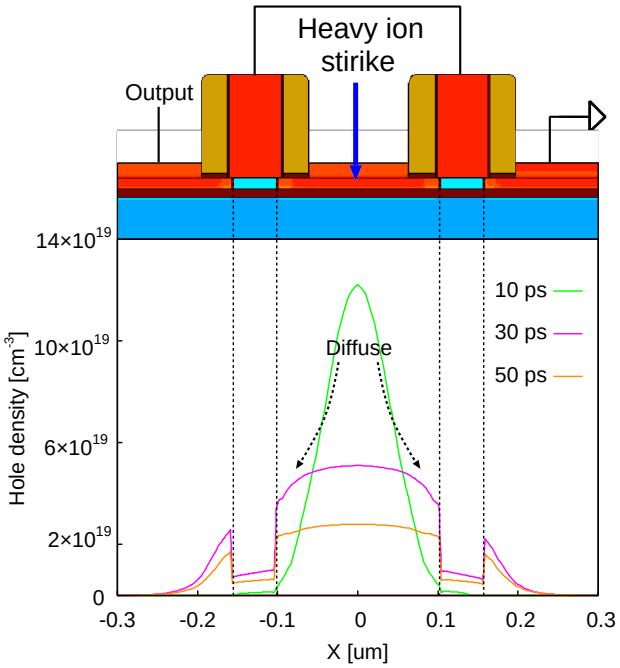


Fig. 5. Simulated transient distribution of holes in the body layer of stacked latch when a heavy ion with LET of 15.7 MeV-cm^2/mg hit at the center of the stacked transistors at 0 ps.

immunity in the FDSOI process.

III. Soft Error Rates on FDSOI Process by Heavy Ion Test

Soft error rates (SERs) of the standard FF and the radiation-hardened FF with the stack structure were measured to obtain their cross sections from accelerated tests and to compare simulation results with measured ones.

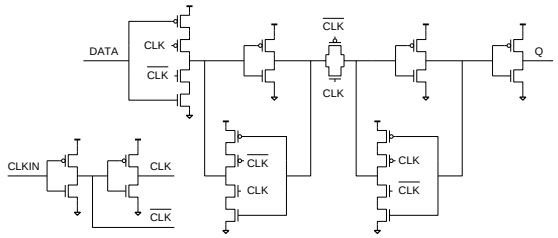


Fig. 6. Schematic diagram of a standard transmission gate FF (TGFF).

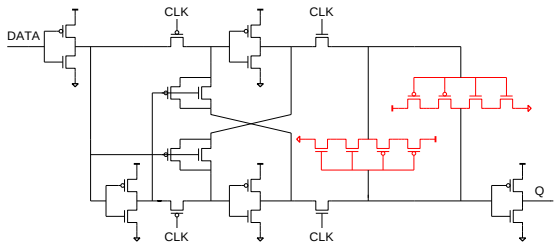


Fig. 7. Schematic diagram of the adaptive-coupling FF with stacked structure.

TABLE I
SPECIFICATIONS OF HEAVY IONS AT QST.

Ion	Energy [MeV]	LET [MeV-cm^2/mg]	Range [μm]
$^{20}Ne^{4+}$	75	6.5	38.9
$^{40}Ar^{8+}$	150	15.8	36.1
$^{84}Kr^{17+}$	322	40.3	37.3

A. Test Chip Structure

To measure SERs by heavy ion tests, we implemented the standard transmission gate FF (TGFF) and the adaptive-coupling FF (ACFF) with the stacked structure named AC_SS FF [13]. Figures 6 and 7 show the schematic diagrams of TGFF and AC_SS FF, respectively. Slave latches of AC_SS FF are constructed by two stacked inverters. Test chips were fabricated in a 65 nm thin BOX FDSOI process. The test chip includes 23,976 TGFFs and 41,760 AC_SS FF. The thicknesses of the BOX layer and body layer are 10 and 12 nm respectively.

B. Experimental Setup and Results

Heavy-ion tests were carried out at National Institutes for Quantum and Radiological Science and Technology (QST), JAPAN. All TGFFs and AC_SS FFs are at a static condition and supply voltage is fixed to 0.8 V. Ne, Ar and Kr ions hit to the chip from the normal angle. Table I shows the specification of heavyy ions at QST.

Figure 8 shows the experimental results of cross sections by LET when all FFs stored 0 and the clock signal was fixed to 0. The cross section of AC_SS FF is smaller than that of TGFF. However, there are still some SEUs in AC_SS FF with the stacked structure, which is consistent with the simulation results.

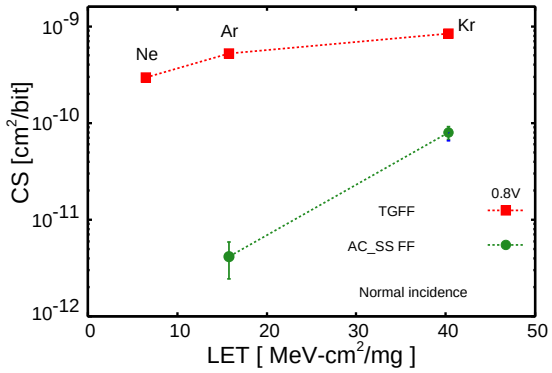


Fig. 8. Experimental results of cross sections of TGFF and AC_SS FF according to LET.

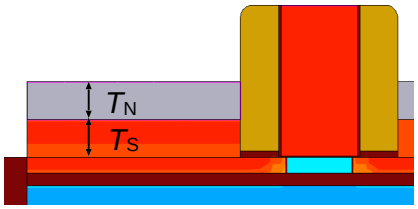


Fig. 9. Structure of raised layer, definition of thickness of silicon (T_S) and thickness of nickel silicide (T_N).

IV. Efficient Soft-Error Mitigation Technique for FDSOI Processes

In this section, we discuss how to enhance soft errors immunity for FDSOI using the stacked structure by optimizing the fabrication process.

In FDSOI, soft errors are caused by hole diffusion on the drain region and PBE as already mentioned in Sect. II. To enhance soft error immunity, dopant concentration in the diffusion region is a key parameter. Deeper concentration accelerates the auger recombination that promotes carrier disappearance. The probability of the auger recombination (R_{Aug}) depends on the carrier density from Eq. (1).

$$R_{\mathrm{Aug}} = \begin{cases} \mathrm{B}n^2p & (n > p) \\ \mathrm{B}p^2n & (p > n) \end{cases} \quad (1)$$

B is the Auger coefficient, n is carrier density of electrons, and p is carrier density of holes. Hole disappear before it reaches the channel region, which improves the soft error resilience. The shape of the raised layer also affects the resilience. The raised layer is composed of silicon and silicide. Figure 9 shows a cross-sectional view. The thickness of silicon and silicide are defined as T_S and T_N. In FDSOI, charge generated at above of the BOX layer becomes a source to cause a soft error. Thinning silicon in the raised layer lowers the amount of generated charge.

We assume that nickel silicide is used as silicide, $T_N = 5$ nm and T_S is changed from 50, 60, and 70 nm.

TABLE II
CROSS SECTIONS OF THE STANDARD LATCH ACCORDING TO DOPING CONCENTRATION AND THE THICKNESS OF SILICON IN THE RAISED LAYER.

Doping concentration [cm^{-3}]	Cross Section [cm^2/ion]		
	T_S = 50 nm	T_S = 60 nm	T_S = 70 nm
1×10^{20}	5.44×10^{-10}	5.76×10^{-10}	6.72×10^{-10}
3×10^{20}	5.76×10^{-10}	—	—
5×10^{20}	5.44×10^{-10}	—	—

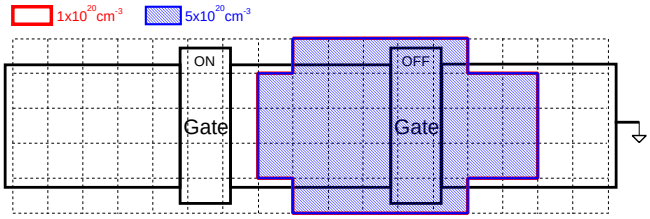


Fig. 10. Simulation results of cross sections of the standard latch according to doping concentration on the drain regions when T_S = 50 nm.

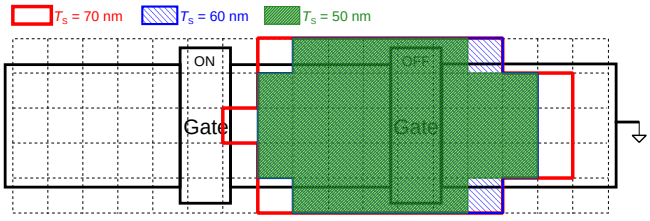


Fig. 11. Simulation results of cross sections of the standard latch according to the T_S on the drain regions when doping concentration in diffusion is 1×10^{20}cm^{-3} .

A. Error Resilience on Standard Latch

Figure 10 shows the cross sections when the dopant concentration in the diffusion layer is changed from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3} when T_S = 50 nm. The cross sections are not influenced by the dopant concentration.

Figure 11 shows the cross sections by changing the thickness of silicon in the raised layer from T_S = 70 to 50 nm with the dopant concentration of 1×10^{20} cm^{-3}. The cross section when T_S = 50 nm is 19.0% smaller than that when T_S = 70 nm. The thickness of the silicon layer impacts the soft error tolerance, while doping concentration in diffusion does not affect it.

B. Results of Stacked Latch

Figure 12 and Table III show device simulation results of cross sections. The condition is same as the standard latch. For the stacked structure, the cross section becomes small by increasing doping concentration from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3}.

At T_S = 50 nm, the cross section changges from 0.44×10^{-10} cm^2/ion to 0 cm^2/ion. At T_S = 60 nm and 70 nm, the cross section decreases by 51.7% and by 47.1% respectively. When T_N was changed from 70 nm to 50 nm, the C_{gg}-V_{gs} curve is changed within 5%, and the I_{ds}-V_{gs} curve is changed within 0.4%. When the doping concentration of the diffusion layer is changed from 1×10^{20} cm^{-3} to 5×10^{20}

TABLE III
CROSS SECTIONS OF THE STACKED LATCH ACCORDING TO DOPING CONCENTRATION AND THE THICKNESS OF SILICON IN THE RAISED LAYER

Doping concentration [cm^{-3}]	Cross Section [cm^2/ion]		
	T_S = 50 nm	T_S = 60 nm	T_S = 70 nm
1×10^{20}	0.44×10^{-10}	1.16×10^{-10}	1.36×10^{-10}
3×10^{20}	0.28×10^{-10}	0.56×10^{-10}	1.36×10^{-10}
5×10^{20}	0	0.56×10^{-10}	0.72×10^{-10}

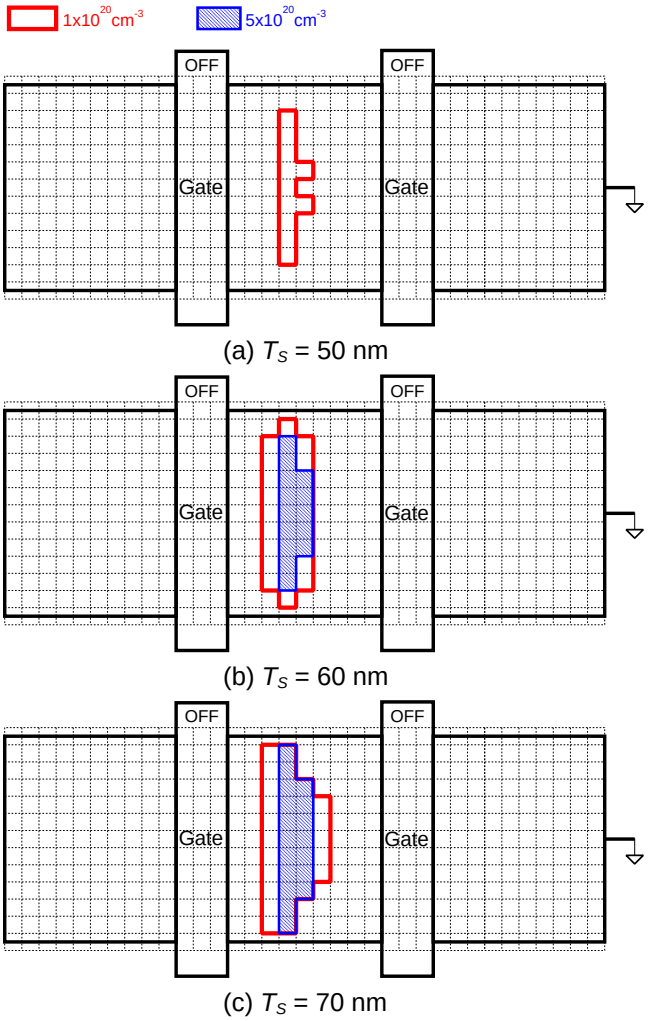


Fig. 12. Simulation results of cross sections according to the impurity density on the drain regions thickness silicon in raised layer .

cm^{-3}, the C_{gg}-V_{gs} curve is changed within 2%, but the I_{ds}-V_{gs} curve does not change. Simulation results show that the stacked structure with 5×10^{20} cm^{-3} doping concentration in the diffusion region decreases soft error rates by 47% or more with almost similar transistor performance with 1×10^{20} cm^{-3}. The soft error rate of the stacked latch is much more influenced by doping concentration than that of the standard latch. Unlike the standard latch, both of doping concentration and the silicon thickness in the raised layer greatly affect the soft error tolerance in the stacked structure.

V. Conclusion

Cross sections of a standard flip-flop (FF) and a radiation-hardened FF with the stacked structure in a 65 nm FDSOI process were investigated by device simulations according to process recipes such as dopant concentration and the structure of the raised layer above drain and source terminals. The BOX layer prevents generated carriers in substrate being collected to transistors. The stacked FF is relatively strong against soft errors because is hard to simultaneously turn on two stacked transistors by a particle strike. But the simulation results reveal that it is possible to turn on both of stacked transistors by a heavy-ion strike in the FDSOI process. It is because heavy-ion-induced holes in drain region are collected to channel by diffusion and then the parasitic bipolar transistor between drain and source turns on by collected holes.

For the stacked structure soft error rates becomes small by increasing doping concentration in the drain regions for the FDSOI process. By increasing doping concentration, generated carriers remain in drain and the parasitic bipolar effect (PBE) is suppressed. PBE is also suppressed by decreasing the silicon thickness of the raised layer. The silicon portion in the raised layer disturbs carrier transportation. Thus the raised layer must be carefully designed considering the soft error resilience. The doping concentration and the raised layer are two key parameters to control the amount of charge generated through a particle hit in FDSOI. Simulation results show the cross section of the stacked FF is reduced to over 47.1% when doping concentration in drain regions is increased from 1×10^{20} cm^{-3} to 5×10^{20} cm^{-3}.

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