Radiation-Hardened Flip-Flops with Low Delay Overheads
Using PMOS Pass-Transistors to Suppress a SET Pulse in a 65 nm FDSOI Process
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Abstract—We propose radiation-hardened flip-flops (FFs) based on the adaptive coupling FF (ACFF) with low dynamic power and short delay overheads in a 65 nm Fully Depleted Silicon On Insulator (FDSOI) process. We designed four FFs composed of the master latch with PMOS pass-transistors to reduce delay time overheads and the slave latch with stacked transistors for high soft-error tolerance. We evaluated radiation hardness of those FFs by TCAD simulations and α irradiation test. The α irradiation results show that error probabilities of the proposed FFs are 1/400 - 1/130 smaller than the conventional radiation-hardened stacked FF. The experimental results show that PMOS pass-transistors can effectively suppress soft errors in the terrestrial region with a low-delay overhead.

I. Introduction
Highly-reliable semiconductor chips are key devices for autonomous driving and drivers assistance. According to technology downscaling, soft errors become a significant issue to threaten the reliability of semiconductor chips. They are mainly caused by α particles from package and neutrons from cosmic ray in the terrestrial region.

Highly-reliable devices need radiation-hardened flip-flops (FFs) against soft errors. Triple modular redundancy (TMR) [1] and dual interlocked storage cell (DICE) [2][3] are widely used for reliable chips. However, they have larger delay, area and power than conventional FFs. Thus, radiation-hardened FFs with small overheads are indispensable. Fully-depleted silicon on insulator (FDSOI) is a device-level mitigation technique against soft errors without any delay, area and power penalties. Single event latch-up (SEL) does not occur in FDSOI processes, because there is no parasitic bipolar structure to cause SEL [4]. FDSOI also have 50x - 110x higher tolerance for soft errors than bulk, because buried oxide (BOX) layers prevent charge from being collected from substrate [5].

In this paper, we propose several radiation-hardened FFs with small dynamic power and short delay overheads in a 65 nm FDSOI process. We evaluated the radiation hardness of the proposed FFs by TCAD simulations and α particle irradiation test. Section II explains the circuit structure of the low-power FF and proposed FFs. Section III shows simulation results by TCAD simulations. Section IV shows experimental results by particle test. Section V concludes this paper.

II. Radiation-Hardened Flip-Flops

Figure 1 shows a conventional FF called a transmission gate FF (TGFF). It has no tolerance against soft errors. Figure 2 depicts the adaptive coupling FF (ACFF) [6]. It has lower dynamic power than the TGFF, because it has no local clock buffer. The ACFF has AC elements, in which PMOS and NMOS transistors are connected in parallel to easily overwrite a stored value of the master latch (ML). Although they prolong delay time, they suppress a single event transient (SET) pulse when CLK = 1 [7]. NMOS pass-transistors suppress a SET pulse from PMOS transistors in the inverters (INV0, INV1), while PMOS pass-transistors suppress a SET pulse from NMOS transistors. However, the slave latch (SL) consists of two mutually-connected inverters without any transistors between them. To guarantee the radiation hardness of the ACFF, the SL must be strong against soft errors.

A. Conventional Radiation-Hardened Flip-Flop

Figure 3 shows the stacked FF [8]. It has inverters in latches composed of two series-connected NMOS and PMOS transistors. As shown in Fig. 4, stacked transistors in FDSOI are isolated by the BOX layer, while they are connected through substrate in bulk. When a radiation particle hits on the stacked inverter, its output does not flip unless both of NMOS transistors are influenced at the same time. Thus the stacked FF is strong against soft errors in FDSOI. However, stacked structure has 1.52x larger area and 1.97x delay overheads than the conventional inverter.

B. Proposed Radiation-Hardened Flip-Flops

1) Circuit Structure: We propose four radiation-hardened FFs based on the ACFF with high soft-error tolerance and short delay time. In Fig. 5, the proposed FF named pulse blocking low dynamic power FF (PBLDPFF) is shown.
NMOS transistors are weaker against soft errors than PMOS transistors mainly due to the difference of the mobility[9]. Pass-transistors between inverters suppress a SET pulse from inverters. PMOS pass-transistors are better to suppress a SET pulse because they can suppress a SET pulse from NMOS transistors which are more frequent than that from PMOS transistors. The ML of the PBLDPFF has only PMOS pass-transistors to suppress a SET pulse from NMOS transistors. The PMOS pass-transistors have a shorter delay time overhead than AC elements because they are always ON-state. The SL is composed of stacked inverters. They have a small impact on delay time because the ML is directly connected to INV3 through the NMOS pass-transistors. However, the PBLDPFF has the nodes N1 or N2 which become over the threshold voltage in all static conditions. In Fig. 6, the PBLDPFF has the nodes N1 or N2 which become over the threshold voltage in all static conditions. It is possible to suppress the static power of the PBLDPFF by applying back bias to body of NMOS transistors as Fig. 9 shows. The static power of the PBLDPFF is reduced by 90% at the substrate bias (VBN) of −1 V on NMOS transistors. Since the threshold of NMOS transistors at VBN = −1 V is 1.5x higher than that at VBN = 0 V, the short-circuit current through the inverter is decreased. The static power of the PBLDPFF is reduced by 70% when PMOS pass-transistors of the ML are replaced with low-threshold transistors.

The area overheads of the proposed FFs are bigger than that of the TGFF despite the same number of transistors. This is because that the proposed FFs contains different number of PMOS and NMOS transistors that generate unoccupied area. A 32-bit micro controller is synthesized from Register Transfer Level (RTL) by using the PBFF or the TGFF. Table II shows the synthesized results. The total area with the PBFF is only 7% bigger than that with the conventional area although the area of the PBFF is 47% bigger.

<table>
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<th>FF</th>
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<th>Area</th>
<th># of Tr.</th>
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<td>Static</td>
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III. TCAD Simulation Analyses

Three-dimensional TCAD simulations are carried out using the Synopsys Sentaurus to evaluate radiation hardness of the ML in the proposed FFs.

Figures 10 (a) and (b) depict the schematic at CLK = 1 and the cross section on device simulations of the ML. We evaluate soft error tolerance in outer space on TCAD simulations. The transistor is injected by heavy ions up to linear energy transfer (LET) of 60 MeV·cm$^2$/mg. This is because the number of particles with over 60 MeV·cm$^2$/mg is much less than those with less than 60 MeV·cm$^2$/mg in outer space [10].

By setting an initial value of N0 to 0 V, a particle with LET of 60 MeV·cm$^2$/mg hits at T3 at $V_{DD} = 0.8$ V. The stored value of the latch is not upset even though a particle has LET of 60 MeV·cm$^2$/mg which is 10x larger than the threshold LET (the minimum LET value at which the latch upsets) of the conventional latch under the same condition. In Fig. 11, voltage waveforms of N1 and N2 are shown. The amplitude of the SET pulse is attenuated by 45% after passing through the PMOS pass-transistor. This is because a PMOS pass-transistor cannot pass low levels signal under the threshold voltage.

IV. Experimental Results

A. Test Chip

Figure 12 shows the fabricated test chip in a 65 nm FDSOI process with thin BOX layers. It has 12 nm SOI and 10 nm BOX layers [11]. Test chip has triple-wells and well-contacts were inserted every 104 um to control substrate potential of transistors. All FFs are serially connected as a shift register.
The error bars are within 68% confidence. Down arrows means no error.

Figures 13 (a) and (b) show experimental results of $\alpha$ particle-induced EP at $V_{\text{DD}} = 0.4$ V and 0.8 V respectively. The EPs of the stacked FF are quoted from [12]. When CLK = 0, the ML holds data, while the SL holds data when CLK = 1. The PBFF_SN and the PBLDPFF_SN have slave latches which consist of stacked NMOS and unstacked PMOS transistors. No distinct difference is observed in the EPs of all proposed FFs at all static conditions. The maximum $N_{\text{error}}$ of all proposed FFs in 10 times of measurements is only 2 at $V_{\text{DD}} = 0.4$ V, and is 1 at $V_{\text{DD}} = 0.8$ V out of 60,320 - 69,600 FFs.

Figures 14 (a) and (b) show the averaged number of $\alpha$ particle-induced EPs of four all static conditions at $V_{\text{DD}} = 0.4$ V and 0.8 V. When $V_{\text{DD}} = 0.4$ V, The EPs of the stacked FF is 1/100 smaller than that of the TGFF. The EPs of proposed FFs are 1/60-1/35 smaller than that of the stacked FF. When $V_{\text{DD}} = 0.8$ V, the EPs of the stacked FF is 1/10 smaller than that of the TGFF. The EPs of all proposed FFs are 1/400 - 1/130 smaller than that of the stacked FF. All proposed FFs are stronger against soft errors by $\alpha$ particle than the stacked FF at $V_{\text{DD}} = 0.4$ V and 0.8 V.

V. Conclusion

We propose four FFs with PMOS pass-transistors in master latches and stacked inverters in slave latches. The PBLDPFF and the PBLDPFF_SN have almost same structure except for the stacking structure in slave latches. The PBLDPFF has inverters with stacked NMOS and PMOS transistors, while the
PBLDPFF\textsubscript{SN} has those with stacked NMOS and unstacked PMOS transistors. A SET pulse is effectively suppressed even in the PBLDPFF\textsubscript{SN} since NMOS transistors are more sensitive to a particle penetration than PMOS transistors. The PBFF and the PBFF\textsubscript{SN} are modified version the PBLDPFF and the PBLDPFF\textsubscript{SN}, respectively, which have clock buffers to decrease static power consumption and shorten delay time with an area overhead.

The PBFF\textsubscript{SN} and the PBLDPFF\textsubscript{SN} are strong against soft errors only injected from NMOS transistors. The PBFF and the PBFF\textsubscript{SN} have 30\% shorter delay and 15\% smaller dynamic power and 15\% smaller static power overheads than the conventional radiation-hardened stacked FF. The PBLDPFF and the PBLDPFF\textsubscript{SN} have 20\% shorter delay, 50\% smaller dynamic power but 35x higher static power overheads than the stacked FF. The static power can be suppressed by the reverse body bias or using low-threshold transistors.

We investigated their radiation hardness by $\alpha$ particle test. The $\alpha$ particle results show that error probabilities of the proposed FFs are 1/60 - 1/35 smaller than that of the stacked FF at $V_{\text{DD}} = 0.4$ V and they are 1/400 - 1/130 smaller than that of the stacked FF at $V_{\text{DD}} = 0.8$ V. These simulation and experiment results clearly show the proposed FFs have larger radiation hardness and smaller overheads than the stacked FF. It is possible to eliminate soft errors in the terrestrial region by using PMOS pass-transistors and the stacked inveter consist of stacked NMOS and unstacked PMOS transistors.

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REFERENCES