Radiation-Hardened Flip-Flops with Low Delay Overheads Using PMOS Pass-Transistors to Suppress a SET Pulse in a 65 nm FDSOI Process

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***Abstract*— We propose radiation-hardened flip-flops (FFs) based on the adaptive coupling FF (ACFF) with low dynamic power and short delay overheads in a 65 nm Fully Depleted Silicon On Insulator (FDSOI) process. We designed four FFs composed of the master latch with PMOS pass-transistors to reduce delay time overheads and the slave latch with stacked transistors for high soft-error tolerance. We evaluated radiation hardness of those FFs by TCAD simulations and α irradiation test. The α irradiation results show that error probabilities of the proposed FFs are 1/400 - 1/130 smaller than the conventional radiation-hardened stacked FF. The experimental results show that PMOS pass-transistors can effectively suppress soft errors in the terrestrial region with a low-delay overhead.**

I. Introduction

Highly-reliable semiconductor chips are key devices for autonomous driving and drivers assistance. According to technology downscaling, soft errors become a significant issue to threaten the reliability of semiconductor chips. They are mainly caused by α particles from package and neutrons from cosmic ray in the terrestrial region.

Highly-reliable devices need radiation-hardened flip-flops (FFs) against soft errors. Triple modular redundancy (TMR) [1] and dual interlocked storage cell (DICE) [2][3] are widely used for reliable chips. However, they have larger delay, area and power than conventional FFs. Thus, radiation-hardened FFs with small overheads are indispensable. Fully-depleted silicon on insulator (FDSOI) is a device-level mitigation technique against soft errors without any delay, area and power penalties. Single event latch-up (SEL) does not occur in FDSOI processes, because there is no parastic bipolar structure to cause SEL [4]. FDSOI also have 50x - 110x higher tolerance for soft errors than bulk, because buried oxide (BOX) layers prevent charge from being collected from substrate [5].

In this paper, we propose several radiation-hardened FFs with small dynamic power and short delay overheads in a 65 nm FDSOI process. We evaluated the radiation hardness of the proposed FFs by TCAD simulations and α particle irradiation test. Section II explains the circuit structure of the low-power FF and proposed FFs. Section III shows simulation results by TCAD simulations. Section IV shows experimental results by α particle test. Section V concludes this paper.

II. Radiation-Hardened Flip-Flops

Figure 1 shows a conventional FF called a transmission gate FF (TGFF). It has no tolerance against soft errors. Figure 2 depicts the adaptive coupling FF (ACFF) [6]. It has lower dynamic power than the TGFF, because it has no local clock buffer. The ACFF has AC elements, in which PMOS and NMOS transistors are connected in parallel to easily overwrite a stored value of the master latch (ML). Although they prolong delay time, they suppress a single event transient (SET) pulse when CLK = 1 [7]. NMOS pass-transistors suppress a SET

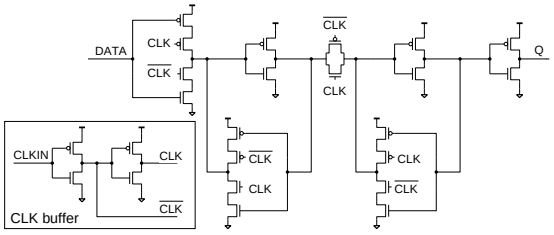


Fig. 1. Transmission-gate FF (TGFF).

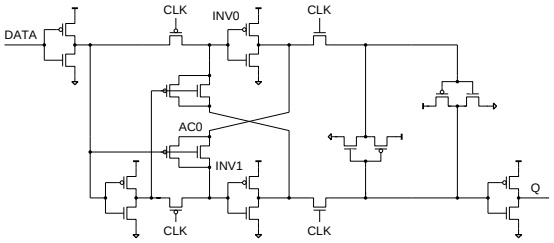


Fig. 2. Adaptive Coupling FF (ACFF).

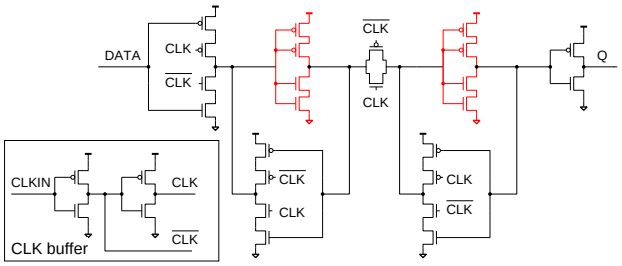


Fig. 3. Stacked FF.

pulse from PMOS transistors in the inverters (INV0, INV1), while PMOS pass-transistors suppress a SET pulse from NMOS transistors. However, the slave latch (SL) consists of two mutually-connected inverters without any transistors between them. To guarantee the radiation hardness of the ACFF, the SL must be strong against soft errors.

A. Conventional Radiation-Hardened Flip-Flop

Figure 3 shows the stacked FF [8]. It has inverters in latches composed of two series-connected NMOS and PMOS transistors. As shown in Fig. 4, stacked transistors in FDSOI are isolated by the BOX layer, while they are connected through substrate in bulk. When a radiation particle hits on the stacked inverter, its output does not flip unless both of NMOS transistors are influenced at the same time. Thus the stacked FF is strong against soft errors in FDSOI. However, stacked structure has 1.52x larger area and 1.97x delay overheads than the conventional inverter.

B. Proposed Radiation-Hardened Flip-Flops

1) Circuit Structure: We propose four radiation-hardened FFs based on the ACFF with high soft-error tolerance and short delay time. In Fig. 5, the proposed FF named pulse blocking low dynamic power FF (PBLDPFF) is shown.

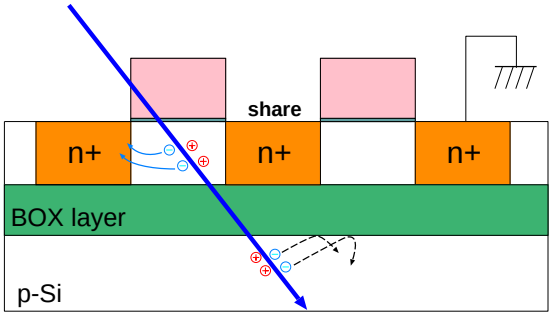


Fig. 4. The cross section of NMOS transistors in stacked invertes.

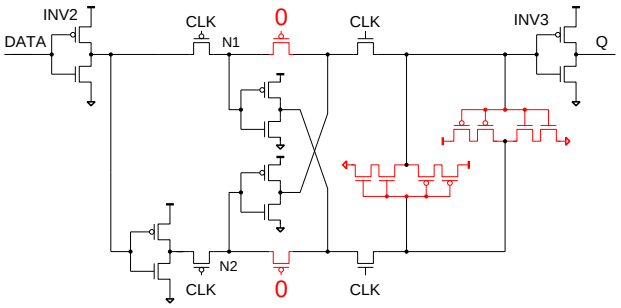


Fig. 5. Pulse Blocking Low Dynamic Power FF (PBLDPFF).

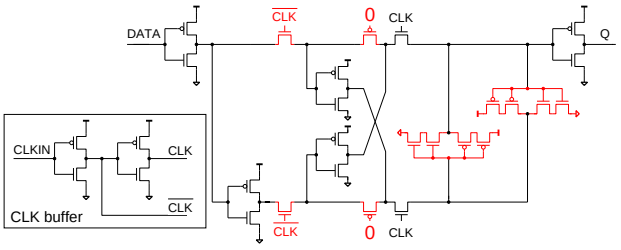


Fig. 6. Pulse Blocking FF (PBFF).

NMOS transistors are weaker against soft errors than PMOS transistors mainly due to the difference of the mobility[9]. Pass-transistors between inverters suppresses a SET pulse from inverters. PMOS pass-transistors are better to suppress a SET pulse because they can suppress a SET pulse from NMOS transistors which are more frequent than that from PMOS transistors. The ML of the PBLDPFF has only PMOS pass-transistors to suppress a SET pulse from NMOS transistors. The PMOS pass-transistors have a shorter delay time overhead than AC elements because they are always ON-state. The SL is composed of stacked inverters. They have a small impact on delay time because the ML is directly connected to INV3 through the NMOS pass-transistors. However, the PBLDPFF has the nodes N1 or N2 which become over the threshold voltage in all static conditions. In Fig. 6, the proposed FF named pulse blocking FF (PBFF) is shown. PMOS pass-transistors between the ML and INV2 in the PBFF are replaced with NMOS pass-transistors in order to stabilize the potential on N1 and N2. However, it must have a local clock buffer. Figures 7 and 8 depict the PBLDPFF with stacked NMOS described as the PBLDPFF_SN and the PBFF with stacked NMOS called the PBFF_SN. They have stacked inverters in the SL composed of two NMOS and one PMOS transistors. It is because PMOS transistors are stronger against soft errors than NMOS transistors. They has smaller area overhead than stacked inverters composed of two NMOS and PMOS transistors.

2) Performance of Proposed Flip-Flops: We measure D-Q delays and power consumptions of FFs by SPICE simulation at supply voltage (V_{DD}) of 1.2 V. Table I indicates the simulation results of delay time, dynamic power at 10% data activity, static power, area and the number of transistors. All values except for the number of transistors are normalized to those of the TGFF. The values in parentheses are normalized to those of the stacked FF.

The delay time of the stacked FF is 1.66x higher than that of TGFF because stacked inverters both in the ML and the SL worsen its delay time. The delay time of the proposed FFs are about 10% shorter than that of the ACFF because the delay times of AC elements depend on an input value.

The dynamic and static power of the PBFF and the PBFF_SN are almost same as that of the TGFF. The dynamic power of the PBLDPFF and the PBLDPFF_SN are almost same as that of the ACFF. This is because they have no local clock buffer. However, the static power of them are about 40x higher than that of the TGFF, because some nodes become over the threshold voltage in static conditions. It is possible to suppress the static power of the PBLDPFF by applying back bias to body of NMOS transistors as Fig. 9 shows. The static power of the PBLDPFF is reduced by 90% at the substrate bias (VBN) of -1 V on NMOS transistors. Since the threshold of NMOS transistors at VBN = -1 V is 1.5x higher than that at VBN = 0 V, the short-circuit current through the inverter is decreased. The static power of the PBLDPFF is reduced by 70% when PMOS pass-transistors of the ML are replaced with low-threshold transistors.

TABLE I

SIMULATION RESULTS AT V_{DD} = 1.2 V OF D-Q DELAY, POWER ,AREA AND NUMBER OF TRANSISTOR OF EACH FF. ALL VALUES EXCEPT FOR THE NUMBER OF TRANSISTORS ARE NORMALIZED TO THOSE OF THE TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF THE STACKED FF.

FF	D-Q delay	Power consumption		Area	# of Tr.
		Dynamic	Static		
TGFF	1	1	1	1	24
ACFF	1.44	0.470	2.35	1.00	22
Stacked FF	1.66	1.02	1.13	1.12	28
PBFF	1.19 (0.72)	0.872 (0.86)	0.926 (0.82)	1.47 (1.31)	28
PBFF_SN	1.17 (0.71)	0.872 (0.86)	0.970 (0.86)	1.47 (1.31)	26
PBLDPFF	1.30 (0.78)	0.488 (0.48)	38.9 (34.4)	1.29 (1.15)	24
PBLDPFF_SN	1.38 (0.83)	0.483 (0.47)	41.8 (37.0)	1.18 (1.05)	22

The area overheads of the proposed FFs are bigger than that of the TGFF despite the same number of transistors. This is because that the proposed FFs contains different number of PMOS and NMOS transistors that generate unoccupied area. A 32-bit micro controller is synthesized from Register Transfer Level (RTL) by using the PBFF or the TGFF. Table II shows the synthesized results. The total area with the PBFF is only 7% bigger than that with the conventional area although the area of the PBFF is 47% bigger.

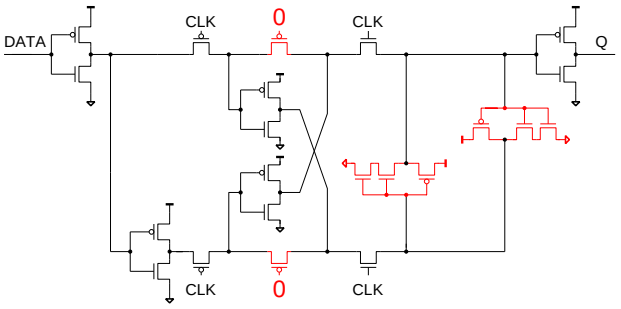


Fig. 7. Pulse Blocking Low Dynamic Power FF with Stacked NMOS (PBLDPFF_SN).

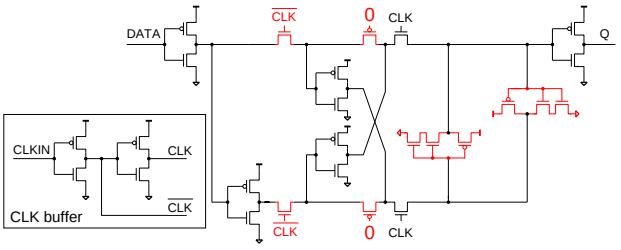


Fig. 8. Pulse Blocking FF with Stacked NMOS (PBFF_SN).

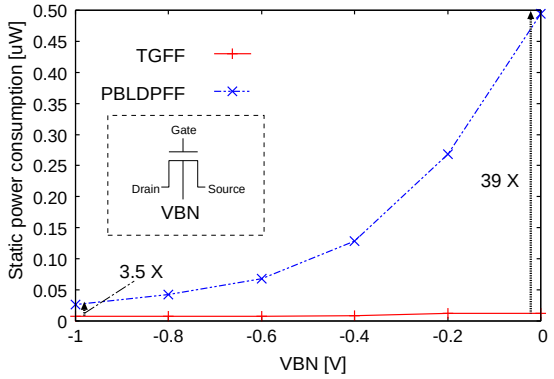


Fig. 9. The static power of the PBLDPFF depending on substrate bias (VBN) of NMOS transistors.

TABLE II

SYNTHESIZED AREA OF A 32-BIT MICRO CONTROLLER NORMALIZED BY THE TGFF.

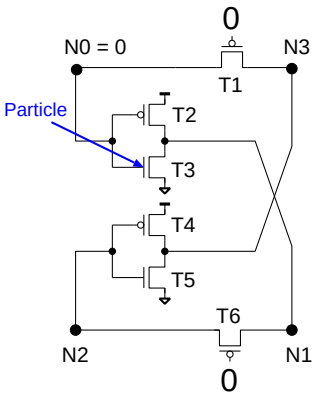
	TGFF	PBFF
Conmbinational	0.7	0.69
Flip-flops	0.3	0.38
Total	1	1.07

III. TCAD Simulation Analyses

Three-dimensional TCAD simulations are carried out using the Synopsys Sentaurus to evaluate radiation hardness of the ML in the proposed FFs.

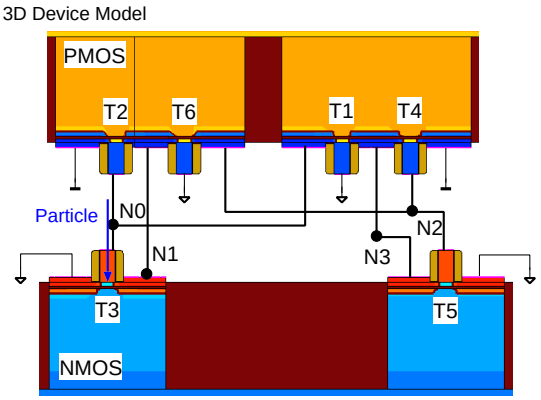
Figures 10 (a) and (b) depict the schematic at CLK = 1 and the cross section on device simulations of the ML. We evaluate soft error tolerance in outer space on TCAD simulations. The transistor is injected by heavy ions up to liner energy transfer (LET) of 60MeV-cm^2/mg . This is because the number of particles with over 60MeV-cm^2/mg is much less than those with less than 60MeV-cm^2/mg in outer space [10].

By setting an initial value of N0 to 0 V, a particle with LET of 60 MeV-cm^2/mg hits at T3 at V_{DD} = 0.8 V. The stored value of the latch is not upset even though a particle has LET of 60 MeV-cm^2/mg which is 10x larger than the threshold LET (the minimum LET value at which the latch upsets) of



Tr. No.	W / L [nm]
T1	450 / 60
T2	320 / 60
T3	230 / 60
T4	450 / 60
T5	345 / 60
T6	365 / 60

(a) Schematic



(b) Cross section

Fig. 10. Schematic (a) and cross section (b) on device simulations of the ML. By setting the initial value of N0 to 0 V, a heavy ion hits at T3 at V_{DD} = 0.8 V. The transistor width and length are shown beside the schematic figure.

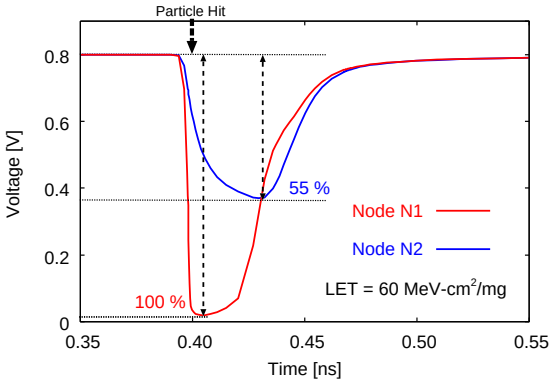


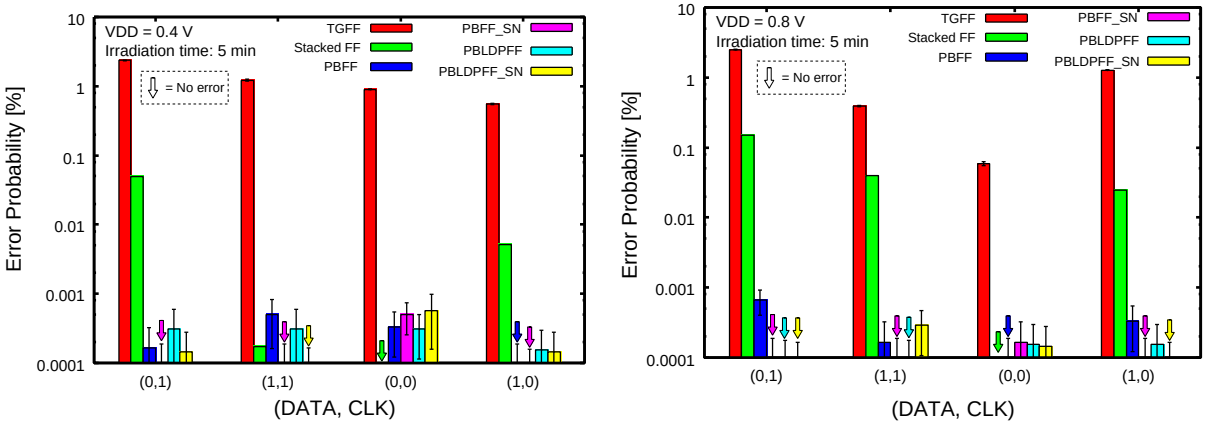
Fig. 11. TCAD simulations results. N1 and N2 are influenced by a particle hits in Fig. 10. The ML of proposed FFs is not upset up to LET = 60 MeV-cm^2/mg .

the conventional latch under the same condition. In Fig. 11, voltage waveforms of N1 and N2 are shown. The amplitude of the SET pulse is attenuated by 45% after passing through the PMOS pass-transistor. This is because a PMOS pass-transistor cannot pass low levels signal under the threshold voltage.

IV. Experimental Results

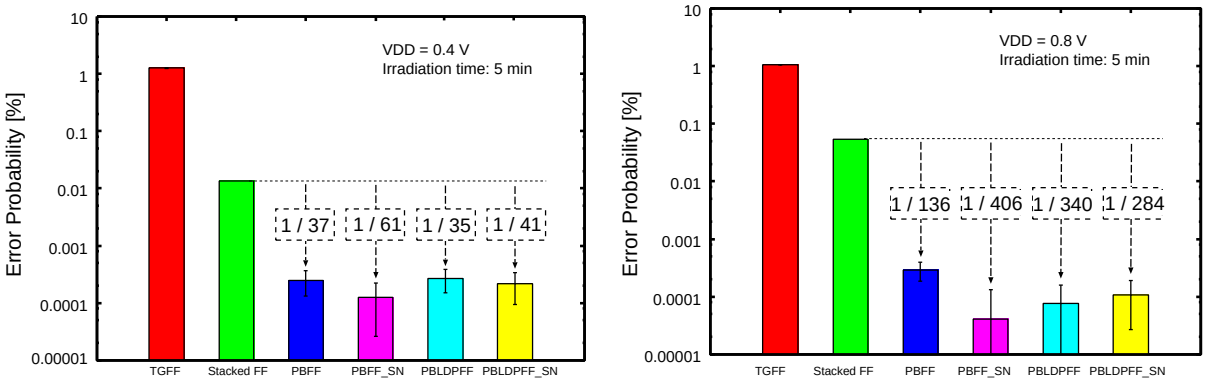
A. Test Chip

Figure 12 shows the fabricated test chip in a 65 nm FDSOI process with thin BOX layers. It has 12 nm SOI and 10 nm BOX layers [11]. Test chip has triple-wells and well-contacts were inserted every 104 um to control substrate potential of transistors. All FFs are serially connected as a shift register.



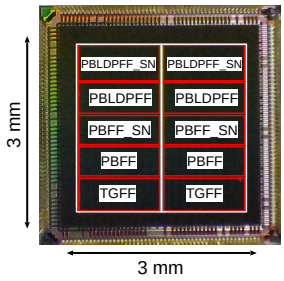
(a) V_{DD} = 0.4 V (b) V_{DD} = 0.8 V

Fig. 13. Experimental results of α particle-induced error probabilities at each condition. The error bars are within 68% confidence. Down arrows means no error.



(a) V_{DD} = 0.4 V (b) V_{DD} = 0.8 V

Fig. 14. Averaged α particle-induced error probabilities of all four static conditions. The worst values in error bars of the proposed FFs are compared with the true value of the stacked FF.



Flip-Flop	bit/chip
TGFF	83,520
PBFF	60,320
PBFF_SN	60,320
PBLDPFF	64,960
PBLDPFF_SN	69,600

Fig. 12. Fabricated chips in a 65 nm FDSOI process with thin BOX layers.

B. α Particle Irradiation

α particle irradiation tests were carried out using a 3 MBq ^{241}Am. All measurement were done by repeating to initialize all FFs, put the α source on a chip for five minutes and read data after removing the α source. We measure the radiation hardness at these static conditions (DATA, CLK) = (0, 1), (1, 1), (0, 0) and (1,0) to evaluate all possible states. The error probability (EP) is used in order to evaluate soft-error tolerances and calculated by Eq. 1. Measurements were carried out for 10 times in each condition and these data are averaged. The error bars are within 68% confidence.

$$EP = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}}} \tag{1}$$

The EP is calculated from the number of errors (N_{error}) and the number of FFs (N_{FF}).

Figures 13 (a) and (b) show experimental results of α particle-induced EP at V_{DD} = 0.4 V and 0.8 V respectively. The EPs of the stacked FF are quoted from [12]. When CLK = 0, the ML holds data, while the SL holds data when CLK = 1. The PBFF_SN and the PBLDPFF_SN have slave latches which consist of stacked NMOS and unstacked PMOS transistors. No distinct difference is observed in the EPs of all proposed FFs at all static conditions. The maximum N_{error} of all proposed FFs in 10 times of measurements is only 2 at V_{DD} = 0.4 V, and is 1 at V_{DD} = 0.8 V out of 60,320 - 69,600 FFs.

Figures 14 (a) and (b) show the averaged number of α particle-induced EPs of four all static conditions at V_{DD} = 0.4 V and 0.8 V. When V_{DD} = 0.4 V, The EPs of the stacked FF is 1/100 smaller than that of the TGFF. The EPs of proposed FFs are 1/60-1/35 smaller than that of the stacked FF. When V_{DD} = 0.8 V, the EP of the stacked FF is 1/10 smaller than that of the TGFF. The EPs of all proposed FFs are 1/400 - 1/130 smaller than that of the stacked FF. All proposed FFs are stronger against soft errors by α particle than the stacked FF at V_{DD} = 0.4 V and 0.8 V.

V. Conclusion

We propose four FFs with PMOS pass-transistors in master latches and stacked inverters in slave latches. The PBLDPFF and the PBLDPFF_SN have almost same structure except for the stacking structure in slave latches. The PBLDPFF has inverters with stacked NMOS and PMOS transistors, while the

PBLDPFF_SN has those with stacked NMOS and unstacked PMOS transistors. A SET pulse is effectively suppressed even in the PBLDPFF_SN since NMOS transistors are more sensitive to a particle penetration than PMOS transistors. The PBFF and the PBFF_SN are modified version the PBLDPFF and the PBLDPFF_SN, respectively, which have clock buffers to decrease static power consumption and shorten delay time with an area overhead.

The PBFF_SN and the PBLDPFF_SN are strong against soft errors only injected from NMOS transistors. The PBFF and the PBFF_SN have 30% shorter delay and 15% smaller dynamic power and 15% smaller static power overheads than the conventional radiation-hardened stacked FF. The PBLDPFF and the PBLDPFF_SN have 20% shorter delay, 50% smaller dynamic power but 35x higher static power overheads than the stacked FF. The static power can be suppressed by the reverse body bias or using low-threshold transistors.

We investigated their radiation hardness by α particle test. The α particle results show that error probabilities of the proposed FFs are 1/60 - 1/35 smaller than that of the stacked FF at $V_{\rm DD}$ = 0.4 V and they are 1/400 - 1/130 smaller than that of the stacked FF at $V_{\rm DD}$ = 0.8 V. These simulation and experiment results clearly show the proposed FFs have larger radiation hardness and smaller overheads than the stacked FF. It is possible to eliminate soft errors in the terrestrial region by using PMOS pass-transistors and the stacked inveter consist of stacked NMOS and unstacked PMOS transistors.

Acknowledgment: The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC) in collaboration with Renesas Electronics Corporation, Cadence Corporation, Synopsys Corporation and Mentor Graphics Corporation. This work is supported by Socionext and JSPS KAKENHI Grant Number 15H02677.

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