A Non-Redundant Low-Power Flip Flop with Stacked Transistors in a 65 nm Thin BOX FDSOI Process

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***Abstract*— We propose a non-redundant Flip-Flop (FF) with stacked transistors based on Adaptive Coupling Flip-Flop (ACFF) with lower power consumption in a 65 nm Fully Depleted Silicon On Insulator (FDSOI) process. The slave latch in ACFF is much weaker against soft errors than the master latch. We design several FFs with stacked transistors in the master or slave latches. We investigate radiation hardness of the proposed FFs by α particle and neutron irradiation test. The proposed FFs have higher radiation hardness than conventional DFF. There is no error in the proposed AC slave stacked FF which has stacked transistors only in the slave latch by α particle and neutron irradiation test. It can decrease soft error rates despite the performance equivalent to that of ACFF.**

I. Introduction

As transistors become downscaling, the reliability of semiconductor chips has become serious by soft errors. They are caused by α particles from package and neutrons from cosmic ray. Highly reliable devices have to equip preventions against soft errors. There are some examples of such devices, including High Performance Computing (HPC) and aerospace. Power consumption of semiconductor chips have also become serious in HPC. The 2.3 GHz PowerEN chip is running at 1.6 GHz and a reduced voltage to fulfill power budget [1]. TMRFF [2], BISER [3] and DICEFF [4], which are redundant Flip-Flop (FF), are proposed to prevent soft errors. However, they have larger delay time, area and power overhead than non-redundant FFs. Therefore, non-redundant FFs with radiation hardness are indispensable.

Fully-Depleted Silicon On Insulator (FDSOI) processes decreases Soft Error Rates (SERs) without any performance overhead. They have smaller threshold voltage variations than bulk processes due to its undoped channel. Therefore, they can operate at lower supply voltage. In addition, transistors in FDSOI processes collect smaller charge to drain than bulk processes because Buried Oxide (BOX) layers prevent charge collection. Thus, they also have 50-110x higher soft error tolerance without any circuit level mitigation techniques [5].

In this paper, we propose non-redundant radiation-hardened FFs in a 65 nm FDSOI process. We also investigate the radiation hardness of the proposed FFs by α particle and neutron irradiation. Section II explains the circuit of the low power FF and proposed FFs. Section III shows experimental results by α particle and spallation neutron irradiation test. Section IV concludes this paper.

II. Low-Power Radiation-Hardened Flip-Flop

A. Unhardened Standard Flip-Flops

Fig. 1 shows conventional DFF with a transmission-gate (TGFF). Upset transistors by radiation depend on DATA and CLK states. When (DATA, CLK) = (0, 0) and (1, 1), the inverter is vulnerable. When (DATA, CLK) = (0, 1) and (1, 0), the tri-state inverter is vulnerable.

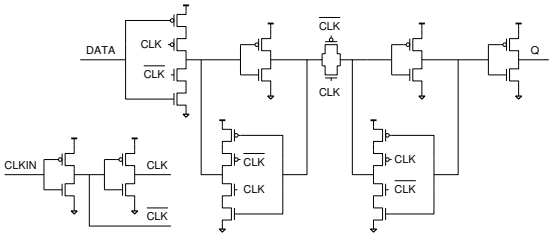


Fig. 1. Transmission-gate FF (TGFF).

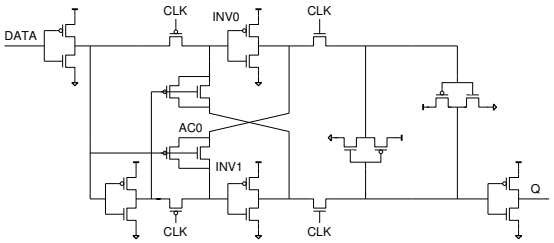


Fig. 2. Adaptive Coupling FF (ACFF).

Fig. 2 shows Adaptive Coupling Flip-Flop (ACFF) [6]. It has pass transistors instead of transmission gates or tri-state inverters. It has no local clock buffer for $\overline{\mathrm{CLK}}$ which consumes large amount of power consumption in FFs. Therefore, it consumes lower power than TGFF. ACFF has AC element, in which PMOS and NMOS are connected in parallel to easily overwrite a stored value in Master Latch (ML). When CLK = 0, the value is transferred to Slave Latch (SL). When CLK = 1, the stored values in ML and SL are equivalent.

The radiation hardness is evaluated by Q_{crit} with SPICE simulations [7]. We connect a current source to a circuit node to estimate the Q_{crit}, which follows the single exponential model with time constant of 10 ps. We determine injected charge as Q_{crit} when stored value flips. Fig. 3 shows the simulation results at 0.8 V depending on DATA and CLK states. When CLK = 0, Q_{crit} of ACFF is almost same compared with that of TGFF. On the other hand, when CLK = 1, Q_{crit} of ACFF is higher than that of TGFF. The reason why the difference is due to AC elements in ML. We assume that a radiation particle hits on NMOS of INV0 in ML when (DATA, CLK) = (1, 1). At this condition, the PMOS pass transistor of AC0 and PMOS of INV0 turn on as shown in Fig. 4(a). High-level signals can pass through the PMOS pass transistor. In contrast, it is difficult for low-level signals to pass through the PMOS pass transistor. If the output of INV0 becomes low by a particle hit, a Single Event Transient (SET) pulse is suppressed to propagate INV1. Fig. 4(b) shows the waveform of SET pulse before and after passing through the PMOS pass transistor when the current source injects from 3 fC to 9 fC. The amplitude of SET pulse becomes smaller after it passes through P1 as shown in Fig. 4(b). Therefore,

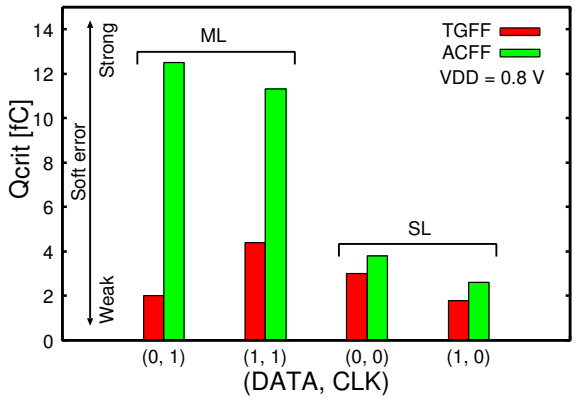


Fig. 3. Q_{crit} simulation results at 0.8 V depending on DATA and CLK state. ML and SL show weak components to soft errors in FF.

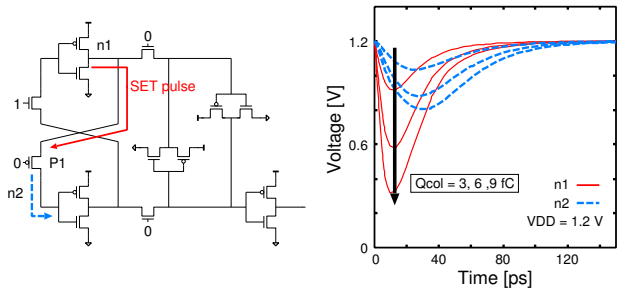


Fig. 4. SET pulse can be suppressed through AC element. Q_{col} stands for the injected charge.

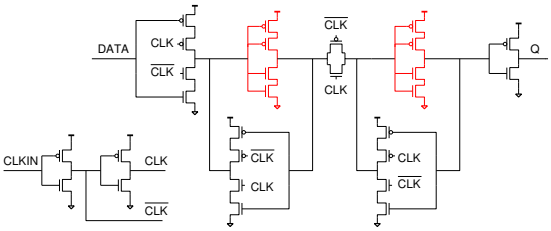


Fig. 5. Conventional stacked FF.

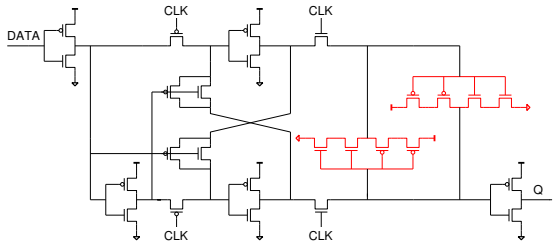
ACFF has higher radiation hardness when CLK = 1. However, ACFF must prevent soft errors in SL when CLK = 0.

B. Radiation Hardened Flip-Flop with Stacked Transistors

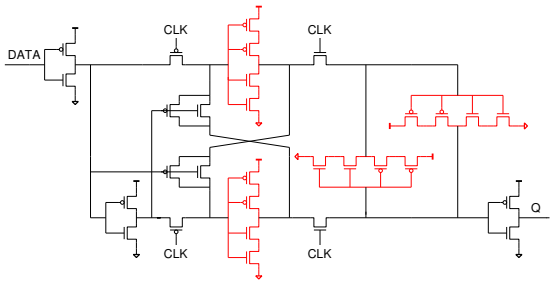
Parasitic bipolar effect (PBE) significantly causes soft errors in SOI devices. A stacked inverter is proposed for SOI (Silicon On Insulator) as a prevention against soft errors, which is composed of two NMOS and PMOS transistors [8]. It is stronger against soft errors than a standard inverter. It is almost impossible that both of NMOS transistors upset by PBE as the same time because they are isolated by BOX layers and Shallow Trench Isolation (STI). Therefore, it prevents soft errors. However, it has area and delay time overhead if all inverters are replaced with stacked inverters. Fig. 5 shows Stacked FF [8]. It can prevent soft errors which occur in the inverters.

C. Proposed Radiation Hardened Flip-Flop Based on ACFF

Fig. 6(a) shows the proposed FF with stacked inverters only in SL called AC Slave Stacked FF (AC_SS FF). Fig. 6(b) shows another FF with stacked transistors in both ML and



(a) AC Slave Stacked FF (AC_SS FF)



(b) AC All Stacked FF (AC_AS FF).

Fig. 6. Proposed FFs based on ACFF.

SL called AC All Stacked FF (AC_AS FF) to compare with radiation hardness of AC_SS FF.

As described in Section II-A, ACFF is sensitive to soft errors in SL. AC_SS FF can suppress soft errors in SL. It also has equivalent performance of ACFF. Stacked inverters in SL do not affect its D-Q delay time because Q is connected to ML through the output port by NMOS pass transistors. However, ML may become weaker than SL. AC_AS FF can suppress soft errors in both ML and SL. But, it has some amount of D-Q delay and area overhead due to stacked inverters in ML.

Table I indicates the simulation results of area, delay time, power consumption at 10% data activity and the number of transistors. All values are normalized to those of TGFF. The values in parentheses are normalized to those of ACFF. The performance of Stacked FF is larger than that of TGFF. Especially, the delay time of Stacked FF is 1.49x compared with that of TGFF because stacked inverters in ML and SL affect its delay time. The area of AC_SS FF and AC_AS FF are bigger than ACFF due to the increase of the number of transistors. The D-Q delay of AC_SS FF is almost same as that of ACFF. That of AC_AS FF is 1.47x compared with ACFF because stacked inverters in ML increase its D-Q delay time. The dynamic power consumption of all ACFFs is equivalent. AC_SS FF has lower delay overhead than stacked FF.

Fig. 7 shows the simulation results of power consumption of each FF depending on data activity. Data activity is the probability that the output node of FF changes from 0 to 1 or from 1 to 0. The power consumptions of ACFFs are lower than that of TGFF in lower data activity. In contrast, the power consumptions of ACFFs are equivalent to that of TGFF in higher data activity. Stacked FF consumes the highest power among all FFs at any data activities.

Fig. 8 shows the fabricated chips in a 65 nm Silicon On Thin BOX (SOTB) [9] process which has 12 nm SOI and 10 nm BOX layers. We measure radiation hardness using fabricated chips as shown Table II.

TABLE I

SIMULATION RESULTS OF AREA, D-Q DELAY, POWER AND NUMBER OF TRANSISTOR OF EACH FF. ALL VALUES ARE NORMALIZED TO THOSE OF TGFF. THE VALUES IN PARENTHESES ARE NORMALIZED TO THOSE OF ACFF.

FF	Area	D-Q delay	Power	# of Tr.
TGFF	1	1	1	24
Stacked FF	1.12	1.49	1.02	28
ACFF	1.00	1.46	0.55	22
AC_SS FF	1.12 (1.12)	1.50 (1.03)	0.58 (1.05)	26
AC_AS FF	1.24 (1.24)	2.14 (1.47)	0.58 (1.07)	28

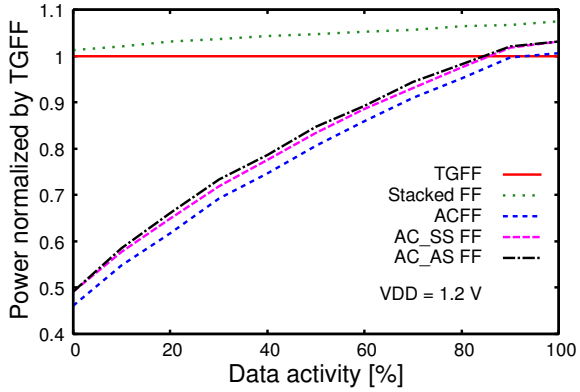
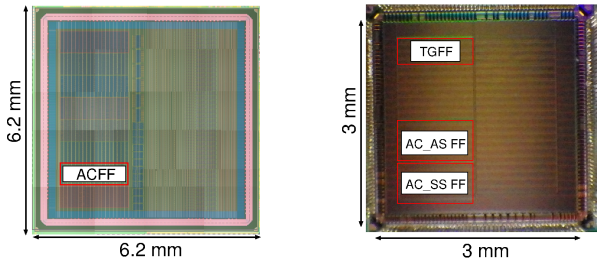


Fig. 7. Power consumption of each FF depending on data activity. All values are normalized to those of TGFF.

TABLE II

NUMBER OF CONTAINED FF IN EACH CHIP.

	FF
Chip (a) in Fig. 8(a)	ACFF (40,320 bit)
Chip (b) in Fig. 8(b)	TGFF (23,976 bit) AC_SS FF (41,760 bit) AC_AS FF (39,150 bit)
Chip (c) [10]	Stacked FF (99,360 bit)



(a) (b)

Fig. 8. Fabricated chips in the 65 nm SOTB process.

III. Experimental Results

A. α Particle Irradiation

α particle irradiation tests are carried out using a 3 MBq ^{241}Am. The irradiation time is one minute. We measure the radiation hardness at these static conditions (DATA, CLK) = (0, 1), (1, 1), (0, 0) and (1, 0).

Fig. 9 shows experimental results of α particle-induced SER. The error bars are within 68% confidence. The SERs of ACFF show the same trend as $Q_{\rm crit}$ simulations. SL of ACFF is weak against soft errors. On the other hand, there is no error in ML and SL of the proposed FFs. We can eliminate soft errors by α particle to replace inverters with stacked inverters in SL.

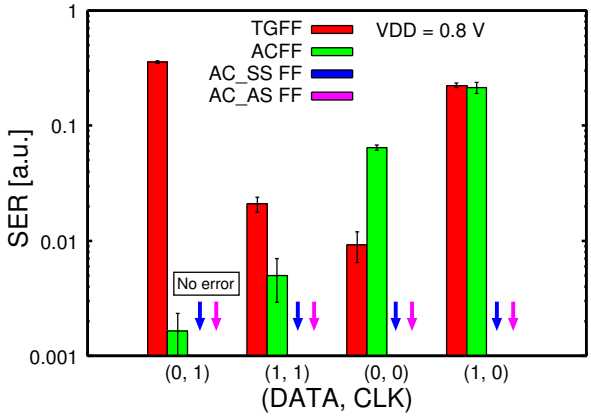


Fig. 9. Experimental results of α particle-induced SER at each condition. The error bars are within 68% confidence.

B. Spallation Neutron Irradiation

The spallation neutron experiments were carried out at Research Center for Nuclear Physics (RCNP). To increase the number of upset FFs, stacked DUT (Device Under Test) boards with four test chips are used. We measure SERs at these static conditions (DATA, CLK) = (0, 1), (1, 1), (0, 0) and (1, 0). There is no data of AC_SS FFs and AC_AS FFs when (DATA, CLK) = (1, 1) and (1, 0) because of limited beam time. It is sufficient because they have vertically-symmetrical structures. All measurement were done by repeating to initialize all FFs, and read data after five minutes. The neutron tests are carried out using chip (a) and chip (b) in Fig. 8 Acceleration factors of chip (a) and chip (b) measurement are 3.8×10^8 and 3.9×10^8 respectively compared with the sea level at NYC. The experimental results of stacked FF are quoted from [10].

To increase the number of soft errors, neutron irradiation tests were carried out at lower supply voltage. Fig. 10 (a) and 10 (b) show neutron-induced SERs at 0.4 V and 0.8 V respectively. The error bars are within 68% confidence. Table III indicates the details of neutron-induced SERs at each condition. Stacked FF can decrease SERs to 11% compared with TGFF at 0.8 V when (DATA, CLK) = (1, 1). It is an effective method to decrease SER. The SERs of ACFF are higher than those of TGFF at lower supply voltage when CLK = 0 as shown in Fig. 10 (a). Except for AC_AS FF at 0.4 V when (DATA, CLK) = (0, 0), there is no error in the proposed FFs at all conditions. We can eliminate soft errors by replacing inverters with stacked inverters only in SL.

IV. Conclusion

We propose FFs with stacked transistors in SL based on ACFF in a 65 nm FDSOI process. The proposed FF with stacked transistors only in SL has only 12% area, 3% D-Q delay and 5% power overhead compared with ACFF. We investigated its radiation hardness by α particle and neutron irradiation tests. There was no error at static conditions of DATA and CLK states. It can suppress soft errors by α particles and neutrons. It has larger radiation hardness and smaller overhead than conventional stacked FF.

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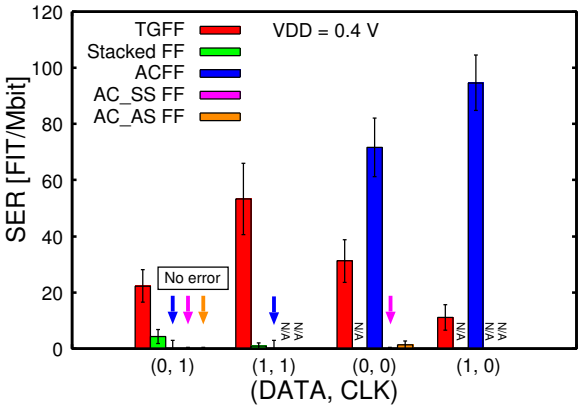
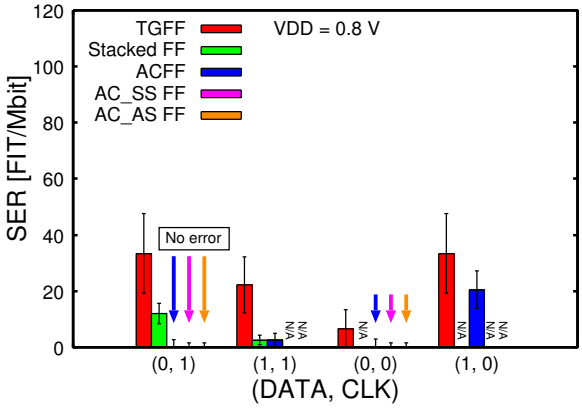


(a) VDD = 0.4 V



(b) VDD = 0.8 V

Fig. 10. Neutron irradiation results at each condition. The error bars are within 68% confidence. There is no data of AC_SS FFs and AC_AS FFs when (DATA, CLK) = (1, 1) and (1, 0).

TABLE III

DETAILS OF NEUTRON-INDUCED SERS AT EACH CONDITION.

	SER [FIT/Mbit] (0.4 V)				SER [FIT/Mbit] (0.8 V)			
(DATA, CLK)	(0, 1)	(1, 1)	(0, 0)	(1, 0)	(0, 1)	(1, 1)	(0, 0)	(1, 0)
TGFF	22.3	53.4	31.2	11.1	33.4	22.3	6.7	33.4
Stacked FF	4.4	1.0	N/A	N/A	12.1	2.6	N/A	N/A
ACFF	0	0	71.7	94.7	0	2.6	0	20.5
AC_SS FF	0	N/A	0	N/A	0	N/A	0	N/A
AC_AS FF	0	N/A	1.4	N/A	0	N/A	0	N/A

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