

A Radiation-Hardened Non-redundant Flip-Flop, Stacked Leveling Critical Charge Flip-Flop in a 65 nm Thin BOX FD-SOI Process

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Abstract— We propose SLCCFF which is a radiation hardened non-redundant flip-flop in 65 nm SOTB (Silicon On Thin BOX) process. We measured its soft error rates by neutron irradiation. SLCCFF has the stacked structure to prevent soft errors on SOI processes while maintaining smaller delay and power overhead than conventional stacked FFs. Experimental results show that the SLCCFF is about 27x stronger than the standard DFF at 0.4V power supply in the SOTB process. It is about 1000x stronger compared with the standard DFF in the bulk process.

I. Introduction

With the process scaling down to nanometers, LSIs are less reliable soft errors. Soft errors are caused by a particle hit from cosmic ray and α particles. Since soft errors can be recovered by reboot or reset, they become dominant on products demanding higher reliability such as super computers, automobiles and aircrafts. To protect FFs from soft errors, several redundant circuits are proposed such as TMR[1], DICE[2] and BCDMR[3]. But redundant FFs have large power consumption and area overhead. Therefore soft-error mitigation technique without redundancy is highly needed. We propose a non-redundant flip-flop highly reliable to soft errors. To estimate its soft error rate, we fabricated a test chip in 65 nm SOTB (Silicon On Thin Buried Oxide) CMOS process.

In this paper, we optimize energy and delay of non-redundant FFs with the downhill simplex algorithm. we also show the measurement results of soft error rates (SERs) of the proposed and conventional FFs by the spallation neutron irradiation. Section II show the structure of the proposed circuit. Section III show the experimental method and measurement results of neutron-induced SEUs and α -particle irradiation. Section IV concludes this paper.

II. The proposed circuit structure and delay time

In this section, we explain the detailed structure of the proposed non-redundant FFs and evaluate its delay time and energy consumption from circuit-level simulation.

A. The proposed SLCCFF on SOTB

Fig. 1 shows the cross section of the SOTB process with 10nm BOX (Buried OXide) layers under 12nm FD-SOI (Fully-Depleted Silicon On Insulator) layers. It demonstrates very small variability and back-bias control to reduce variations[4]. In addition, bulk transistors can be easily integrated by removing the thin BOX layers[5].

Fig. 2(a) and (b) show a standard inverter and a stacked inverter. In SOI processes, the stacked inverter becomes much stronger to soft errors[6]. It is because these stacked transistors are fully separated by STI (Shallow Trench Isolation) and BOX layers. Neither parasitic bipolar action nor charge sharing happens simultaneously among these two stacked transistors.

Fig. 3 shows a conventional stacked FF called the stacked FF [6]. In order to reduce the area overhead, the inverters in the master and slave latches is stacked. But the delay time

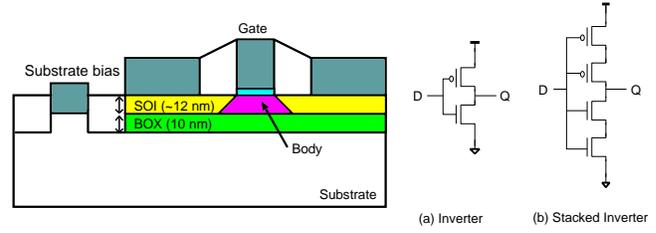


Fig. 1. Cross Section of SOTB (Silicon On Thin BOX).

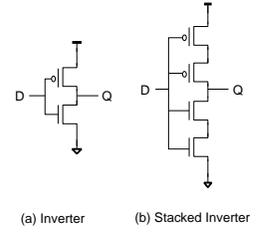


Fig. 2. Structure of the inverter and stacked-inverter.

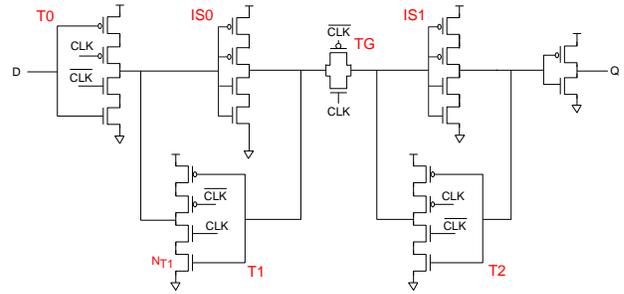


Fig. 3. Conventional stacked FF.

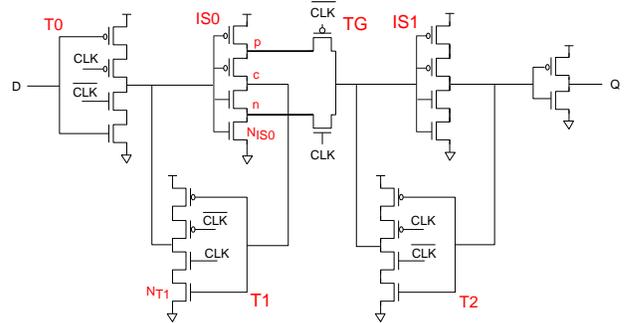


Fig. 4. SLCCFF (Stacked Leveling Critical Charge Flip-Flop).

of stacked-inverter is greater than standard inverters, its delay penalty is bigger than the standard DFF (D-type Flip Flop).

Fig. 4 shows the proposed SLCCFF (Stacked Leveling Critical Charge Flip-Flop). The difference between the SLCCFF and the stacked FF is the connection between the stacked inverter (IS0) and the transmission gate (TG). In the SLCCFF, PMOS and NMOS transistors in TG are connected to the intermediate nodes (p and n) instead of the output node (c) to shorten the delay.

B. Energy, Delay and Area Comparison

We optimize delay of the SLCCFF and the stacked FF by the downhill simplex method[7] by changing the transistor size to minimize ED (Energy Delay) product. Fig. 5 shows the rise delay and the energy by optimizing the downhill simplex method. In addition, Table I indicates the energy, delay and area when ED becomes minimum. The area of the SLCCFF is about 1.1x bigger than that of the stacked FF. However, the

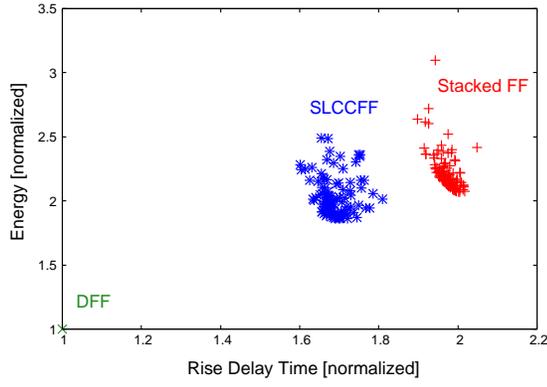


Fig. 5. Energy and delay optimized by the downhill simplex method (normalized by DFF values).

TABLE I
ENERGY, DELAY AND AREA COMPARISON

	Energy	Delay	Area
Stacked FF	2.13	2.00	1.12
SLCCFF	1.89	1.67	1.24

delay and the energy of the SLCCFF are about 16% and 11% smaller than those of the stacked FF, respectively.

III. Radiation Hardness Evaluation of Flip-Flops by Spallation Neutron and α -Particle Irradiation

This section shows the experimental method and measurement results.

A. Test chip

The error rates of the non-redundant FFs on the fabricated test chip are measured by spallation neutron and α -particle irradiation. We exposed two types of test chips; one is fabricated by the SOTB process and the other is fabricated by the bulk process. Note that these two types of chips have the exactly same layout pattern besides BOX layers. Fig. 6 shows the detailed structures of the test chip. The FFARRAY part of a test chip is 1.3 mm \times 5 mm and contains 390,816 FFs; 105,984bit of DFFs, 99,360bit of the stacked FFs and 185,472bit of the SLCCFFs. All FFs on the triple-well (3W) structure, and those are connected in series to form a shift register.

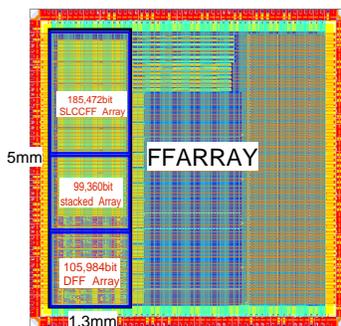


Fig. 6. Floor plan of test chip.

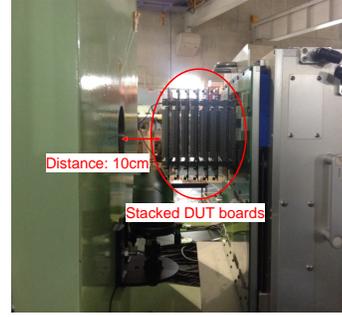


Fig. 7. Radiation test by the spallation neutron beam.

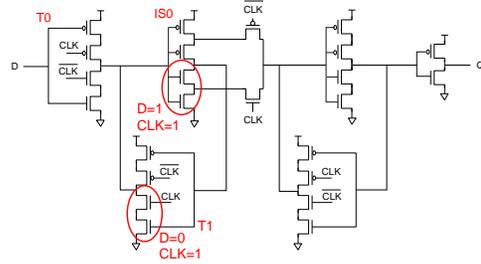


Fig. 8. The transistor which causes a soft error.

B. Measurement Results of Spallation Neutron Irradiation

Spallation neutron irradiation tests were carried out at Research Center for Nuclear Physics (RCNP). Fig. 7 shows the test setup. In order to increase the number of errors in the limited measurement time, stacking boards are used. One DUT (Device Under Test) board equips four test chips. We stacked six DUT boards. We measured these two conditions; (D, CLK)=(0, 1) and (1, 1) at which the master latch is in the latch state and the slave latch is in the transparent state. Fig. 8 shows the transistor which causes a soft error. If (D, CLK)=(0, 1), the NMOS transistor N_{T1} in the tristate inverter is vulnerable to particle hits. On the other hand, If (D, CLK)=(1, 1), the NMOS transistor N_{ISO} in the inverter is vulnerable. Note that we assume that NMOS transistors are much more vulnerable to particle hits than PMOS transistors[8].

Fig. 9 and 10 shows the neutron induced SERs (Soft Error Rates) in the bulk process when (D, CLK)=(0, 1) and (1, 1), respectively. By reducing the supply voltage from 1.2 V to 0.6 V, the SERs becomes almost tripled. The SERs of the stacked and the SLCCFF are almost same or smaller than the DFF in the bulk process. There is no distinct tendency when (D, CLK)=(0, 1), while the stacked FF and SLCCFF are 12% and 33% stronger than the DFF at 0.6 V when (D, CLK)=(1, 1).

Fig. 11 and 12 shows the measurement results in the SOTB process when (D, CLK)=(0, 1) and (1, 1), respectively. Compared with the results of the bulk process, SERs of the stacked FF and the SLCCFF is much smaller than the conventional DFF. Especially, when (D, CLK)=(1, 1), the SER of the SLCCFF is no larger than 3 FIT/Mbit in all supply voltages. It is almost 1/27 compared with that of the DFF at 0.4 V. Compared with the stacked FF, the SLCCFF exhibits lower or almost same SERs at any supply voltages and states. However, when (D, CLK)=(0, 1), the error tolerances of the stacked FF and the SLCCFF may not be sufficiently high.

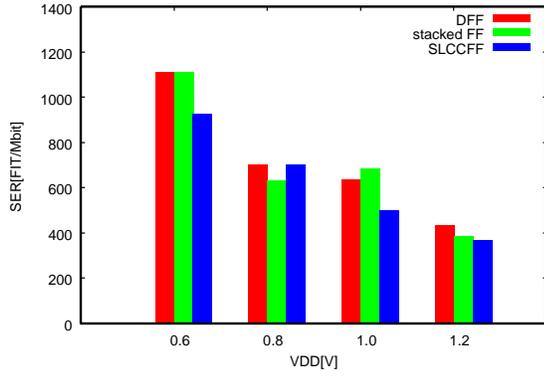


Fig. 9. Measurement results by neutron in bulk process (D, CLK)=(0, 1).

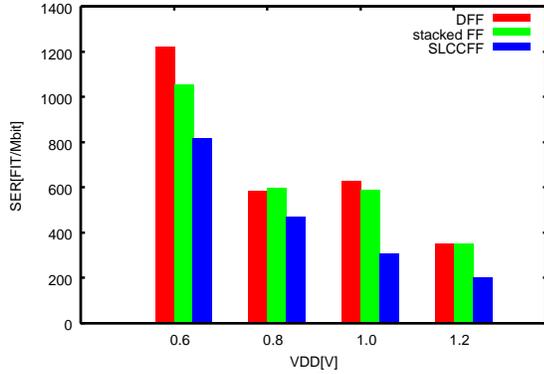


Fig. 10. Measurement results by neutron in bulk process (D, CLK)=(1, 1).

If the tristate inverters are stacked, they become more robust to soft errors with some amount of area, delay and power overhead.

C. α -Particle Irradiation Test

The error resilience of the FFs on the fabricated chip are measured by α -particles from 3M Bq ^{241}Am . Fig. 13 shows the test setup of α -particle irradiation test. The distance between the α source and the DUT is 0.7 mm. We measured these two conditions; (D, CLK)=(0, 1) and (1, 1) at which the master latch is in the latch state and the slave latch is in the transparent state.

Fig. 14 and 15 shows the measurement results by α -particle irradiation from 3M Bq ^{241}Am in the bulk process when (D, CLK)=(0, 1) and (1, 1), respectively. By reducing the supply voltage, the error probability becomes almost tripled, which is almost same tendency with the neutron irradiation. The error probabilities of the SLCCFF are smaller than the DFF and stacked FF by α -particle irradiation test in the bulk process.

Fig. 16 and 17 shows the measurement results in the SOTB process when (D, CLK)=(0, 1) and (1, 1), respectively. Regardless of the (D, CLK) state, error probabilities of the stacked FF and the SLCCFF are much smaller than the DFF. When (D, CLK)=(1, 1), the error probabilities of the SLCCFF are almost the same as that of the stacked FF at low supply voltage. Especially, the error probabilities of the stacked FF and the SLCCFF are less than 1/100 compared with the conventional DFF at 0.4 V. On the other hand, when (D, CLK)=(0, 1), the error probabilities of the SLCCFF are almost 1/10 and 1/100 compared with the the stacked FF and conventional DFF at 0.4 V, respectively. When (D, CLK)=(0, 1),

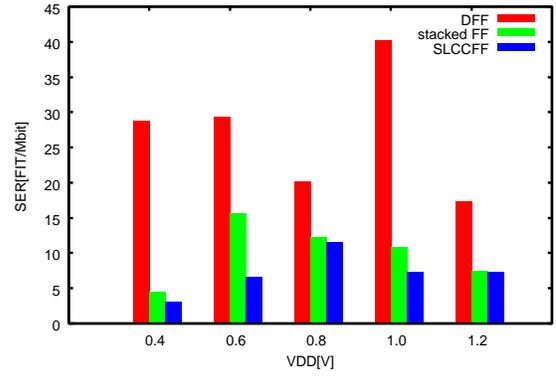


Fig. 11. Measurement results by neutron in SOTB process (D, CLK)=(0, 1).

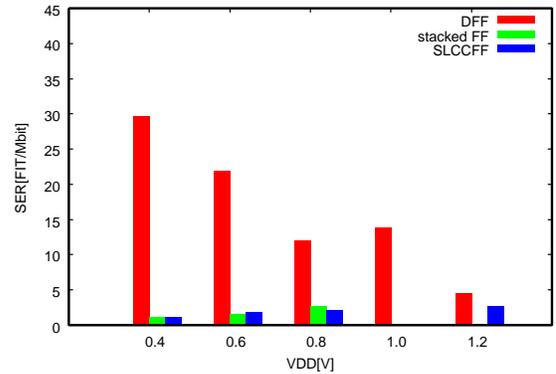


Fig. 12. Measurement results by neutron in SOTB process (D, CLK)=(1, 1).

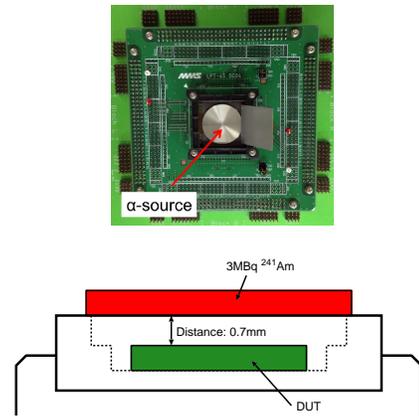


Fig. 13. Radiation test by α -particle irradiation.

it is conceivable that the NMOS transistor N_{T1} in the tristate inverter causes a soft error. However, the circuit structure of the tristate inverter is the same between the stacked FF and the SLCCFF. We compare the critical charge. If generated charge by a particle exceeds a critical charge, stored values in FFs are flipped. We evaluate a critical charge of the NMOS transistor N_{T1} . SPICE simulation results shows the critical charge of the stacked FF and SLCCFF are 1.4 fC and 1.0 fC, respectively. As a result, the cause of the difference in the soft error tolerance between stacked FF and SLCCFF when (D, CLK)=(0, 1) is not the NMOS transistor N_{T1} . Such a small difference of the critical charges does not cause the

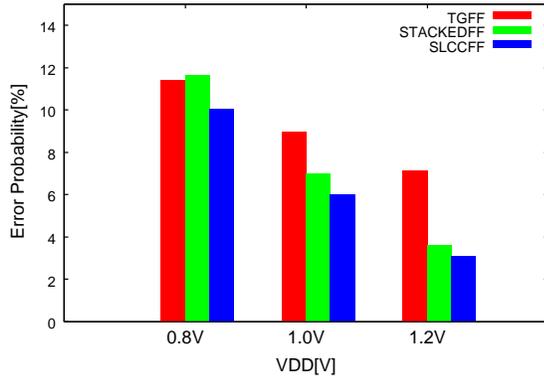


Fig. 14. Measurement results by α -particle in bulk process (D, CLK)=(0, 1).

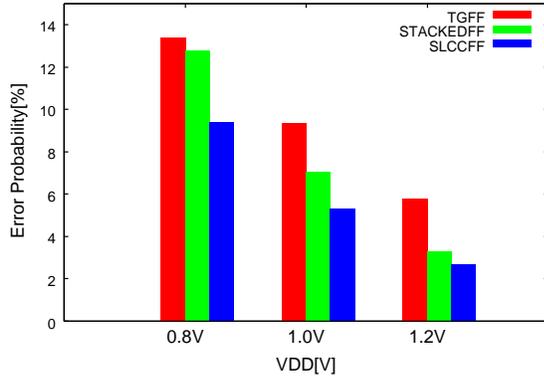


Fig. 15. Measurement results by α -particle in bulk process (D, CLK)=(1, 1).

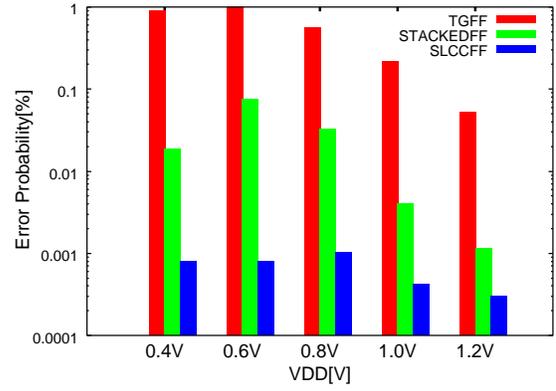


Fig. 16. Measurement results by α -particle in SOTB process (D, CLK)=(0, 1).

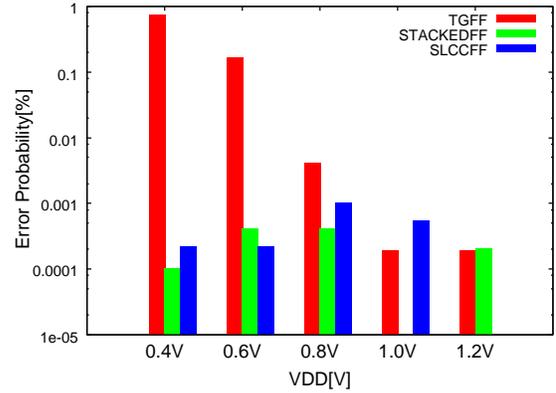


Fig. 17. Measurement results by α -particle in SOTB process (D, CLK)=(1, 1).

difference of the error probabilities of one order of magnitude in Fig. 16. It might be in the layout structure of FFs.

IV. Conclusion

The SOI process has lower soft error sensitivity than the conventional bulk process. Redundancy consumes large area and delay overhead to mitigate soft errors. By implementing radiation-hard circuits with the SOI process, no redundancy is required. We propose the SLCCFF (Stacked Leveling Critical Charge Flip-Flop) which is resilient to soft errors only in the FD-SOI process for lower energy consumption and smaller delay than the conventional stacked FF. The rise delay and the energy of the SLCCFF are about 16% and 11% smaller than those of the stacked FF, respectively. From the spallation neutron irradiation, the SER of the SLCCFF is 1/27 of the conventional DFF on the SOTB chip. The SER of the conventional DFF on the SOTB chip is 1/40 of that on the bulk chip. Thus, the SLCCFF on the SOTB chip is more than 1000x (three orders of magnitude) stronger than the conventional DFF on the bulk chip. In addition, from α -particle irradiation test, the error probability of the SLCCFF is less than 1/100 compared with conventional DFF in the SOTB process. By using an SOI process, SLCCFF are enough to decrease SERs by the three orders of magnitude.

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