Dependence of Cell Distance and Well-contact Density of MCU Rates by Device Simulations and Neutron Experiments in a 65-nm Bulk Process

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***Abstract*—Technology scaling increases the role of charge sharing and bipolar effects with respect to multiple cell upset. We analyze contributions of cell distance and well-contact density to suppress MCU by device-level simulations and neutron experiments. Device simulation results reveal that the ratio of MCU to SEU exponentially decreases when the distance between latches is increased. MCU is suppressed when well contacts are placed between redundant latches. Experimental results also show that the ratio of MCU to SEU exponentially decreases by increasing the distance between cells. MCU is suppressed effectively by increasing the density of well contacts.**

I. Introduction

Radiation induced charge collection at a single sensitive node, such as the drain region of a single transistor, is a possible source of SEU. Radiation-hardened circuits, for instance Triple Modular Redundancy (TMR), Built-in Soft Error Resilience (BISER)[1], Dual Interlocked Storage Cell (DICE)[2], and Error Correction Code (ECC) have been employed to mitigate an SEU. As process are scaled down, multiple node charge collection has an increasing impact on the response of the circuit[3]. Soft errors have become an increasingly troublesome issue for memories as well as sequential logic circuits.

Recently, the charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the charge sharing, also the bipolar effect become dominant when a particle hit on latches or flip-flops. It makes radiation-hardened circuit more sensitive to Multiple Cell Upsets (MCUs)[4]. MCU rate depends on cell distance and well-contact density. In order to reduce radiation-induced multiple errors, each vulnerable transistor is placed on different p-well regions or separated over 1.1μm[5], [6]. The parasitic bipolar effect and the charge sharing also affect SEU[7] and Single Event Transient (SET) pulse widths[8]. To estimate soft-error rates and increase its resilience, it is necessary to measure characteristics of radiation-induced multiple errors.

In this paper, we analyze the impact of cell distance and well-contact density on redundant flip-flops by device-level simulations[9] and neutron experiments[10]. All device-level models are constructed in a 65-nm process. Test chips are fabricated in a 65-nm bulk CMOS process and accelerated tests are carried out at Research Center for Nuclear Physics (RCNP). Section II shows the impact of cell distance and well-contact density on redundant latches in device-level by TCAD simulations. The same results by neutron experiments are shown in Section III. We compare the simulations and experimental results in Section IV. Section V concludes this paper.

II. Impact of Cell Distance and Well-contact Density in Device-level

A. Device-level Simulation Setup

A device simulator Sentaurus from Synopsys is used to do all device-level simulations. Fig. 1 shows a circuit including

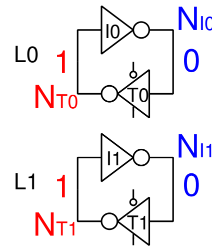


Fig. 1. Redundant latches.

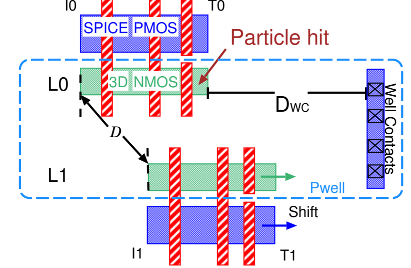


Fig. 2. layout of two latches in two rows.

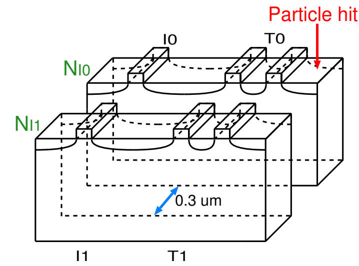


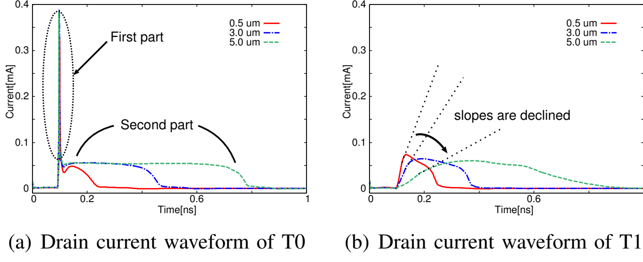
Fig. 3. 3D device-level structure of redundant latches in two rows. A particle hit at the tri-state inverter T0.

two latches placed in two adjacent rows in a 65-nm bulk technology. A radiation particle hits the NMOS transistor of the tri-state inverter T0 in the odd row. The layout structure of the redundant latches in two rows is shown in Fig. 2. All of the NMOS transistors are placed in the same P-well. Well contacts are placed side by side in the same well. The output nodes (N_{T0}, N_{T1}) of the tri-state inverters T0 and T1 are initially set to "1". Output voltage of the tri-satate inverter is decreased by charge collection and bipolar effects when a particle hits NMOS of the tri-state inverter. The redundant latches simultaneously flip by one particle hit. It is so as to analyze the MCU tolerance of redundant latches.

Based on the circuit and layout structures, we construct a 3D device-level NMOS model as shown in Fig. 3. This 3D NMOS model is constructed in a triple well structure. The distance between the well contacts and latches is defined as D_{WC}. D is the distance between redundant latches L0 and L1. D_{WC}. D is 0.3 μm when the redundant latches are aligned vertically as shown in Fig 3. A heavy-ion model that its length is 2 μm and the radius is 0.07 μm is used in all simulations. The ion hits T0 at 0.1 ns from the beginning of simulations.

B. Contribution of Cell Distance D to Suppress MCU

Fig. 4 shows the drain current of tri-state inverters T0 and T1 when the redundant latches start to flip simultaneously. D_{wc} is 20 μm. D is 0.5, 3.0 and 5.0 μm. The waveform of T0 can be divided to two parts as shown in Fig. 4(a). The first part is very steep, that can be modeled by a single or double exponential model, while the second part is shallow. From the simulation results, we can obviously recognize that there are



(a) Drain current waveform of T0 (b) Drain current waveform of T1

Fig. 4. Transient drain current caused by a particle hit at T0 when redundant latches simultaneously flip. D is 0.5, 3.0, 5.0 μm

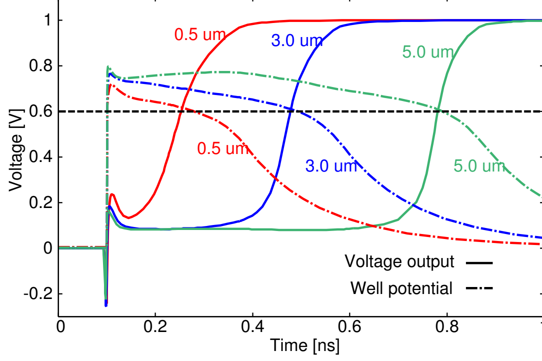


Fig. 5. Voltage outputs of I0 and the well potential of the latch L0 by a particle. D is 0.5, 3.0, 5.0 μm.

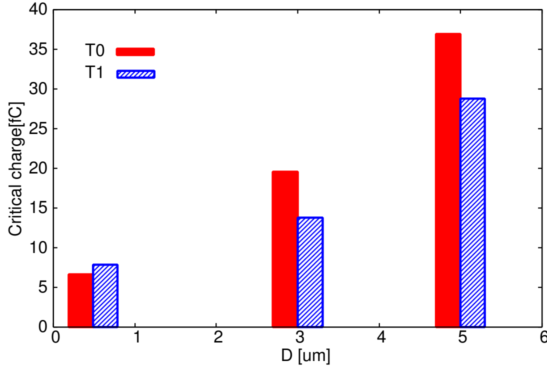


Fig. 6. Critical charge by ion particle hit on T0. D is 0.5, 3.0, 5.0 μm.

two mechanisms occur in the whole charge collection. After the particle hit, a large amount of electrons are collected in the drain region immediately. The first part appears a steep current by the drift. After that, holes still remain in the bulk region, which reduces the source-well potential barrier due to the increase in the potential of the p-well. The source injects electrons into the channel which can be collected at the drain. This effect is called the parasitic bipolar effect because the source-well-drain of NMOS transistor acts as an n-p-n bipolar transistor. The shallow current waveform in the latter part is caused by the parasitic bipolar effect.

As D is increased from 0.5 to 5.0 μm, the first parts do not change a lot while the shallow parts become wider as shown in Fig 4(a). More charge is collected into T0 by the bipolar effect according to D. Fig. 4(b) shows the current waveforms of T1. The slope of the current waveforms are declined by increasing D. The charge collection becomes slower by the distance D. Less charge is collected into T0 by drift after the particle hits T0. However, the waveforms become wider. More charge is collected into T1 by the bipolar effect. Charge sharing between the redundant latches become weaker while

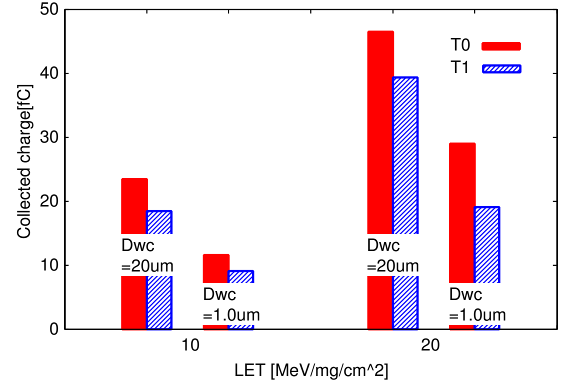


Fig. 7. Collected charge according to D_{WC}.

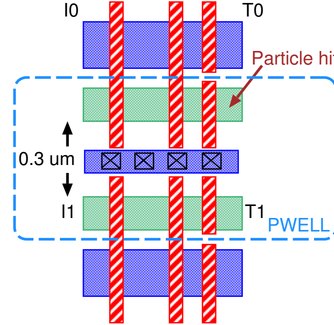


Fig. 8. Well contacts are placed between the redundant latches.

the charge is mainly collected into T1 by bipolar effects. Fig. 5 shows the voltage waveforms of I0 and the well potential by a particle hit on the tri-state inverter. D is 0.5, 3.0 and 5.0 μm. The voltage waveforms keep low when the well potential is higher than 0.6V. The voltage waveforms are start to flip when well potential decreases below 0.6V. We also find that the flipped voltage waveforms cross the well potential waveforms at 0.6V. The bipolar transistor can not turn off until the well potential decreases below 0.6V.

Fig. 6 shows the values of critical charge of tri-state inverters T0 and T1 when the redundant latches simultaneously flip. The critical charge becomes bigger when D is increased as shown in Fig. 6. As D is increased, charge sharing between T0 and T1 becomes weaker. Charge is mainly collected into T1 by the bipolar effect. However, it is hard to elevate the well potential under T1 because T1 is separated far away from T0 ($D \gg 0.3$ μm). Thus, the energy of the ion particle which simultaneously upsets the redundant latches becomes higher. More charge is collected into T0 and T1 by increasing D.

C. Contribution of Well-contact Position to Suppress MCUs

We place the well contacts adjacent to latches, D_{WC} is shorten to 1.0 μm from 20 μm. LET are 10 and 20 MeV/mg/cm^2. The redundant latches are aligned vertically (D = 0.3 μm) in these simulations. The volume of collected charge of T0 and T1 are shown in Fig. 7. When the distance D_{WC} is shorten from 20 μm to 1.0 μm, the volume of collected charge decreases by 50%. The well potential under latches keeps steady by placing well contacts close to latches. Bipolar effects under T0 and T1 are suppressed. Thus, less charge is collected to the redundant latches.

When the well contacts are placed between the redundant latches L0 and L1 as shown in Fig. 8, the volume of collected charge is shown in Fig. 9. the collected charge of T0 decreases

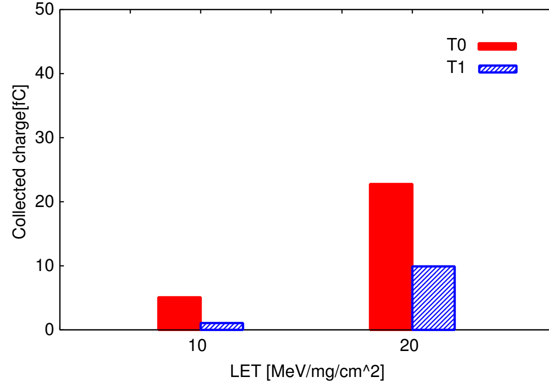


Fig. 9. Collected charge of the structure at which well contacts are placed between the redundant latches.

TABLE I
PARAMETERS FOR SER ESTIMATION

F ($cm^{-2}s^{-1}$)	5.65e-3
Q_s (fC)	5.72
K	2.2e-5

TABLE II
QCRIT AND MCU RATES BY DEVICE SIMULATIONS WHEN D_{WC} IS 20 μM.

D	Q_{crit}	MCU/SEU [%]
0.5	8.31	50.18
0.6	9.95	37.70
1.0	11.3	29.70
1.5	17.2	10.59
2.0	26.9	1.94
2.5	30.9	0.97
3.0	32.4	0.74
4.0	51.5	0.026
4.5	61.5	0.0046
5.0	75.4	0.0004
Fig. 8	45.7	0.073

the same volume as the collected charge when D_{WC} is 1.0 μm. Even though the redundant latches are aligned vertically, the volume of collected charge of T1 decreases by 90% compared to the collected charge when D_{WC} is 20 μm. In this case, generated charge under the latch T0 can not cross over the well contacts to the T1 side. Thus the charge sharing between the redundant latches is almost prevented. Also the bipolar effects are suppressed effectively, because the well contacts between the redundant latches suppress the well potential elevation. The redundant latches simultaneously flip when LET is increased to 35 MeV/mg/cm^2, and the critical charge is 45.7 fC.

D. Soft Error Rate Calculation

Eq. (1) [11] is used to calculate SER in FIT (Failure In Time, number of errors/10^9 hours).

$$N_{SER}(Q_{crit}) \quad = \quad F \times A \times K \times \exp\left(-\frac{Q_{crit}}{Q_s}\right) \qquad (1)$$

where F is the high-energy neutron flux and A is the drain area of transistors related to soft errors. K is a fitting parameter. Q_s is called "charge collection efficiency" that strongly depends on doping and supply voltage[12]. We use the parameter values as in Table I that are scaled from 100 nm[11] to 65-nm.

MCU rates are calculated by the critical (minimum) charge at which the redundant latches are simultaneous flipped. D_{WC} is the distance between the redundant latches and well contacts as in Fig. 2. The Q_{crit} and the ratios of MCU to SEU are shown in Table II when D_{WC} is 20 μm. Fig. 10 shows the distance-dependence of MCU / SEU on redundant latches. Not that the ratios of MCU to SEU which lower than 0.1% are not shown on Fig. 10. The ratio exponentially decreases by increasing D. The ratio of MCU to SEU decreases to 0.073% when the well contacts are placed between redundant latches.

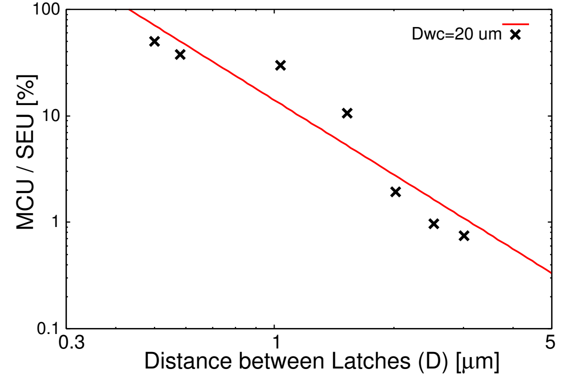


Fig. 10. MCU/SEU rates by D. D_{WC}=20 μm.

III. Impact of Cell Distance and Well-contact Density on redundant FFs by Neutron Experiments

The experimental results of neutron-induced MCUs on D-FFs are described in this section. We use four different shift registers to estimate soft error rates on redundant flip-flops[10]. The dependence of MCUs on the distance of FFs and well-contact density is also shown in this section.

A. Test Chips

We fabricated a test chip in 65-nm bulk CMOS process to measure soft error rates by spallation neutron beam. These test chips are used to reveal the follows.

- MCU rates are decreased by increasing the cell-distance of redundant FFs.
- MCU rates are decreased by high well-contact density (closed well-contact distance).

To estimate soft error rate on redundant FFs, we implement four different shift registers as shown in Fig. 11. All shift registers are constructed by FFs and clock buffer chain [13]. These FFs are constructed in the same layout structure except for well contacts. Fig. 12 shows the schematic diagram. The

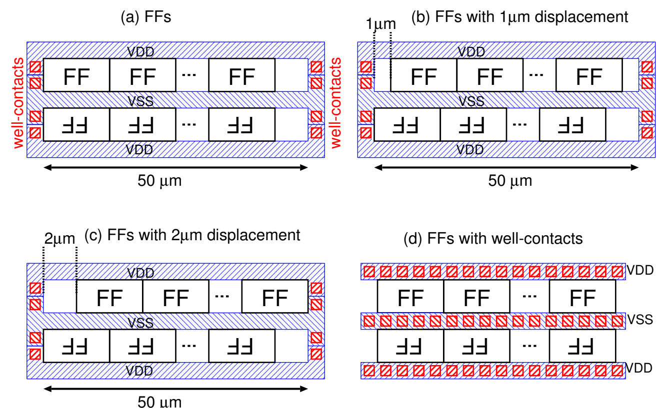


Fig. 11. Conceptual layout structures of four different shift registers. Clock buffer chains are omitted in this figure.

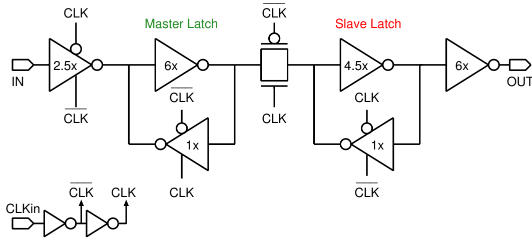


Fig. 12. Schematic diagram of implemented FFs. The values of this figure show normalizing drive strengths.

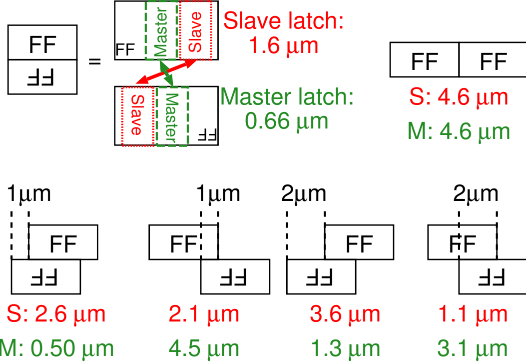


Fig. 13. Distance between master or salve latches on shift register (a) – (c) in Fig. 11.

master and slave latches are constructed by inverters and tri-state inverters.

The distance between odd rows and even rows in registers (a) – (c) are 0 μm, 1 μm, and 2 μm as shown in Fig. 11. We use these shift registers to estimate the cell-distance independence MCU rates. In addition, shift registers have different distance between slave latches and between master latches as shown in the upper left of Fig. 13.

The well-contacts of shift registers (a) – (c) are inserted every 50 μm. The shift register of Fig. 11 (d) has well-contact arrays under its power and ground rails, which has 60x higher well-contact density than the others. Therefore, we obtain dependence of MCU rates on well-contact density by comparing MCU rates between the shift registers (a) and (d) which have the same cell distance.

B. Experimental Setup

Fig. 14 shows a test chip micrograph fabricated in a 65-nm bulk CMOS process. Each shift register includes 10k FFs. The total area of four shift registers is 0.5 $\times$ 0.8 mm^2 on a 2 $\times$ 4 mm^2 die.

Experiments were carried out by spallation neutron irradiation at RCNP. Fig. 15 shows the neutron beam spectrum compared with the terrestrial neutron spectrum of Tokyo at the ground level. The average acceleration factor is 3.8×10^8. In order to increase error counts, we measured 28 chips at the same time using stacked DUT boards. An engineering LSI tester is used to control DUTs and collect shifted error data.

C. Experimental Results

Table III shows the number of SEU and MCU of each shift register as shown in Fig. 11 by the spallation neutron beam. The ratio of MCU to SEU is up to 23.4% which is close to that on 65-nm SRAM cells[4]. These results clearly show that the shift register (d) has a very low MCU rate and only one MCU is observed on it. The number of MCU is reduced from 110 to 1 by inserting well-contact arrays under supply

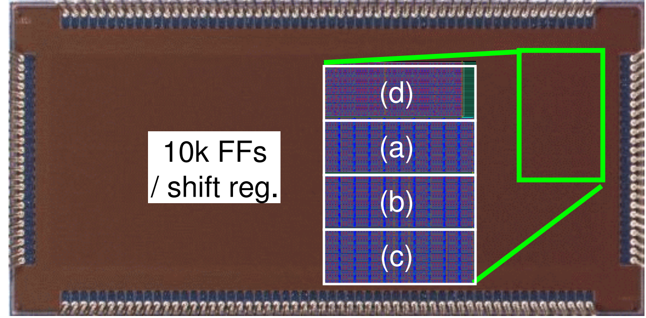


Fig. 14. Chip micrograph with floorplan.

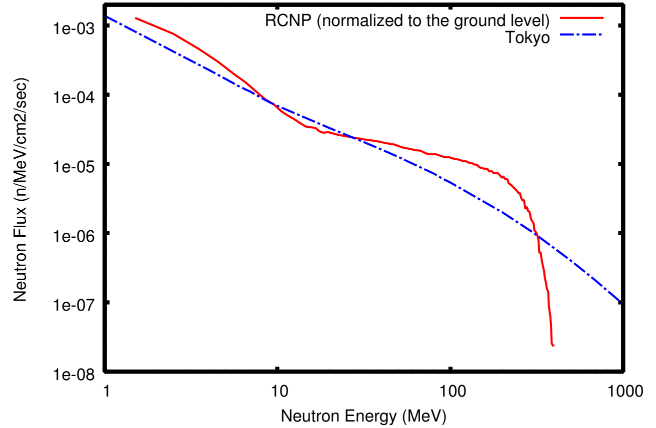


Fig. 15. Neutron spectrum at RCNP.

and ground rails of FFs. Therefore, we can improve soft-error resilience of the redundant FFs by increasing well-contacts between redundant latches. It also shows that in the fabricated technology, almost all MCU is caused by the parasitic bipolar effect since it is caused by well-potential perturbation[14].

IV. Comparison of Device-level Simulations Results and Experimental Results

Fig. 16 shows the distance-dependence of MCU / SEU on FFs which is obtained from the shift registers (a)-(c). The MCU / SEU (y-axis) is obtained from measurement results. The ration of MCU to SEU exponentially decreases influenced by $D^{-1.67}$ (D is the distance between two latches) and fitting line shows that it is almost 100% when $D < 0.3$ μm. As shown in Fig. 12, master and slave latches in the FF have different structures. However, experimental results of MCU / SEU are distributed along the same straight line. Therefore, the ratio of MCU to SEU does not depend on the drive strength and load capacitance.

The ratio of MCU to SEU influenced by D by device simulations is also shown in Fig. 16. FFs are placed every 5 μm on the measured chips. Thus, we calculate the MCU / SEU by device simulations by altering D_{WC} in increments of 5 μm

TABLE III
THE NUMBER OF SEUS AND MCUS BY NEUTRON IRRADIATIONS.

Shift Register	Min. cell distance	# of SEU	# of MCU	MCU/SEU [%]
(a) FFs	0.66 μm	617	110	17.8
(b) FFs w/ 1 μm	0.5 μm	631	148	23.4
(c) FFs w/ 2 μm	1.3 μm	654	91	13.9
(d) FFs w/ well-contacts	0.66 μm	498	1	0.2

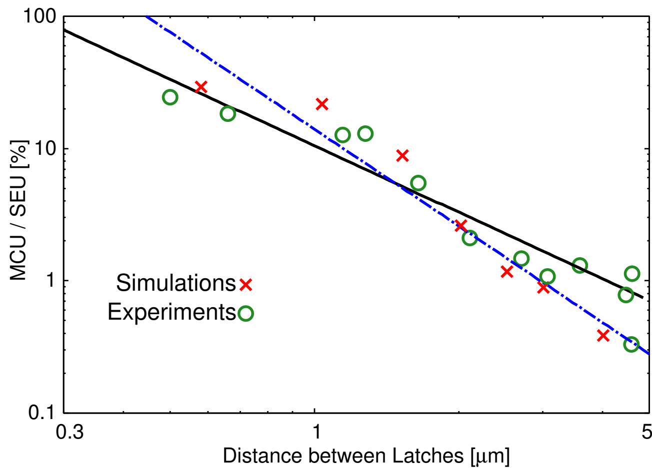


Fig. 16. Distance-dependence of the ratio of MCU to SEU by device simulations and neutron experiments.

from 5 to 25 μm. The average values are shown in Fig. 16. It is obviously shown that the ratio of MCU to SEU by device simulations exponentially decreases when the cell distance D is increased. The fitting line by simulations exponentially decreases influenced by $D^{-2.23}$, which almost coincides with the experimental results. According to the results of experiments and simulations. In order to achieve 100x higher soft-error tolerance in redundant FFs than in non-redundant FF, we must implement redundant FFs whose latches are separated by 4 μm from each other. It consumes huge area or complicated design procedures and these drawbacks become dominant by the process scaling.

Only one MCU is observed when the well contacts are placed between redundant flip-flops by neutron experiments, and the ratio of MCU to SEU decreases to 0.073% by device simulations. Thus, MCU is suppressed when well-contact array under the supply and ground rail. However, the well potential is fixed in this layout structure. This kind of structure can not be used if the well potential is changed to mitigate variations or to control performance and leakage.

V. **Conclusion**

Based on the result of device simulations, we show that charge sharing and bipolar effect are two main factors when MCU occur in redundant latches. MCU is suppressed when the distance between the redundant latches (D) is increased. Total charge collected by L0 and L1 decreases by 50% to placed the well contacts adjacent (D_{WC} is 1.0 μm) to the latches. Total collected charge of T1 reduces by 90% when the well contacts are placed between redundant latches. The ratio of MCU to SEU decreases to 0.073%.

According to the results of neutron experiments and device simulations, the ratio of MCU to SEU exponentially decreases by increasing the distance of latches D. The fitting lines are influenced by $D^{-1.67}$ and $D^{-2.23}$ by experiments and simulations respectively. Experimental results also show that MCU rates can drastically be reduced by inserting well-contact arrays under supply and ground rails. The number of MCU is reduced to one. The result of device simulations coincides with the neutron experiments.

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