A Low-Power and Area-Efficient Radiation-Hard Redundant Flip-Flop, DICE ACFF, in a 65 nm Thin-BOX FD-SOI

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***Abstract*—In this paper, we propose a low-power area-efficient redundant flip-flops for soft errors, called DICE-ACFF. Its structure is based on the reliable DICE (Dual Interlocked storage CEll) and the low-power ACFF (Adaptive-Coupling Flip-Flop). It achieves lower power at lower data-activity. We designed DICE-FF and DICE-ACFF using 65 nm conventional bulk and thin-BOX FD-SOI (Silicon on Thin-BOX, SOTB) processes. Its area is twice as large as the conventional DFF. As for power dissipation, DICE ACFF achieves lower power than the conventional DFF below 20% data activity. When data activity is 0%, its power is half of the DFF. As for soft error rates DICE ACFFs are 1.5x stronger than conventional DICE FFs by circuit-level simulations to estimate critical charge. No SEU is observed on the DICE ACFF by alpha-particle irradiation at 1.2V on the bulk and and SOTB chips. The soft error rates of the DFF of the SOTB chip is 1/200 compared with that of the bulk chip.**

I. Introduction

Process scaling makes LSI less reliable to soft errors. High performance computers (HPCs) are struggling with the power wall. Power consumption eliminates performance of HPCs. They are also very sensitive to soft errors since over several thousands of CPUs have to keep on running without error for a few days. Soft errors are caused by a particle hit. Neutrons are coming from cosmic ray and alpha particles are from radioactive impurities embedded in packages, bonding wires and so on. Memory cells or latches are flipped if some amount of charge is generated due to particle hits. To reduce soft error rates, various redundant flip-flop (FF) structures are proposed, for example, TMR (Triple Modular Redundancy)[1] and DICE (Dual Interlocked storage CEll)[2]. They employ various radiation-hard techniques, but large area and power overhead are required. In this paper, We propose a low-power area-efficient redundant flop-flops for soft errors, called DICE ACFF.

This paper is organized as follows. Section II explains the structure of the proposed DICE ACFF in detail. Section III gives the fabricated test chip to measure power and soft error rates of several non-redundant and redundant FFs. We explain how to evaluate soft error rates by charge sharing from circuit-level simulations in Section IV. Section V describes simulation and mesurement results. Finally we conclude this paper in Section VI.

II. DICE-ACFF

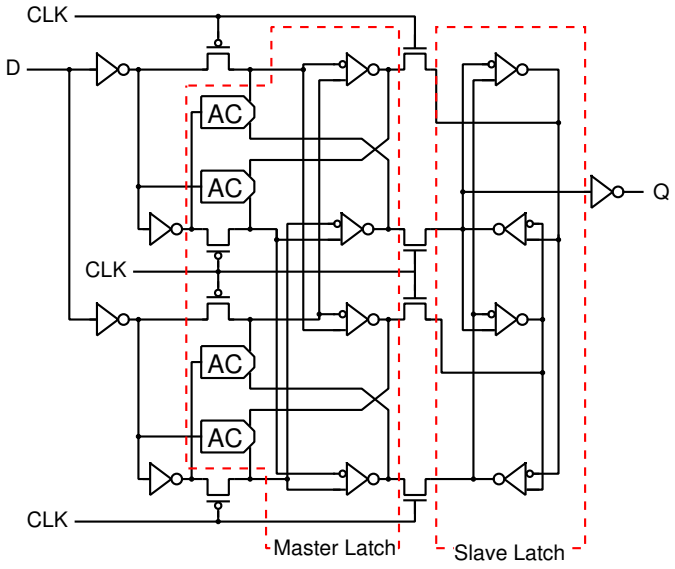
Fig. 1 (a) shows the proposed low-power area-efficient redundant radiation-hard FF, called DICE-ACFF. Its structure is based on the reliable DICE FF(Fig. 1(b)) and the low-power ACFF (Fig. 2).

The DICE structure mitigates soft errors by duplicating latches implemented by the half C-element and the clocked half C-element as shown in Fig. 1 (c). The input and output signals of these half C-elements have cross-coupled connections to be automatically recovered from a flip on a single node. On the other hand, redundant FFs such as TMR, BISER[3] and BCDMR[4] mitigates soft errors by majority voting among three storage cells, in which a flipped node is left until the next clock signal is injected to supply an unflipped new value. Compared with these majority-voter-based structures, the DICE structure is area-efficient since latches are not triplicated but duplicated.

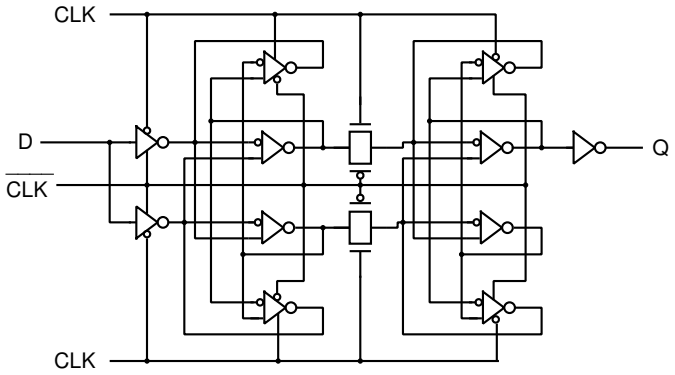
ACFF connects inverters for input, master and slave latches by PMOS or NMOS pass transistors. Conventional FFs based on transmission gates (called TGFF hereafter) use two phases of clock signals CLK and $\overline{\mathsf{CLK}}$. ACFFs, however, is operated by a single phase clock signal, which eliminates local clock buffers dissipating useless power when the activity of the input signal (the data activity, α) is low. In the conventional FFs, power dissipation of clock buffers are dominant if α is low. The AC elements as shown in the right side of Fig. 1 (c) is required to overwrite the master latch by PMOS pass transistors. They weaken the connection between the cross coupled inverters when the input of either inverter becomes 1 and the overwritten value is 0.

The proposed DICE ACFF are implemented by combining these two structures, DICE and ACFF. In the master and slave latches, inverters in the ACFF structure are replaced by half C-elements in the DICE structure. The half C-elements are duplicated and they are cross-coupled in the same manner as the original DICE.

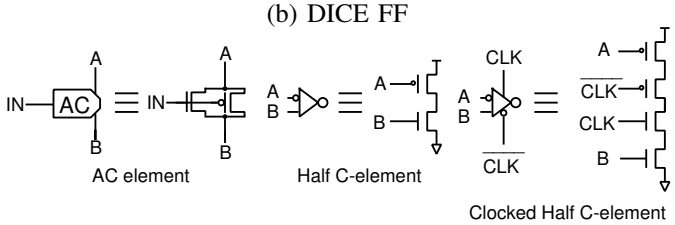
BCDMR ACFF[5] is another redundant FF based on BCDMR and ACFF as shown in Fig. 3. There is no local clock buffer because of its ACFF-based structure, which makes it lower-power at lower data activity. It is one of triplicated redundant FFs by voting two redundant latches and one keeper in the master or slave latch. Due to the triplicated structure, its area overhead is bigger than the DICE ACFF. If one of redundant latches is flipped, the keeper keeps the correct value since the C-element becomes high impedance. Even if the keeper is flipped, the C-element can overwrite the flipped value.



(a) DICE ACFF



(b) DICE FF



(c) AC, half-C and clocked half-C elements.

Fig. 1. Schematic diagram of DICE ACFF (a), DICE FF (b) and the detailed schematics of AC, half-C and clocked half-C elements (c).

III. FF Array Chip in a 65 nm Thin-BOX FD-SOI Process

The DICE ACFF is implemented using the double-height structure (DHC)[6] by sharing PMOS (N-well) regions (Fig. 4), which is much stronger to soft errors than sharing NMOS regions[7]. It is partly because major carriers of NMOS are electrons whose mobility is much faster than holes. NMOS regions are much more sensitive than PMOS regions.

We have implemented a chip including the DICE FF and DICE-ACFF arrays with other non-redundant and redundant FFs in a 65nm thin BOX (Buried OXide) FD-SOI (Fully-Depleted Silicon On Insulator) process called SOTB (Silicon on Thin BOX)[8]. Fig. 5 compares SOTB (a) and the conventional bulk (b) cross sections. SOTB guarantees low-voltage operations by undoped transistor channels to reduce variations of transistor characteristics due to dopant fluctuations. In addition to that, the back-gate bias voltage can be controlled through the thin BOX layer. It can be forward ($V_{\rm bs} > 0$ on NMOS) when high-performance operations are expected, while it can be reversed (backward) on sleep or low-power operations.

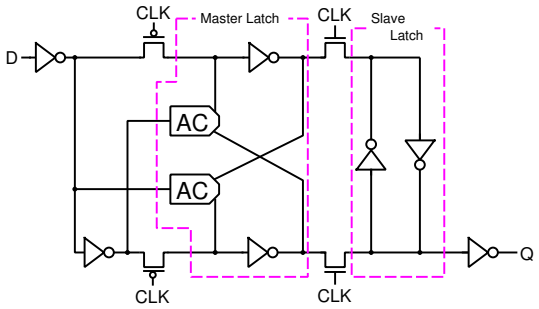


Fig. 2. Schematic diagram of ACFF.

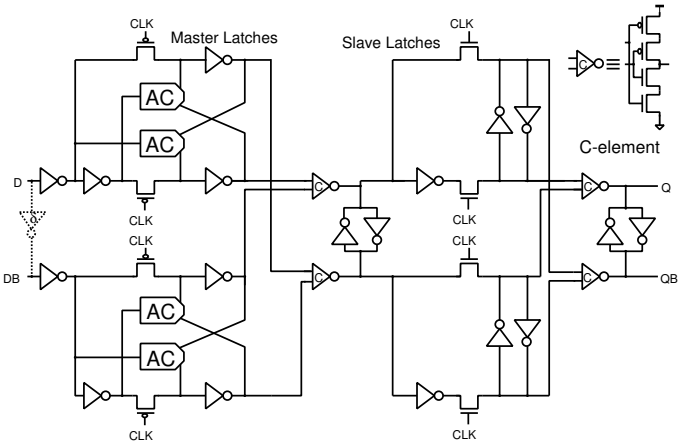


Fig. 3. Schematic diagram of BCDMR ACFF[5]

Two types of chips are fabricated by the SOTB and bulk processes. Note that these two are fabricated by the exactly same layout patterns besides thin BOX layers on SOTB.

Fig. 6 shows the chip micrograph with a block diagram and cell layout patterns. We have implemented seven FF arrays each of which including ACFFs, TGFFs (Transmission Gate FF), DICE FFs, DICE ACFFs, BCDMR FFs, BCDMR ACFFs and TMR FFs. TGFF is a conventional DFFs using transmission and tristate gate. Non-redundant FFs such as ACFFs and TGFFs are implemented in a single row, while

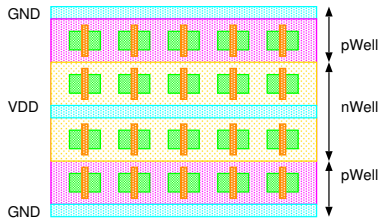


Fig. 4. Double Height Cell (DHC) structure

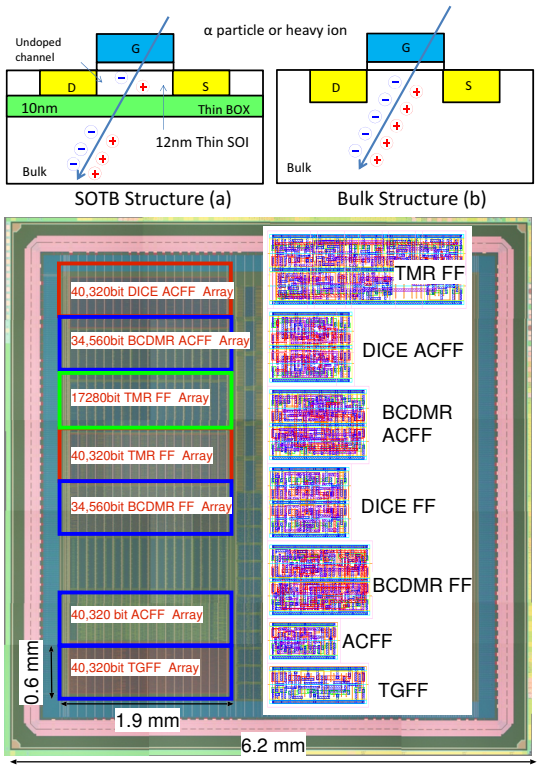


Fig. 6. Chip layout with block diagrams and cell layout patterns.

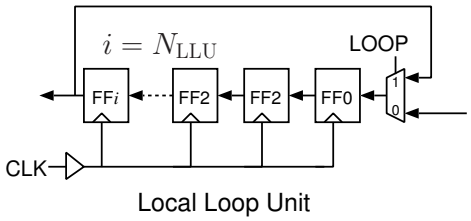


Fig. 7. Local loop to trap flipped values inside the loop while applying clock.

the other five redundant ones are implemented in two rows as the double height cells.

The area of DICE ACFF is almost twice larger than TGFF but only 1.05x bigger than the conventional DICE FF. The detailed comparison of the cell areas are described later in Section V-B.

When initializing data in all FF arrays on measurements, all FFs are connected in series as shift registers. On measurements by α particles or neutron irradiation, several FFs are connected in a loop to trap flipped values in the FF array while applying clocks[4] as shown in Fig. 7. Table I lists the total number of FFs in each array and the number of FFs in a local loop unit (N_{LLU}). Note that N_{LLU} is different with each array due to the cell layout widths. Wider FFs have smaller N_{LLU} to align the width of LLUs of all FFs.

IV. Estimation of Soft Error Rates

Stored values in FFs are flipped if generated charge by a particle hit exceeds a certain threshold value, which is called $\mathrm{Q_{crit}}$. In redundant FFs such as DICE, two nodes must be flipped simultaneously. However, the possibility is too low when two continuous or simultaneous hits on two redundant

TABLE I
Number of FFs in an LLU (N_{LLU}) and the total number of FFs in each array.

FF	N_{LLU}	Total number of FFs
DICE ACFF	14	40,320 ($18 \times 160 \times 14$)
BCDMR ACFF	12	34,560 ($18 \times 160 \times 12$)
TMR FF	6	17,280 ($18 \times 160 \times 6$)
DICE FF	14	40,320 ($18 \times 160 \times 14$)
BCDMR FF	12	34,560 ($18 \times 160 \times 12$)
ACFF	14	40,320 ($18 \times 160 \times 14$)
TGFF	12	40,320 ($18 \times 160 \times 14$)

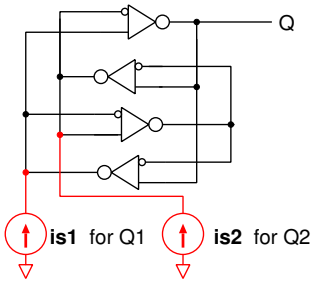


Fig. 8. Two single exponential current sources (is1 and is2) attached to two nodes of the latch.

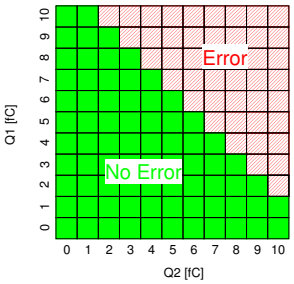


Fig. 9. Error map for DICE structure

nodes. We assume that a single particle hit flip multiple redundant nodes and generated charge from a single particle is shared by these redundant nodes. As shown in Fig. 4, the implemented DICE ACFF shares a PMOS region. There is no redundant node simultaneously flipped among NMOS transistors since they are separated by the PMOS region. We only evaluate Multiple Cell Upsets (MCUs) in the PMOS region. Eq. (1) is an empirical equation to compute soft error rates (SERs) by terrestrial neutrons[9], [10], [11]

$$N_{SER}(Q_{\mathrm{crit}}) = F \times K \times A \times \exp(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}) \quad (1)$$

in which, F is a neutron flux on the terrestrial region (0.00565 /cm^{2}s), K is a constant value of 2.2×10^{-5}, and A is the total drain area connected to the node. $\mathrm{Q_s}$ is a value that can be determined by process parameters. From 65 nm neutron irradiation results, $\mathrm{Q_s}$ in NMOS is 6.92 fC and that in PMOS is 3.40 fC.

In order to compute MCUs by a single particle hit, we use charge collection ratio according to the distance from the particle hit point. From the heavy ion results in [12], charge collection efficiency (E) is exponentially reduced by the distance x between the drain and the particle hit point expressed by the following equations.

$$E_{\mathrm{n}}(x) = 0.285\exp(-1.12x) \quad : \text{for NMOS} \quad (2)$$

$$(3)$$

In non-redundant FFs such as TGFFs, a single-exponential current source is enough to evaluate $\mathrm{Q_{crit}}$. In the triplicated structure, two successive simulations with one single-exponential current source are enough to compute Q_{crit} since two storage elements such as latches or keepers does not influence with each other. In the DICE structure, however,

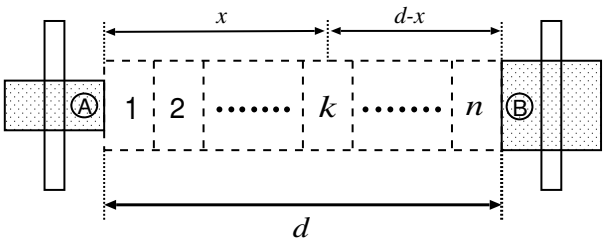


Fig. 10. Compute MCU rates of the critical pair transistors A and B

two single-exponential current sources must be attached on the circuit-level simulations as shown in Fig. 8 since two redundant storage elements are cross-coupled. Two independent current sources Q1 and Q2 are attached to the pair of two nodes that can flip the stored value, which is called a critical pair. By changing the amount of charge on Q1 and Q2, a Shmoo-like error map is depicted in Fig. 9.

Fig. 10 shows how to compute MCU rates from the critical charge of two transistors in a critical pair. From Eq. (2), we can compute $Q'_{\mathrm{critA}}(x)$ and $Q'_{\mathrm{critB}}(d-x)$. The maximum value $Q_{\mathrm{mcrit}}(k)$ between these two Q'_{crit} values can be considered as the critical charge in the region k.

By assigning $Q_{\mathrm{mcrit}}(k)$ to Q_{crit} and the area of the region k to A in Eq. (1), $N_{\mathrm{SER}}(k)$ is computed in the region k. By summing these values from all the region, we can obtain the total SER N_{TSER} of the critical pair as follows.

$$N_{\mathrm{TSER}} = \sum_{k=1}^{n} N_{\mathrm{SER}}(k) \quad (4)$$

V. Simulation and Measurement Results

We compare the proposed DICE ACFF in terms of soft-error resilience, power, area, delay and ADPP (Area, Delay and Power Product) with TGFF, ACFF, DICE FF, BCDMR FF, BCDMR ACFF and TMR FF.

A. Power Dissipations by Data Acitivity

We evaluate power dissipation by circuit-level simulations and measurements. In the circuit-level simulations, we bundle 8 FFs with a clock buffer as shown in Fig. 11. It is because FFs based on the ACFF dissipates less power due to its clock-buffer-less structure. Fig. 12 show power dissipation according to the data activity α from circuit-level simulations.

The power dissipation of DICE ACFFs becomes lower than TGFFs when α is below 20%. In general ASICs, the activity ratio α is from 5% to 15%[13]. The proposed DICE ACFF always operates at lower power under the condition. The power dissipations at α=10% is 77% of TGFF.

Fig. 13 shows power dissipation from measurements. The y axis is the power dissipation per each FF in the arbitrary unit. The bulk and SOTB chips are fabricated from exactly the same layout pattern besides the BOX layer, but the threshold voltages (V_{TH}) of transistors are different. The SOTB transistors have lower V_{TH} than the bulk transistors. To equalize the performance at VDD=1.2 V, the reverse body bias of -2.1 V is applied to both NMOS and PMOS of the SOTB chip. The power dissipation of the SOTB chip at the -2.1 V reverse

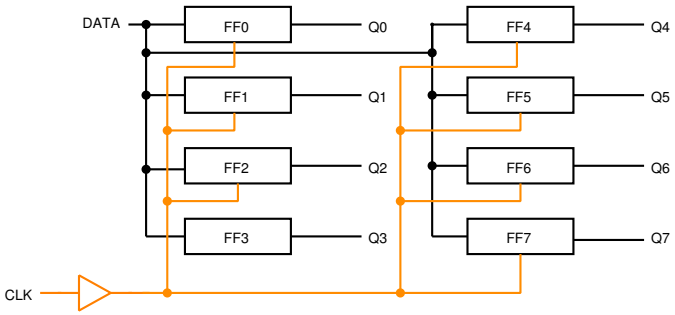


Fig. 11. Simulated circuit structure to compute power dissipation

body bias is 69% of the bulk chip. The reason why the SOTB power is lower than bulk is mainly due to the lower junction capacitance of the SOTB transistors.

Table II lists area, power at α=10% and delay. Note that the definition of the delay is CLK to Q estimated from circuit-level simulations with extracted stray capacitance. In the slave latches of ACFF, DICE ACFF and BCDMR ACFF, there is one inverter for output from clock-controlled pass transistors between master and slave latches, while there are two series inverters in the slave latches of TGFF and DICE FF. Thus the CLK-to-Q delay becomes longer in TGFF and DICE FF. In BCDMR ACFF, the C-element and the keeper make delays longer. Delays of those FFs become longer as the following order.

$$\begin{aligned} D_{\mathrm{ACFF}} &< D_{\mathrm{DICE\ ACFF}} < D_{\mathrm{TGFF}} \\ &< D_{\mathrm{BCDMR\ ACFF}} < D_{\mathrm{DICE\ FF}} < D_{\mathrm{TMR\ FF}} \end{aligned}$$

B. Area, Delay and Power Product

Table III shows the ADP products (ADPP). Delay and power values are obtained from circuit-level simulations. At $\alpha = 0\%$, the ADPPs of DICE ACFF and TGFF are equivalent. As α increases, the ADPP of DICE ACFF increases compared with that of TGFF. But the ADPP at α=10% is still only 39% bigger than that of TGFF. The proposed DICE ACFF is efficient in terms of area, power and delay.

C. Soft Error Rates from Simulations

Table IV lists SERs in FIT (Failure in Time)/Mbit from circuit-level simulations at V_{DD}=1.2V as explained in Section IV. It shows the highest SERs obtained from all possible stored values and clock states. As shown in the table, TGFF and ACFF have several hundreds FIT/Mbit due to their non-redundant structures. The proposed DICE ACFF has the 1.5x lower SER than DICE FF which relationship is equivalent to that between ACFF and TGFF. DICE ACFF has lower SER than DICE FF mainly because the lower critical charge and the longer distance between the nodes in the critical pairs.

BCDMR ACFF has approximately 5x lower SER than DICE ACFF. It is mainly because of its area penalty. As the distances between critical pairs become shorter, the values of Q_{crit} also becomes smaller according to Eq. (2). The main purpose of the DICE ACFF is to achieve lower power and lower area penalty. As in Table II, BCDMR ACFF is 14.3% bigger than

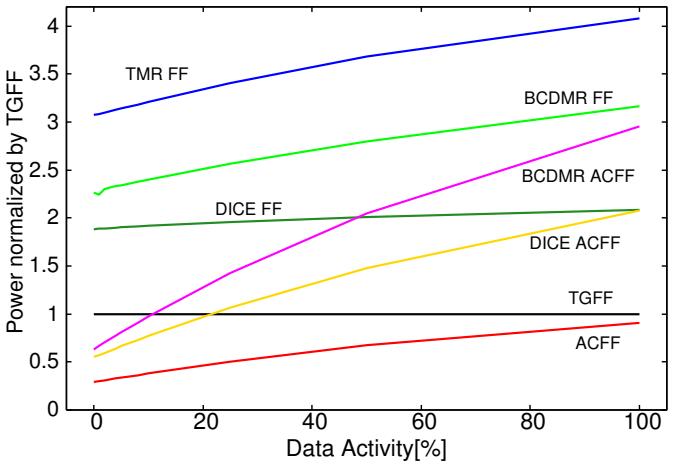


Fig. 12. Simulated power dissipations normalized by the power of TGFF

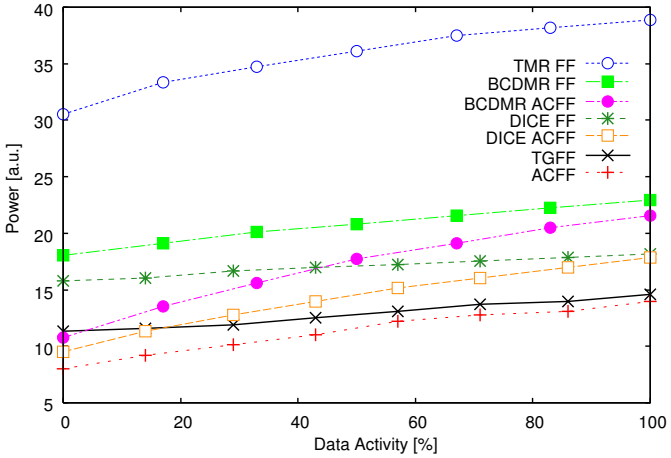


Fig. 13. Measured power dissipations of the SOTB chip.

DICE ACFF. The ADPP of DICE ACFF is always lower than that of BCDMR ACFF at any data activities α. It means that DICE ACFF achieves lower power, shorter delays and smaller area at the expense of the 5x higher SER than BCDMR ACFF.

D. Soft Error Rates from Measurement Results

We measure soft error rates by an α particle source (3 MBq ^{241}Am), which is mounted on the top of the DUTs. The distance between the die and the α particle source is approximately 0.7 mm. Tables V and VI show number of errors from 300 sec. α particle irradiation without applying any clock during irradiation. The error rates of TGFF is higher than that of ACFF, which is consistent with the simulations results in Table IV. All the implemented FFs are positive-edge triggered. Thus the master latches are in the hold state when CLK=1, while the slave latches are in the hold state when CLK=0.

In the DICE structure, a flipped node by an α hit automatically goes back to its original state soon after. The multiple hit on a DICE FF does not cause any error. Thus we observe no errors on DICE FFs and DICE ACFFs.

If multiple α hits two latches on a TMR FF flips, its output is flipped since we apply no clock during irradiation. The error rates of TMR FFs are higher due to the higher error rates on

TABLE II
AREA, POWER AND DELAY VALUES AT α=10% OF FFS NORMALIZED BY TGFFS. (POWER AND DELAYS FROM CIRCUIT-LEVEL SIMULATIONS.)

FF	Area	Power	average delay	rise delay	fall delay
TGFF	1.00	1.00	1.00	1.00	1.00
ACFF	0.76	0.456	0.49	0.43	0.55
DICE FF	2.00	2.28	1.29	1.43	1.18
DICE ACFF	2.10	0.716	0.86	0.73	0.97
BCDMR FF	2.50	2.403	1.75	1.51	2.03
BCDMR ACFF	2.40	0.911	1.15	1.21	1.11
TMR FF	5.20	3.21	1.52	1.55	1.52

TABLE III
AREA × DELAY × POWER OF FFS NORMALIZED BY CONVENTIONAL TGFFS ACCORDING TO THE DATA ACTIVITY *alpha*. (POWER AND DELAYS FROM CIRCUIT-LEVEL SIMULATIONS.)

FF	α=0	α=10	α=25	α=100
TGFF	1.00	1.00	1.00	1.00
ACFF	0.12	0.15	0.21	0.38
DICE FF	4.48	4.95	5.05	5.39
DICE ACFF	1.00	1.39	1.93	3.75
BCDMR FF	9.92	10.5	11.2	13.9
BCDMR ACFF	1.74	2.68	3.92	8.15
TMR FF	24.3	25.4	26.9	32.2

TABLE IV
SERS OF FFS COMPUTED BY EQ. (1). ($Q_{\rm crit}$ IS ESTIMATED BY CIRCUIT-LEVEL SIMULATIONS.)

FF	SER [FIT/Mbit]	SER/TGFF	1/(SER/TGFF)
TGFF	379	1.00	1.00
ACFF	285	0.75	1.32
DICE FF	1.22	0.0032	311
DICE ACFF	0.82	0.0022	462
BCDMR FF	0.17	0.00045	2349
BCDMR ACFF	0.16	0.00042	2369

the TGFF. The error rate of TMR FFs ($R_{\rm TMR}$) are computed from Eq. 5 using the error rate of TGFFs ($R_{\rm TGFF}$)

$$R_{\rm TMR} = 3R_{\rm TGFF}^2 - 2R_{\rm TGFF}^3 \quad (5)$$

When $R_{\rm TGFF}$=11.5% (CLK=0 in Table V), $R_{\rm TMR}$ is computed as 3.6% which is almost equivalent to the value of 6.1% in Table V.

The error rates of TGFF, 0.07% on the SOTB chip when CLK=1 is almost 1/200 compared with 15.6% of the bulk chip as shown in Fig. 14. The error rate of SOTB is smaller than bulk by two orders of magnitude. We observe no error on the redundant FFs in the SOTB chip. The SOTB process gives very high soft-error tolerance due to its lower sensitive volume.

VI. CONCLUSION

We propose low-power area-efficient redundant flip-flops, called DICE ACFF. Its structure is based on reliable DICE and the low-power ACFF. It achieves low-power at lower data-activity. If data activity is lower than 20%, its power is lower than conventional DFF based on transmission gates (TGFF). Conventional ASICs have 5% to 15% data activity. DICE ACFFs always achieve lower power than TGFF in these regions. Its area overhead is 2.1x of the TGFF and 1.05x of the conventional DICE FF. DICE ACFFs is superior to DICE FF in power, area and soft error resilience. We have implemented

TABLE V

BULK IRRADIATION RESULTS AT VDD=1.2V WITH NO BODY BIAS. NUMBER OF ERRORS FROM 300 SEC. α IRRADIATION AND ERROR RATES DEFINED AS THE RATIO BETWEEN THE NUMBER ERRORS AND TOTAL NUMBER OF FFS.

		ACFF	TGFF	TMR FF	BCDMR FF	BCDMR ACFF	DICE FF	DICE ACFF
# of Errors	CLK=0	1,911	4,672	1,053	10	15	0	0
	CLK=1	59	7,887	944	9	3	0	0
Total # of Errors		1,970	12,559	1,997	19	18	0	0
Total # of FFs		40,320		17,280	34,560		40,320	
Error Rate	CLK=0	4.7%	11.5%	6.1%	0.03%	0.04%	0	0
	CLK=1	1.5%	19.6%	5.5%	0.03%	0.01%	0	0
	Average	3.1%	15.6%	5.8%	0.03%	0.03%	0	0

TABLE VI

SOTB IRRADIATION RESULTS AT VDD=1.2V WITH -2.1V REVERSE BODY BIAS ON BOTH NWELL AND PWELL.

		ACFF	TGFF	TMR FF	BCDMR FF	BCDMR ACFF	DICE FF	DICE ACFF
# of Errors	CLK=0	3	0	0	0	0	0	0
	CLK=1	0	57	0	0	0	0	0
Total # of Errors		3	57	0	0	0	0	0
Total # of FFs		40,320		17,280	34,560		40,320	
Error Rate	CLK=0	0.01%	0	0	0	0	0	0
	CLK=1	0	0.14%	0	0	0	0	0
	Average	0.005%	0.07%	0	0	0	0	0

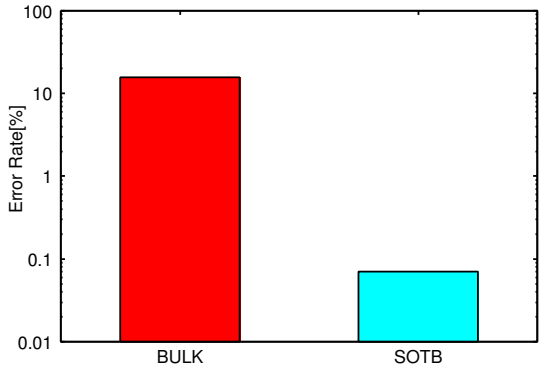


Fig. 14. Comparison of error rates of TGFFs between bulk and SOTB at VDD=1.2V.

arrays of DICE ACFFs and DICE FFs and other redundant and non-redundant FFs in both 65 nm bulk and SOTB processes. We observe no error on DICE FF and DICE ACFF by α particle irradiation for 300 sec. The error rate of TGFF of SOTB is smaller than bulk by two orders of magnitude. The SOTB process gives very high soft-error tolerance due to its lower sensitive volume.

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