A 65 nm Low-Power Adaptive-Coupling Redundant Flip-Flops

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Abstract

We propose a low-power redundant flip-flop to be operated with high reliability over 1GHz clock frequency based on the low-power ACFF and the highly-reliable BCDMR FF. Its power dissipation is almost equivalent to transmission gate FFs at 10% data activity while paying 3x area penalty. Experiments by α-particle and neutron irradiation reveals its highly-reliable operations with no errors at 1.2V and 1GHz.

Introduction

To protect FFs from soft errors caused by α particles or neutrons, several redundant flip-flop structures are proposed such as TMR, DICE[1] or BISER[2]. According to the process scaling, reliability is increasingly reduced. Currently, processors for servers are implemented with some redundancy to guarantee reliability. In the near future, redundancy must be used on consumer products for low-power portable applications. The conventional redundant FFs have large area and power overhead. It is very hard to reduce the area penalty since redundancy requires additional transistors. But the power penalty can be reduced to adapt lower power techniques. We propose a low-power redundant flip-flop with highly reliable operations over 1 GHz with almost same power as transmission gate FFs. We have fabricated a test chip in a 65 nm process. The chip contained several FFs with proposed FF. As for the power dissipation, BCDMR-ACFF has less than 38.5% of the original BCDMR obtained at 0% data activity from the measurement results. The experimental results by α particle and neutron irradiations show that no error is observed up to 1GHz operations on the proposed redundant FF array.

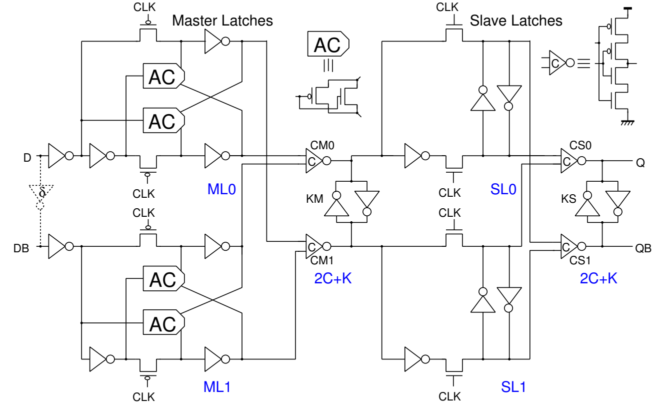

Fig. 1. Schematic diagram of BCDMR ACFF

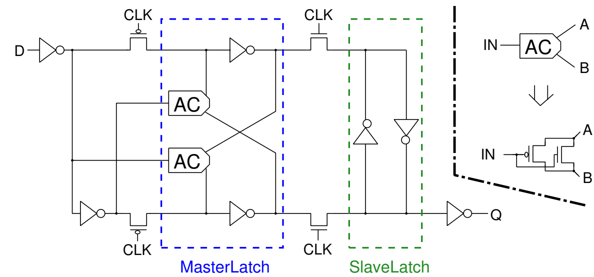

Fig. 2. Schematic diagram of ACFF

Low-Power Highly-Reliable Redundant Flip-Flop

Fig. 1 shows the proposed low-power highly-reliable redundant flip-flops named as "BCDMR-ACFF" based on the BCDMR FF [3] for high reliability and ACFF[4] for low-power operation.

Fig. 2 shows the schematic of ACFF. It operates with the single-phase clocking sheme using pass-transistor. Without using local clock buffers, power dissipation by them can be drastically reduced. To overwrite master latch is difficult because of PMOS pass-transistors. The Adaptive-Coupled (AC) two transistors makes it easy to overwrite the master latch by weaking the cross-coupled loop.

Fig. 3 shows the schematic of BCDMR. It consists of two pairs of master and slave latches and two "2C+K" parts. The "2C+K" parts includes two Muller's inverting C-elements and one keeper. If one of two latches is flipped by a temporal soft error, the C-element becomes a high impedance and the keeper keeps the original value. The "2C+K" from the BCDMR structure achieves highly-reliable operations at higher clock frequency. It is developed in order to mitigate a Single-Event Transient (SET) pulse between the master and slave latches. Fig. 5 shows two possible cases of upsets in redundant FFs caused by SET pulses coming to the input of master or slave latches. The SET pulse width is distributed from several hundred ps to 1000 ps according to the tap (well contact) density, gate sizes and etc. The possibility that an SET pulse is captured by latches depends on the clock frequency. If a pulse is injected at a clock edge, it will be captured by multiple redundant master or slave latches. For example, a 500 ps SET pulse is roughly captured by 50% at 1 GHz clock.

To remove a SET pulse coming to master latches, a delay element (δ) can be used as described by dotted lines in Fig. 3. However, the delay element between the master and slave latches makes the area and delay penalties much bigger. The BCDMR structure prevents a SET pulse to be captured by both of slave latches. It is based on the BISER structure, which is more area-efficient than the triple-modular redundancy (TMR). But the BISER structure has only a single C-element, which produces SET pulses to be captured by both of slave latches. On the other hand, in the BCDMR structure with duplicated C-elements, a SET pulse from CM0 is only captured by SL0. BCDMR FF based on the conventional

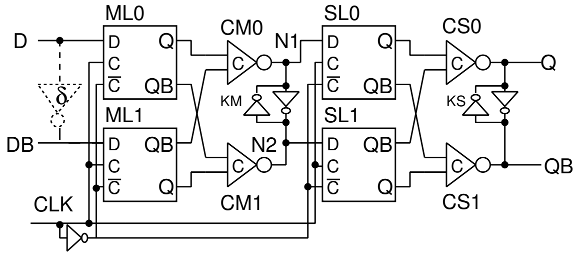

Fig. 3. Schematic diagram of BCDMR

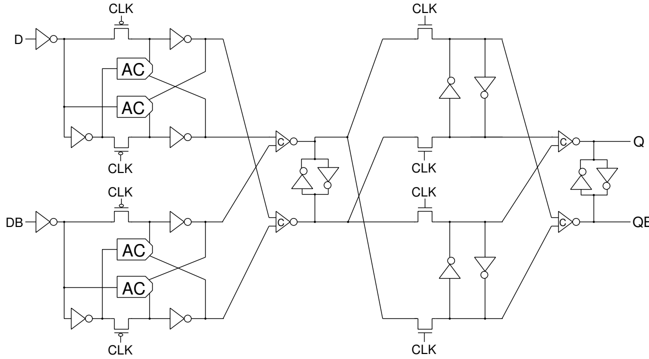

Fig. 4. Another schematic of BCDMR ACFF with smaller number of Trs, bit with lower resiliency.

TGFF shows over 100× better error resiliency than TGFFs by the spallation neutron irradiation[5].

Fig. 4 is another structure of BCDMR ACFF. The nunber of transistors is smaller than Fig. 1. However, a SET pulse from amaster latch may be captured by both of redundant slave latches. Thus the soructure in Fig. 1 is used to gurantee high reliability by dissipating two inverters.

Table I shows area, delay, power and ADP (area-delay-power) products of redundant and non redundant FFs. BCDMR-ACFF consumes over 4x higher power than transmission gate FF (TGFF) at the 100% data activity ($\alpha = 100\%$), while it consumes almost same power at $\alpha = 10\%$. Note that the power is obtained from circuit-level simulations by driving 8 FFs with a 2x clock buffer. Without adding the clock buffer, ACFF achieves much less power because no local clock buffer is required. The delay of the BCDMR-ACFF is almost equivalent and the area is 3x larger than TGFF. Fig. 6 shows power dissipation at 1.2V according to data activity normalized by TGFF. BCDMR-ACFF is less than original BCDMR below 40% data activity. BCDMR-ACFF achives low power operations, because average data activity of flip-flops in an SoC chip is typically between 5 and 15%. BCDMR-ACFF has less than 27% of the original BCDMR at 0% data activity. The ADP product in Fig. 7 of BCDMR-ACFF is about 2.0 at α=0%, which is almost 3.8x smaller than BCDMR FF implemented with TGFFs. We can construct a low-power BCDMR FF by using any kind of low-power master-slave edge-triggered FFs. It is the most significant advantages of the BCDMR structure.

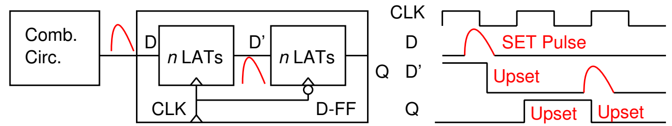

Fig. 5. SET pulse coming to the input of redundant master or slave latches (n LATs) to be captured by positive or negative edge of clock.

Table I: Area, delay and power of FFs normalized by TGFF.

FF	Area	Delay	α=10%	α=100%
			Power	
ACFF	1.05	0.72	0.51	1.21
BCDMR FF	2.84	1.27	2.21	2.73
BCDMR ACFF	3.16	1.11	1.16	3.79

Test Chip

We have fabricated a 2 mm×4 mm test chip in a 65 nm CMOS bulk process as in Fig. 8 with the detailed structures and the cell layout of the BCDMR-ACFF. The critical nodes are separated as far apart as possible without area penalty to eliminate a simultaneous flip of redundant components[5]. These four sorts of FFs are implemented on a die: BCDMR-ACFFs, BCDMR FFs, ACFFs and TGFFs on the twin-well (2W) structure, and BCDMR-ACFFs, BCDMR FFs on the triple-well (3W) structure. Table II shows bit numbers of these FFs. All those FFs are connected in series as a shift register. The chip has two clock pins, SHIFT_CLK and PLL_CLK. The former is used on the shift operation, while the latter is used during irradiation. To guarantee the hold restrictions of all serially-connected FFs, these clock signals are given from the tail of the shift register (CI to CO), while the shift input is given from the head (SI to SO). In order to measure soft-error resiliency of these FFs around 1GHz, PLL is used to multiply the clock up to 80x.

Fig. 9 shows the simplified schematic structure of the shift register and the clock distribution scheme. All FFs are connected in series on the shift operation (LOOP=0). Clock signals are also connected in series from head to tail, while all FFs are in the loop mode during irradiation, in which 8 FFs form a loop to capture flipped values. During irradiation, the clock signal is given from PLL_CLK. The whole clock distribution tree consists of a clock stem and clock branches

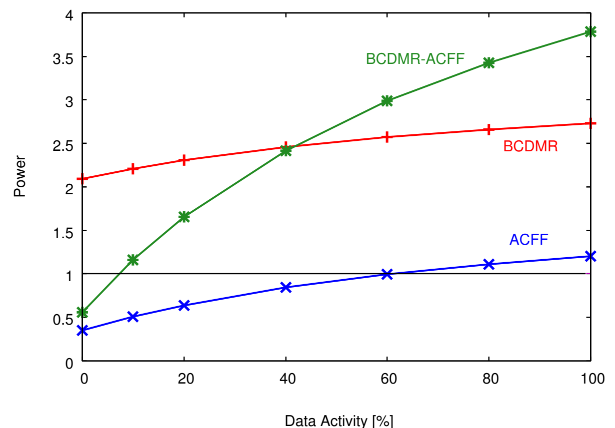

Fig. 6. Power dissipation at 1.2V according to data activity normalized by DFF.

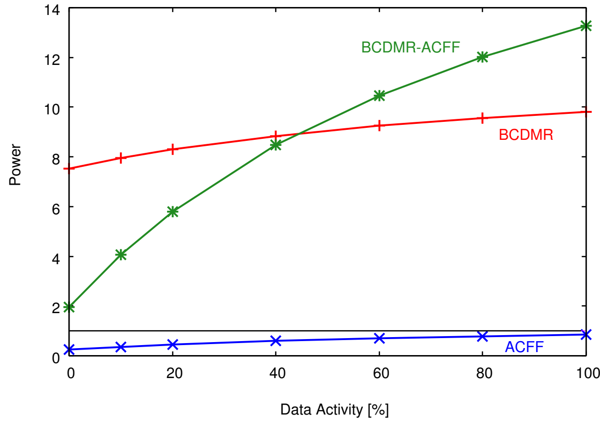

Fig. 7. ADP products at 1.2V according to data activity normalized by DFF.

Table II: No. of FFs on the fabricated chip.

	No. of FFs
TGFF	2336
ACFF	2272
BCDMR(3W)	16800
BCDMR(2W)	16800
BCDMR-ACFF(3W)	16384
BCDMR-ACFF(2W)	16384

to distribute higher clock frequency to FFs. If such higher clock is given from SHIFT_CLK through the clock branches in series, it disappears in the middle of the branches because of the propagation-induced pulse-width fluctuation.

Experimental Results

The error resilience of the FFs on the fabricated chip are measured by α-particles from 3M Bq $^{241}\mathrm{A_m}$ and neutron irradiations at RCNP of Osaka University. On the neutron irradiation, multiple DUTs were measured at the same time to increase the number of observed errors.

Fig. 10 and Table III shows the measurement results by α-particles and neutron irradiations respectively according to the clock frequency. ACFF has lower error rates than TGFF over all measured frequencies on the α irradiations. However, the results are different on the neutron irradiation. The error resilience of TGFF and ACFF seems to be almost equivalent. We observed a few errors in BCDMR and BCDMR-ACFF regions only at 0 Hz. BCDMR structure keeps value by two latchs and a keeper. If one latch is upset, the other latch and the keeper hold the correct value. The upset latch recovers when the next clock is injected to the FF. When no clock is applied, the upset latch remains upset. If the other latch is upset afterwards, the output of the FF becomes wrong.

No error is observed up to 1GHz in BCDMR and BCDMR-ACFF regions. BCDMR-ACFF has as high reliability as BCDMR.

We measured power dissipation of the redundant FFs on the fabricated chip by changing the data activities. It is possible to give the clock signal only on the specified FF region in the fabricated chip. The local loop structure in the upper-right side of Fig. 9 can be used to change the data activities, α. When these 8 FFs stores the same value, α is equal to 0%, while it becomes 100% by storing the checker-board pattern in these 8 FFs. Fig. 11 shows the measurement results

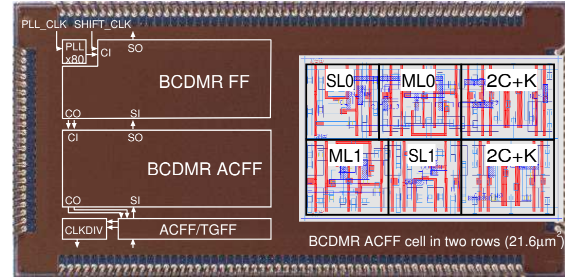

Fig. 8. Chip micrograph with detailed structure and BCDMR ACFF layout

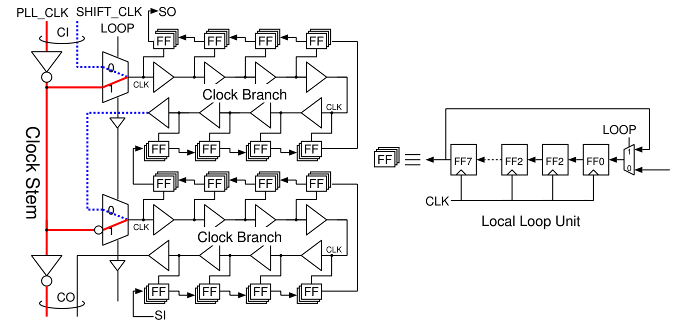

Fig. 9. Clock distributions to guarantee over 1 GHz operations during soft-error experiments and no-hold violations at shift operations

at 1.2V supply voltage normalized by the power of TGFF. FFs implemented with the ACFF structure achieve low-power operations at lower data activites. At the 0% data activity, BCDMR-ACFF has less than 38.5% of the original BCDMR.

Conclusions

We have fabricated a 65-nm chip including the low-power redundant FF called BCDMR-ACFF by using low-power ACFF and the highly-reliable BCDMR FF. The ADP product of BCDMR-ACFF is smaller than the original BCDMR when data activity is below 40%. At 0% data activity, the ADP product of BCDMR-ACFF is 2x larger than the TGFF. No error is observed in the proposed BCDMR-ACFF up to 1GHz clock frequency except 0Hz by the α-particle and neutron irradiation. As for the power dissipation, BCDMR-ACFF has less than 38.5% of the original BCDMR at 0% data activity

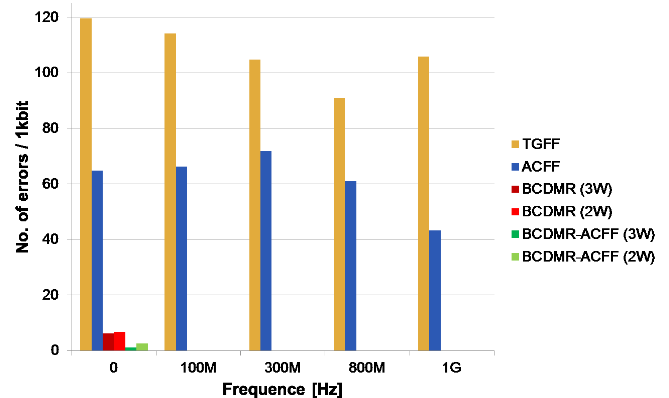

Fig. 10. No. of errors (flipped FFs) per 1kbit by 5min. α irradiations at 1.2V.

Table III. Soft Error Rate (FIT/Mbit) from neutron irradiations at 1.2V.

	Freq.(MHz)			
	100	300	800	1000
TGFF	362	306	268	251
ACFF	291	267	250	321
BCDMR(3W)	0	0	0	0
BCDMR(2W)	0	0	0	0
BCDMR ACFF(3W)	0	0	0	0
BCDMR ACFF(2W)	0	0	0	0

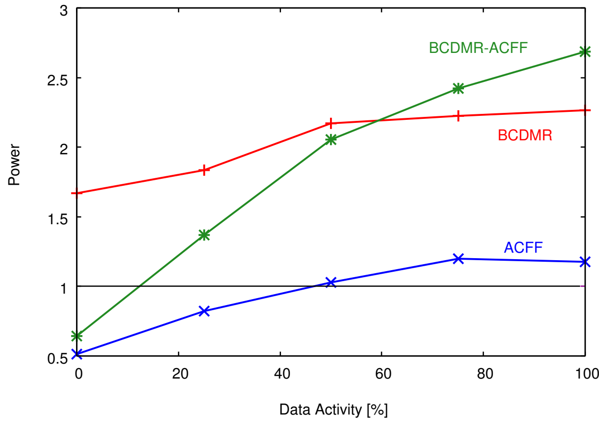

Fig. 11. Measured power dissipations at 1.2V normalized by the power of TGFF

from the measurement results. TGFFs and ACFFs are also integrated on the same die. From the α irradiation results, ACFF has better error resilience than TGFF while they have almost same error rates by the neutron irradiation. We expect that the BCDMR-ACFF has better error resilience than the original BCDMR for α particles, becasuse BCDMR-ACFF is based on ACFF.

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