Soft-error Tolerance by Guard-Gate Structures on Flip-Flops in 22/65 nm FD-SOI Technologies

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***Abstract*—We evaluated soft-error tolerance by heavy-ion irradiation test on three-types of flip-flops (FFs) called the standard FF (STDFF), the dual feedback recovery FF (DFRFF), and the DFRFF with long delay (DFRFFLD) in 22/65 nm FD-SOI technologies. The guard-gate (GG) structure in the DFRFF mitigates soft errors. An SET pulse is removed by the C-element with the signal delayed by the GG structure. DFRFFLD increases the GG delay by adding two more inverters as delay elements. We investigate the effectiveness of GG structure in 22 nm and 65 nm. In 22 nm, Kr (40.3 MeV-cm^2/mg) irradiation tests revealed that DFRFFLD has sufficient soft-error tolerance in outer space. In 65 nm, the relationship between GG delay and CS reveals the GG delay time which no error was observed under Kr irradiation.**

***Index Terms*—soft error, heavy ion, FD-SOI, 22 nm, flip-flop, guard-gate, radiation-hard.**

I. Introduction

Process scaling results in high integration density and low power consumption. Soft errors are one of the important reliability issues. When a radiation particle hits a transistor, an error pulse is generated, which is called a single event transient (SET) pulse. A single event upset (SEU) occurs when a SET pulse is generated in a storage element such as SRAM or flip-flop (FF).

In the device level, the fully-depleted silicon on insulator (FD-SOI) process has around 10-100x higher soft-error tolerance than the bulk process[1]. It is because the buried oxide (BOX) layer prevents charge collected from substrate. However, soft errors still occur on FFs on FD-SOI structure. Soft errors in FD-SOI are mainly caused by parasitic bipolar effects (PBEs). Therefore, circuit-level countermeasures are mandatory for mission-critical applications.

In the circuit level, several redundant FFs such as triple modular redundancy (TMR) [2] and dual interlocked storage cell (DICE) [3][4] have been proposed as radiation-hardened structures. However, they have larger area, delay, and power overheads than conventional standard FFs. Therefore, radiation-hard FFs with minimum overheads are required.

In this paper, we evaluate soft-error tolerance of FFs in 22 nm and 65 nm FD-SOI processes by heavy-ion irradiation test and investigate the effect of the guard-gate structure[5] in 22 nm and 65 nm. We explain device architectures and several types of FFs evaluated for soft-error tolerance in Section II. Section III explains the heavy-ion irradiation test. Section IV explains the experimental results and the discussion. We conclude this paper in Section V.

TABLE I: Parameters of FD-SOI.

Technology node	Gate length [nm]	Body thickness [nm]	BOX thickness [nm]
22 nm	28	12	20
65 nm	65	12	15

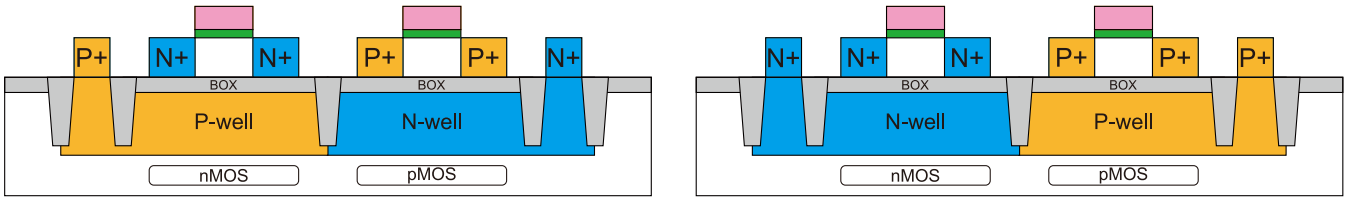
II. Proposed FFs in FD-SOI

The thin-BOX FD-SOI process with low power and high performance is used for aerospace and automotive applications. The performance can be optimized by changing body bias through the thin BOX layer. Fig. 1 shows the cross sections of thin BOX FD-SOI devices in 22/65 nm. In 22 nm, the flip-well architecture is adopted instead of the conventional well architecture in 65 nm[6]. In the flip-well architecture, the performance of pMOS is higher than conventional because the body bias of both pMOS and nMOS is usually set to 0 V. Table I shows the parameters of 22/65 nm processes[7][8].

We designed three types of FFs, a standard FF (STDFF), and two radiation-hardened FFs (DFRFF, DFRFFLD), in 22/65 nm thin BOX FD-SOI processes. In 22 nm, all FFs have reset and scan input pins.

Fig. 2 shows STDFF without radiation hardness. STACKEDFF shown in Fig. 3 is radiation-hard FF by the stacked transistors[9]. STACKEDFF is composed of latches composed of stacked inverters and stacked tristate inverters. The stacked structure in SOI prevents the PBE. The PBE is the main cause of soft errors in SOI. However, STACKEDFF has larger performance overheads than STDFF. In particular, the delay time of STACKEDFF is reported to be around 2x of STDFF[10][11].

Fig. 4 shows the dual feedback recovery flip-flop (DFRFF)[12]. DFRFF is a radiation-hardened flip-flop with a small delay overhead. The GG structure in DFRFF mitigates soft errors. However, the delay of the GG structures (GG delay) within the DFRFF becomes small and must be increased to protect long SET pulses generated in outer space by a heavy-ion hit. In this work, the GG delay of the primary latch (PL) is increased from [12] by swapping inputs of the C-element of the secondary latch (SL). Moreover, DFRFF in Fig. 4 adopt the different stacking structure than STACKEDFF and DFRFF in [12] as shown in Fig. 5. The on-state nMOS transistor with CLK input are placed between two off-state



(a) Conventional well structure. Regular threshold voltage type.

(b) Flip well structure. Low threshold voltage type.

Fig. 1: Cross sections of thin BOX FD-SOI devices.

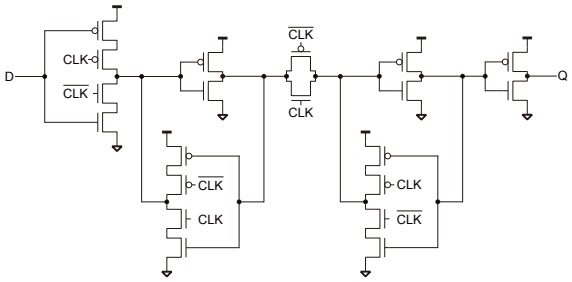


Fig. 2: Standard D-FF (STDFF).

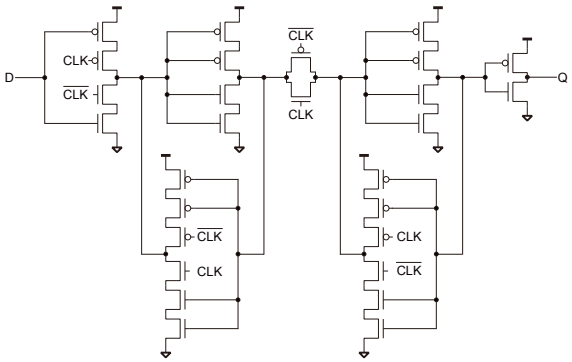


Fig. 3: STACKEDFF.

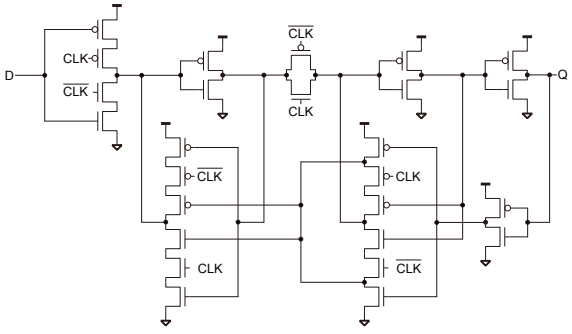
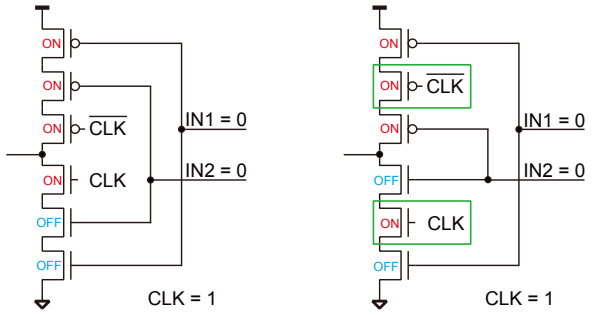


Fig. 4: The dual feedback recovery flip-flop (DFRFF).

nMOS transistors. It prevents radiation particles from hitting in two off-state transistors simultaneously.



(a) Conventional type.

(b) Proposed type.

Fig. 5: Two types of C-elements.

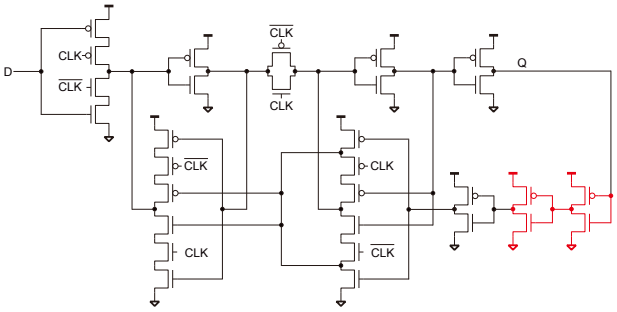


Fig. 6: DFRFFLD. The red inverters are added as GG delay elements.

Fig. 6 shows the dual feedback recovery flip-flop with long delay (DFRFFLD). DFRFFLD increases the GG delay by adding two more inverters as delay elements. In the 22 nm process, the output inverter is outside of the GG delay element.

Table II shows the simulation results of area, delay, and power consumption at 10% data activity of STDFF, STACKEDFF, DFRFF, and DFRFFLD in 22/65 nm. The supply voltage (V_{DD}) is set to 0.8 V and 1.2 V in 22 nm and 65 nm, respectively. Delay is defined as the sum of the setup time and CLK-to-Q delay. Power consumption is estimated at 10% data activity.

In 65 nm, delay overheads of both DFRFF and DFRFFLD are kept below 10%. Comparing DFRFF and DFRFFLD

TABLE II: Comparison of Area, Delay, and Power in 22/65 nm. ADP refers to the Area, Delay, and Power.

	Area		Delay		Power		ADP	
	22 nm	65 nm	22 nm	65 nm	22 nm	65 nm	22 nm	65 nm
STDFF	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
DFRFF	1.94	1.18	1.90	1.09	1.47	1.16	5.40	1.49
DFRFFLD	2.05	1.35	1.84	1.08	1.60	1.15	6.02	1.68

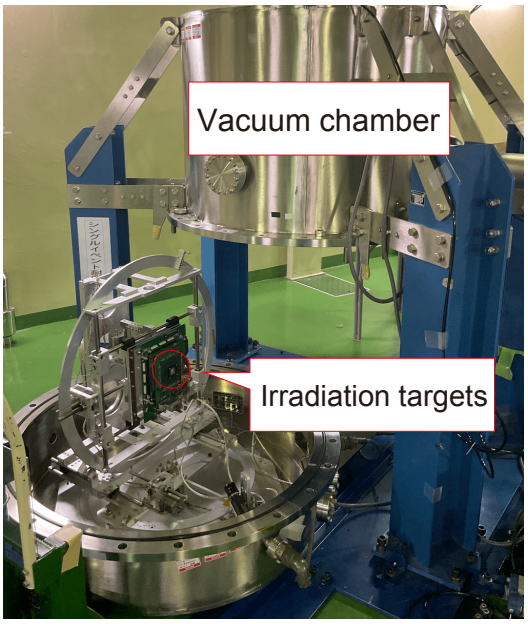


Fig. 7: Measurement setup. A vacuum chamber was used to prevent attenuation of the heavy ion beam by air.

TABLE III: LET and energy of irradiated heavy ions.

	Ar	Kr
LET [MeV-cm^2/mg]	15.8	40.3
Energy [MeV]	137	289

results, there is no significant overhead in delay or power consumption by adding delay elements of GG.

In 22 nm, all performance overheads are large unlike 65 nm. This is because that performances are limited by strict design rules. In particular, the significant large area overhead is due to dummy transistors in the C-elements of DFRFF and DFRFFLD. The source and drain of all dummy transistors are always shorted. In 22nm, even the low-overhead radiation-hard FFs have large performance overhead, which means large-overhead radiation-hard FFs such as DICE have much more performance.

III. Heavy-ion Irradiation Test

The test chips were fabricated in 22/65 nm FD-SOI. All FFs are implemented in shift registers. Heavy ion irradiation test was conducted by Ar and Kr at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA). Fig. 7 shows the experimental setup of the heavy-ion irradiation tests. Table III shows linear energy transfer (LET) and energy of irradiated heavy ions. Fig. 8 shows the existence probability of heavy

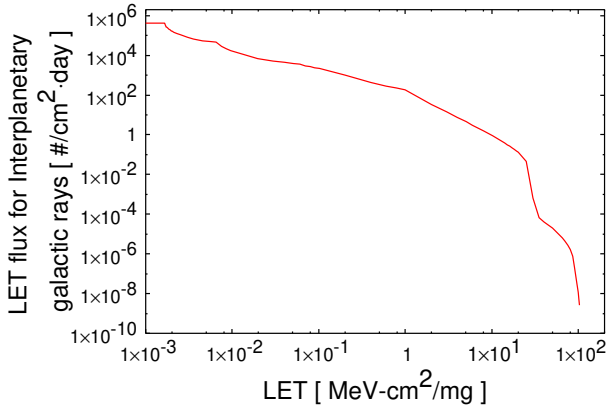


Fig. 8: LET distribution of heavy ions in outer space[13].

ions in outer space[13]. The number of particles above 40 MeV-cm^2/mg is very small in outer space compared to that of particles below 40 MeV-cm^2/mg. Secondary ions generated by a neutron hit with Si is mainly less than 18 MeV-cm^2/mg which is close to LET of Ar[14]. The measurement procedure is as below.

1. Initialize all FFs by 0 or 1.
2. Irradiate ions with clock signal fixed to 0 or 1.
3. Read out all FFs.

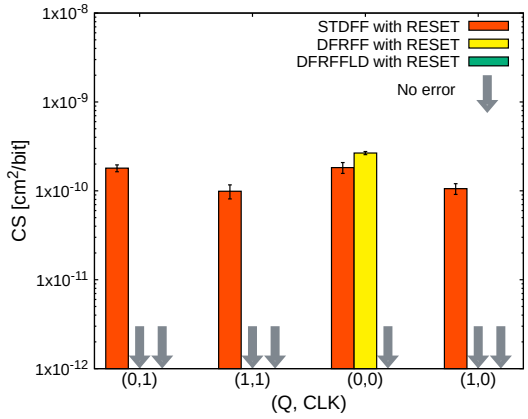
Irradiation tests were performed in the four static conditions of $(\mathrm{Q}, \mathrm{CLK}) = (0,0), (0,1), (1,0), (1,1)$. The cross section (CS, σ_{SEU}) represents the soft-error tolerance. CS refers to the upset area when a particle passes through the circuit block. CS is calculated by Eq. (1) using the number of errors (N_{error}), the number of FFs (N_{FF}), the effective heavy-ion fluence per cm^2 (N_{ion}), and the angle of heavy-ion to the chips (θ)[15]. In this measurement, Heavy ions were irradiated to the TEG chip perpendicularly ($\theta = 0°$).

$$\sigma_{\mathrm{SEU}}\,[\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}} \times N_{\mathrm{ion}} \cos\theta}. \quad (1)$$

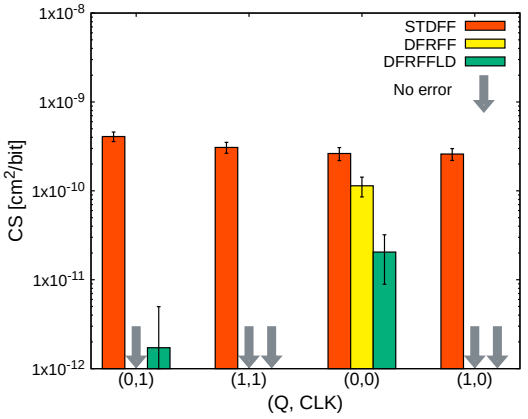
IV. Experimental Results and Discussion

Figs. 9 and 10 show the experimental results of the CS of 22/65 nm by Ar and Kr with error bars of 95% confidence. V_{DD} is set to 0.8 V in 22 nm and 1.2 V in 65 nm. In this work, we assume that SET pulses are generated only in nMOS transistors because more than 90% of soft errors are generated by heavy ion hits on nMOS transistors[16].

At $(\mathrm{Q}, \mathrm{CLK}) = (0,1)$, the soft-error tolerance of both DFRFF and DFRFFLD in 22/65 nm have more than 200x of STDFF under Ar irradiation as shown in Fig. 9. However, the soft-error tolerance in 65 nm is only around 20x of STDFF under Kr irradiation as shown in Fig. 10 (b). The SET pulses are generated at the outputs of the feedback gates in the PLs or the clocked inverters at D. However, the feedback gates are stacked transistors and no SET pulse is generated at the stacked feedback gates and the transmission gates in SLs at $(\mathrm{Q}, \mathrm{CLK}) = (1,0)$. In 22 nm, the transmission gates are attached at the input of PL as shown in Fig. 11 and no

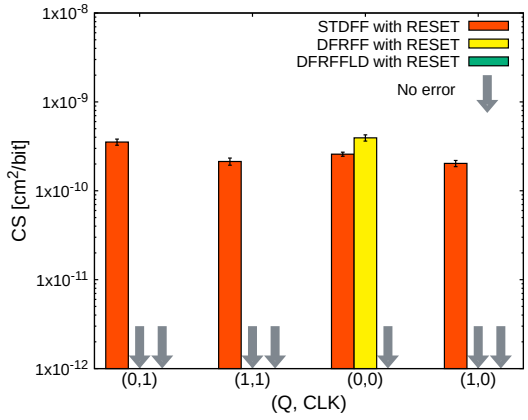


(a) In 22 nm ($V_{\mathrm{DD}} = 0.8\,\mathrm{V}$).

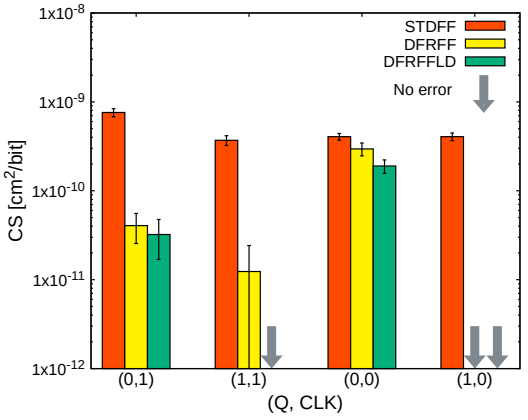


(b) In 65 nm ($V_{\mathrm{DD}} = 1.2\,\mathrm{V}$).

Fig. 9: Experimental results of the CS by Ar irradiation. The error bars at no errors are less than $2 \times 10^{-13}\,\mathrm{cm}^2/\mathrm{bit}$.



(a) In 22 nm ($V_{\mathrm{DD}} = 0.8\,\mathrm{V}$).



(b) In 65 nm ($V_{\mathrm{DD}} = 1.2\,\mathrm{V}$).

Fig. 10: Experimental results of the CS by Kr irradiation. The error bars at no errors are less than $2 \times 10^{-13}\,\mathrm{cm}^2/\mathrm{bit}$.

error was observed. Therefore, the SET pulses in 65 nm are generated at the inverters at D. Thus, the clocked inverter at D must be split into an inverter and a transmission gate as in SL to increase radiation hardness.

At $(\mathrm{Q}, \mathrm{CLK}) = (0, 0)$, DFRFF is as vulnerable as STDFF in both of 22 nm and 65 nm because of the insufficient GG delay in SL. Therefore, the soft-error tolerance of DFRFFLD with more delay elements than DFRFF is improved. In particular, DFRFFLD in 22 nm has no error under all conditions having enough soft-error tolerance for outer space use.

However, the improvement of CS of DFRFFLD in 65 nm is small at $(\mathrm{Q}, \mathrm{CLK}) = (0, 0)$ as shown in Figs. 9 (b) and 10 (b). In particular, the soft-error tolerance of DFRFFLD in 65 nm is only around 2x of STDFF under Kr irradiation. We investigate the relationship between the GG delay and CS under Kr irradiation in 65 nm as shown in Fig. 12. The blue line refers to the fitting function as shown in Eq. (2).

$$\sigma_{\mathrm{SEU}}\,[\mathrm{cm}^2/\mathrm{bit}] = -3.37 \times t\,[\mathrm{sec}] + 3.94 \times 10^{-10}. \quad (2)$$

According to Eq. (2), CS become $0\,\mathrm{cm}^2/\mathrm{bit}$ at 117 ps GG

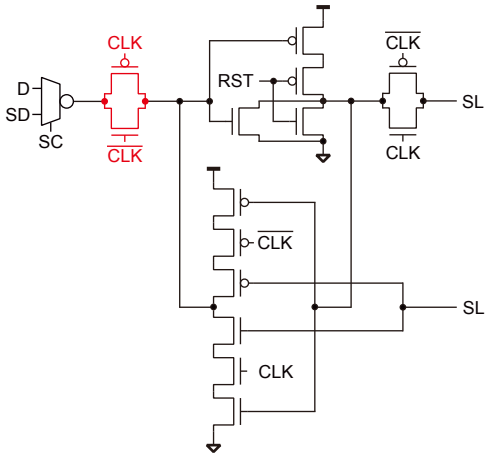


Fig. 11: The PL of DFRFF and DFRFFLD in 22 nm.

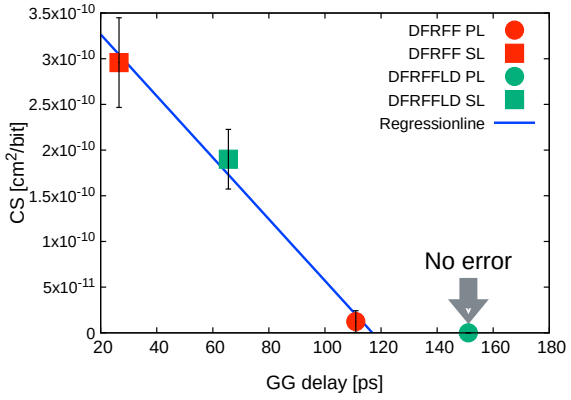


Fig. 12: Comparison between the GG delay and CS under Kr irradiation in 65 nm. At the point where the GG delay of PL on DFRFFLD was 151 ps, no error was observed.

delay. Thus, the width of most SET pulses generated by Kr in 65 nm is less than 117 ps. The GG delay must be longer than 117 ps to prevent errors by Kr.

V. Conclusion

We evaluated the soft-error tolerance of three types of FFs, STDFF, DFRFF, and DFRFFLD, in 22/65 nm FD-SOI by heavy-ion irradiation. In 22 nm, DFRFFLD has no error under all conditions. Therefore, DFRFFLD in 22 nm has enough soft-error tolerance for outer space use. In 65 nm, DFRFFLD has only about of STDFF under Kr irradiation. The relationship between GG delay and CS reveals the condition of GG delay which no error was observed under Kr irradiation. The GG delay must be longer than the condition to prevent errors by a heavy ion hit.

VI. Acknowledgment

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