Single Bit Upsets versus Burst Errors of Stacked-Capacitor DRAMs Induced by High-Energy Neutron - SECDED is No Longer Effective -

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***Abstract*—We measured soft errors on two 8Gb DRAMs by neutron irradiation. The results showed that the soft error rates for both DRAMs were about 3 FIT/Gb. An SBU that can be corrected by ECC were rarely measured, while burst errors caused by soft errors on peripheral circuits become dominant. Burst errors cannot be corrected by conventional ECC. Thus the SEC (Single Error Correction) mandatory in DDR5 cannot recover soft errors.**

***Index Terms*—DRAM, SEU, Burst Error, Stacked Capacitor, Trench Capacitor, ECC, SECDED**

I. Introduction

Prior to DDR4, DRAM technology maintained high yield and reliability by providing redundant rows and columns in memory cells [1]. The DDR5 standard approves the mandatory use of SEC (Single Error Correction) [2]. Each 128-bit data bit is stored in DRAM with additional 8-bit parity. In [3], DDR4 SDRAM and DDR3 SDRAM were irradiated with protons to evaluate the soft error tolerance of DRAMs. In this paper, we investigate the effectiveness of SECDED against soft errors in DRAMs by irradiating LPDDR4 and GDDR5 SDRAMs with neutrons and examining the types of soft errors.

II. Stacked DRAM Structure to Reduce Soft Error Rates

Soft errors were firstly reported on DRAM [4]. However, the soft error rate of DRAM is decreasing due to aggressive process scaling [5]. The descreaing trend discussed in [5] is mainly because of constant cell capacitance in spite of process scaling.

A conventional DRAM cell has a trench capacitor and a planar MOSFET as shown in Fig. 1. When a radiation particle penetrate to the Si substrate and hit an Si atom, generated electron-hole pairs charges the trench capacitor. That is the main source of soft errors on DRAMs with the trench capacitor. The other type of DRAM capacitors is called "Stacked Capacitor" [6] as shown in Fig. 2. Access transistors of the stacked capacitor DRAM are fabricated by digging into the Si substrate which reduces leakage cirrent by the long channel length. The stacked capacitor reduces leakage current is strong against soft errors since the stacked capacitor is placed far apart from the substrate Recent DRAM process technologies are based on the stacked capacitor [7].

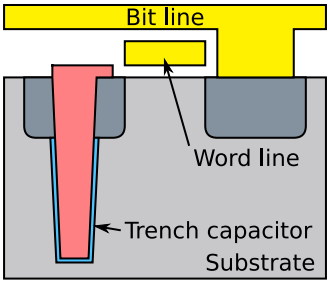


Fig. 1: Trench capacitor and planar MOSFET

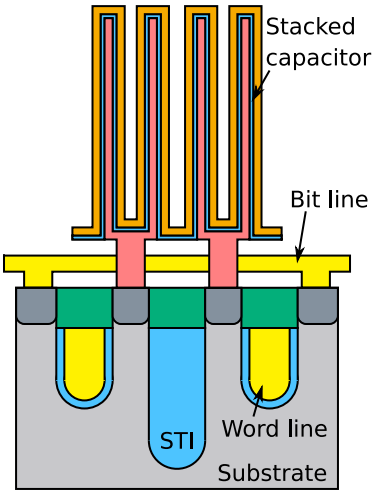


Fig. 2: Stacked capacitor and trench MOSFET

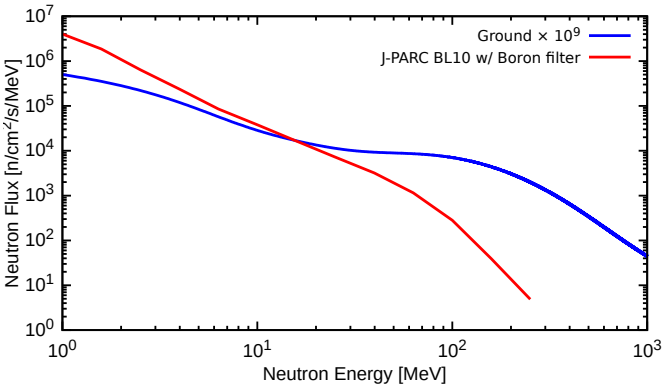


Fig. 3: The irradiated neutron and natural terrestrial neutron spectrum

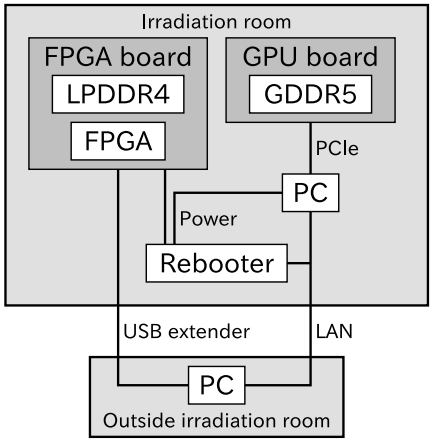
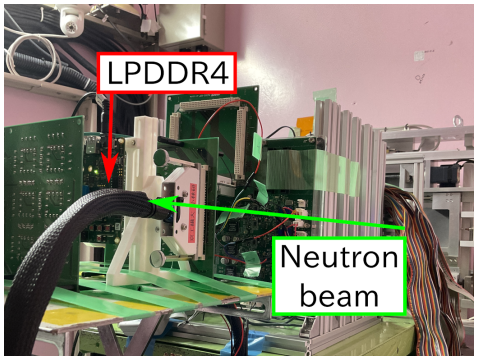
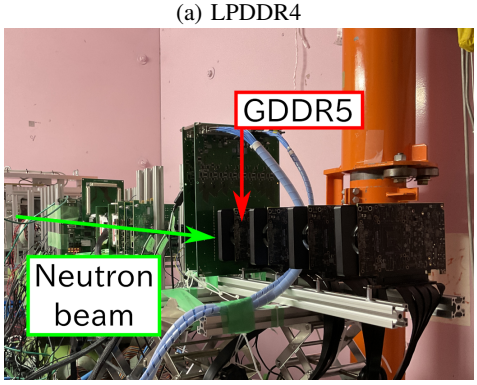


Fig. 4: Measurement system



(a) LPDDR4



(b) GDDR5

Fig. 5: Measurement setup

TABLE I: Test patterns

	Example	Description
A0	0x00000000	All 0
A1	0xFFFFFFFF	All 1
CHB	0x55555555/ 0xAAAAAAAA	Checker board
ADR	0x12345678	Store address

III. NEUTRON EXPERIMENT

A. Experimental Facility

Neutron irradiation experiments were conducted at the beam line 10 (BL10) of Materials and Life Science Experimental Facility (MLF) in the Japan Proton Accelerator Research Complex (J-PARC). Fig. 3 shows a comparison of the irradiated neutron and natural terrestrial neutron spectrum.

B. Device Under Test

Two types of DRAMs, LPDDR4 SDRAM and GDDR5 SDRAM, were irradiated. The capacity of those DRAMs is 8 Gb/chip fabricated in a 1X nm process. The LPDDR4 SDRAM is the IS43LQ32256A-062BLI from Integrated Silicon Solution Inc. It is mounted on Trenz's TE0802 FPGA board. GDDR5 SDRAM is MT51J256M32HF-80:A of Micron Technology Inc. It is mounted on Nvidia's Quadro P2000 GPU board.

C. Experimental Setup

Figs. 4 and 5 show the schematic of the measurement system and the measurement setup, respectirely.

The FPGA board equipped with LPDDR4 is connected to the PC placed outside the irradiation room with a USB extension cable to initialize the FPGA and acquire error information. The GPU board equipped with GDDR5 is connected to the control PC in the irradiation room with a 2 m PCI Express cable. The control PC and power supply are installed under an experimental table to reduce neutron flux. The control PC is operated via SSH from the PC outside the irradiation room. When the experimental system becomes unstable, the power supply is turned off and on using the rebooter.

D. Experimental Method

Each DRAM is initially written once and then read back periodically. Four types of test patterns are prepared as shown in Table I. One of these patterns is selected and written to all areas of the memory.

The pattern initially written are compared with the read-out data. If they are different, it determines that soft errors occur and the address and erroneous data are saved. It took about

TABLE II: Error classification

SBU (Single Bit Upset)	Error in a single bit.
RB (Row Burst)	Burst errors along rows.
CB (Column Burst)	Burst errors along columns.
SEFI (Single Event Functional Interrupt)	Malfunction.

TABLE III: Number of observed errors

DUT	Error type	Number of observed errors
LPDDR4 (8Gb)	RB	40
GDDR5 (32Gb)	SBU	152
	RB	14
	CB	84
	SEFI	9

3 minutes for LPDDR4 and about 10 seconds for GDDR5 to check errors once in all areas of the DRAMs.

IV. Measurement Results

Total neutron irradiation time was 30.62 hours for LPDDR4 and 55.20 hours for GDDR5. Average neutron flux above 10 MeV was 6.35×10^8 n/cm^2/h.

The errors are classified into the four types as shown in Table II. SBUs are errors that occur in memory cells, and burst errors come from the DRAM peripheral circuitry [8].

Table III shows the number of observed errors. The breakdown of errors are shown in Fig. 6. Only row-burst errors were observed in LPDDR4.

Examples of error locations in each DRAM are shown in Figs. 7 and 8. These graphs depicts a two-dimensional arrangement of the entire memory area, with the rows corresponding to the upper bits of the address and the columns to the lower bits. The address where an error was observed is dotted.

Specific examples of error patterns were shown in Table IV. In both DRAMs, burst errors were often observed in which one byte out of a 32 bit word was changed.

SER is calculated by Eq. 1 using the number of errors (N_{error}), measurement time (t), memory capacity (N_{mem}), and acceleration factor (AF). One burst error is regarded as one error. Table V shows parameters to compute SER. The AF

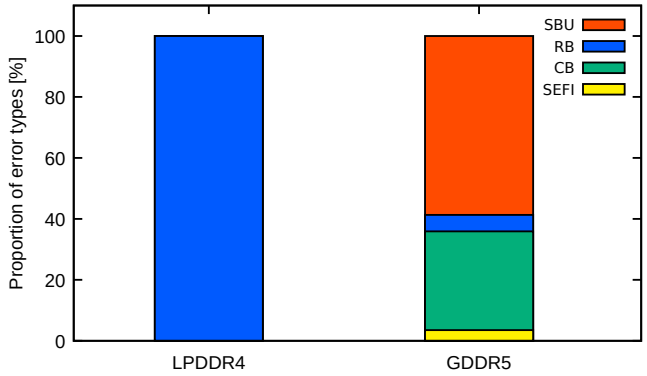


Fig. 6: Breakdown of observed errors

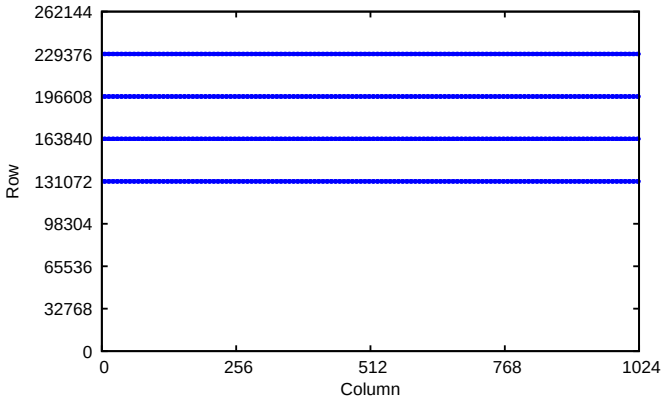


Fig. 7: LPDDR4. All errors were row burst.

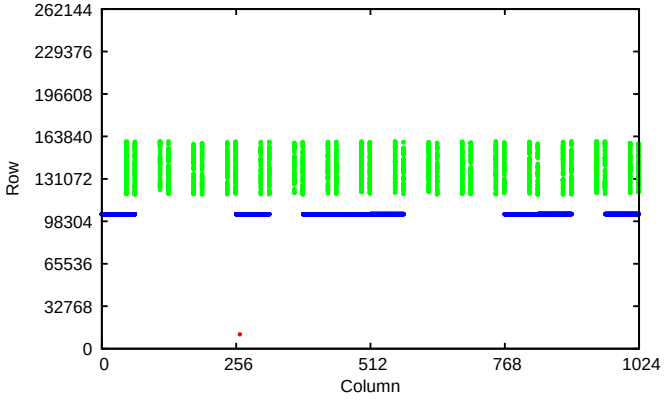


Fig. 8: DGGR5. The red dot represent single bit upset. The blue dots represent row burst. The green dots represent column burst.

TABLE IV: Example of typical errors

Correct data	Errors
0x00000000	0x0000AA00
	0x00EA0000
	0x00000017
	0x80000000
0xFFFFFFFF	0xFFFF51FF
	0xFFFFFF59
	0xFF4FFFFF
0x55555555	0x55AA5555
	0x55555522
0xAAAAAAAA	0xAAAAAA8A
	0x16AAAAAA
0x042E7000	0x042E7023
0x05D1D000	0x0555D000
0x142E7000	0x142E702D

was computed as 4.9×10^7 by using 12.946 n/cm^2/h of the terrestrial neutron flux over 10 MeV defined in [9].

$$\mathrm{SER[FIT/Gb]} = \frac{N_{\mathrm{error}} \times 10^9 \times 1024^3}{t[\mathrm{h}] \times N_{\mathrm{mem}} \times AF}. \quad (1)$$

The SER of LPDDR4 was 3.32 FIT/Gb and that of GDDR5 was 2.99 FIT/Gb.

Burst errors were always observed within a specific, but were not observed across multiple bytes. Thus the burst

TABLE V: Parameters to calculate SER

	N_{error}	t[h]
LPDDR4	40	30.62
GDDR5	259	55.20

errors come from peripheral circuits per byte such as address decoders.

V. Conclusion

Soft error tolerance of two types of DRAMs were compared by neutron irradiation experiments. SBUs, row bursts, column bursts, and SEFIs were observed in GDDR5. However, in LPDDR4 no SBU was observed, and only row bursts were observed. Errors other than SBUs cannot be corrected by the conventional ECC because they generate a large number of errors in a word. In the DDR5 standard, ECC becomes mandatory [2], but SECDED is no longer useful to protect DRAMs from soft errors. Multiple memory chips must be combined to form an error-correcting code, such as chipkill [10].

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