MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

QUEST2024

QUBECS
Quantum Bit Error Correction System
Moonshot Goal 6

Classical Electronics to Control Qubits and Correct Errors in Room-temperature and Cryogenic Environments

Prof. Kazutoshi Kobayashi

Kyoto Institute of Technology (KIT), Japan

Project Manager of Moonshot Goal 6

https://www.greenlab.kit.ac.jp/qubecs/

Keynote at Quest 2024 in Kyushu

Agenda

- **Self Introduction**
- **Introduction**
  - ✓Moonshot Goal 6 for quantum computers
  - ✓Integrated circuits (Classical electronics) and quantum computers
- **QUBECS**
  - ✓Overview of my project for developing an FTQC (Fault-tolerant quantum computer)
- **Conclusion**

Prof. Kazutoshi Kobayashi

- **Graduated from Kyoto University, 1991 (BE), 1993 (ME). Ph. D in 1999**
  - ✓ One of mentors was Prof. Yasuura (Former vice president of Kyushu Univ.) as same as Prof. Koji Inoue
- **Research Topics: CiM (Computing in Memory) for Ph. D thesis, system-level design (SystemC), variation-aware FPGA, reliability issues (soft error and aging degradation) , power electronics and etc.**

  One of the most famous professors in the field of semiconductor reliability in Japan
- **From 2022, Project Manager of the Moonshot goal 6 for FTQC (Fault-tolerant quantum computer)**

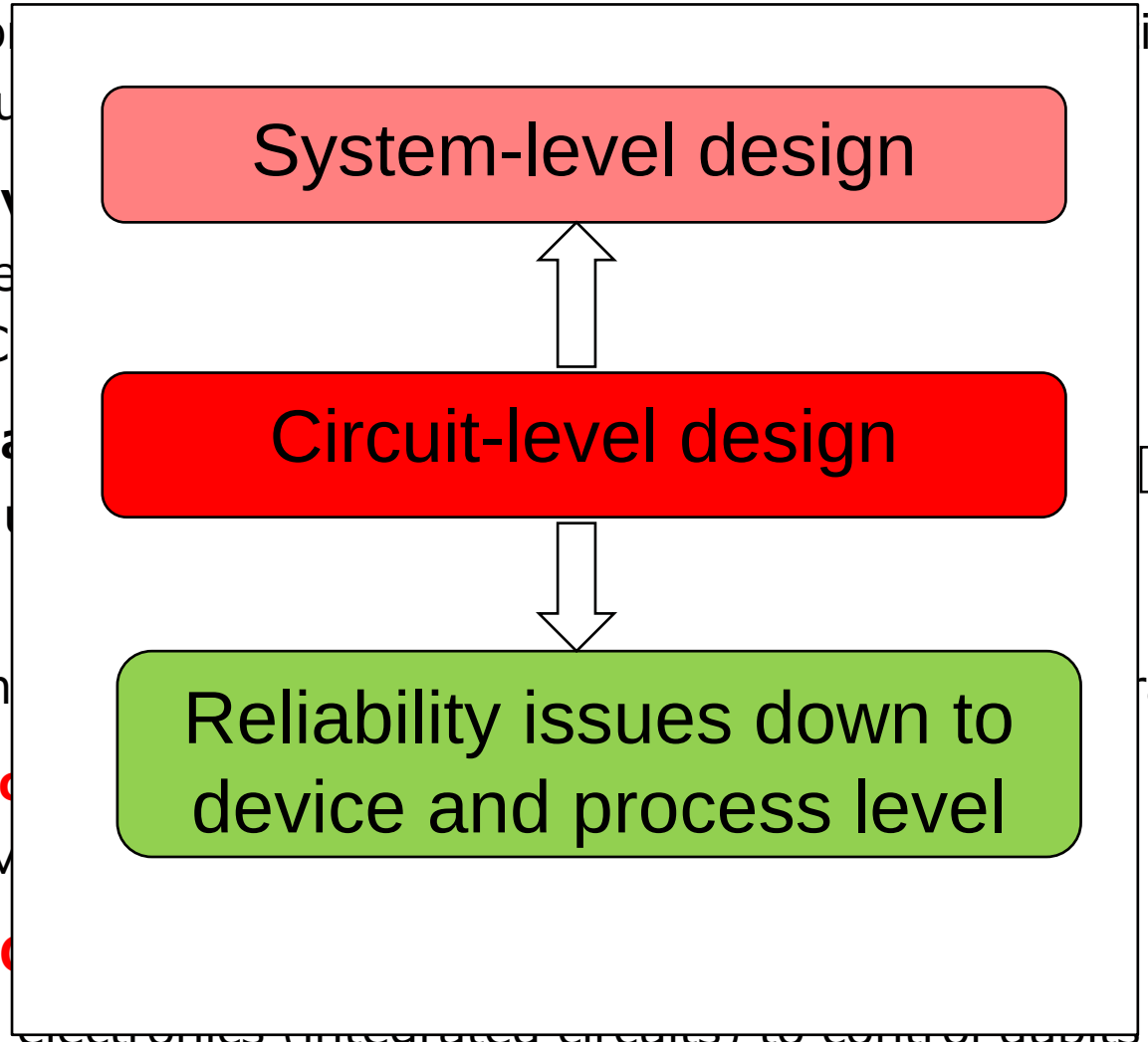
Prof. Yasuura and Prof. Inoue

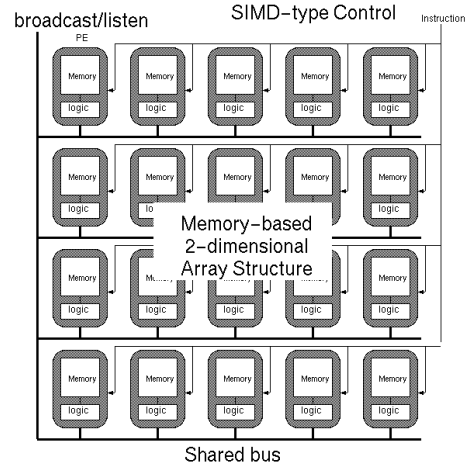
My Research History`

- **Computing in Memory (CiM) (1991-2000)**
  - ✓ CAM (Co
  - ✓ FMPP (Fu
- **System-lev**
  - ✓ Resource
  - ✓ SystemC
- **Variation-a**
  - ✓ Reconfigu
- **Reliability**
  - ✓ Variation
- **Power Elec**
  - ✓ Gate driv
- **Quantum C**
  - ✓ Classical electronics (integrated circuits) to control qubits and correct errors on qubits

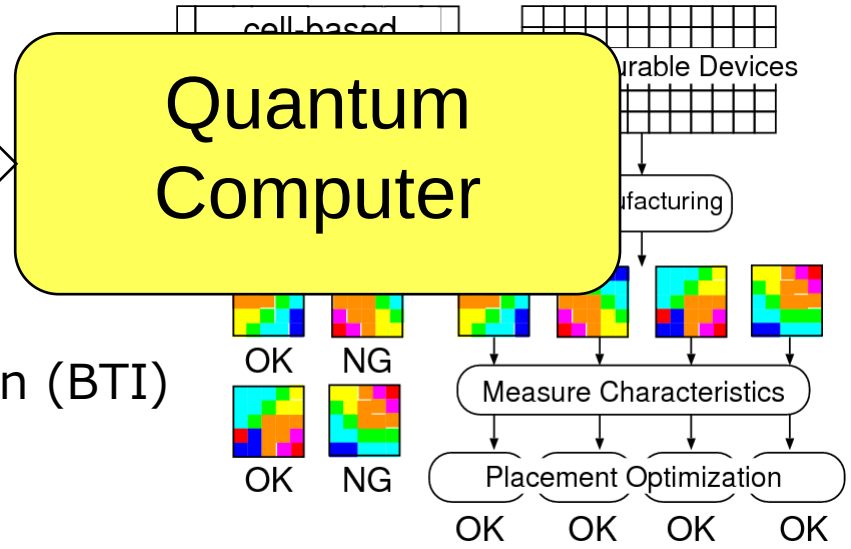
ion

radation (BTI)





FMPP (supervised by Prof. Yasuura)



Variation-aware FPGA

Our Research Group at KIT: VLSI System

http://www-vlsi.es.kit.ac.jp/

京都工芸繊維大学
KYOTO INSTITUTE OF TECHNOLOGY

- **7 faculty members: 2 full profs, 2 assoc. profs, 2 project assoc. profs and 1 project assistant prof.**

Kobayashi Takai Hiroki Shintani Tanaka Navarro Takayama

Furuta
Assoc. prof. in Okayama Pref. Univ from 2024

- ✓ Biggest group in KIT
- ✓ Prof. Takai and Shintani joined in 2022
- ✓ Prof. Tanaka, Navarro, Takayama joined in 2024
- ✓ 3 Ph.D. candidates, 30 master-course students, 14 undergraduates

Everyone Goes to Quantum Computers ^^;

- **Prof. Edoardo Charbon from EPFL**
  - ✓ His first paper on IEEE Xplore was “Single Photon Imaging in CMOS” in 2006
  - ✓ He knows Prof. Onodera (my boss in Kyoto University)

Prof. Charbon

Prof. Onodera/Yasuura

- **Dr. Kristiaan De Greve from imec**
  - ✓ His first paper on IEEE Xplore was “Fault-tolerant quantum repeaters for long-distance quantum communication based on quantum dots” in 2012

At imec

- **Prof. Tibor Grasser from TU Wien (Famous in aging degradation on a chip)**
  - ✓ He sent me an e-mail “We have entered this field a little while ago and are working on DFT calculations of SiGe spin qubits”

Prof. Grasser

Governmental Funds and Projects to Support QC

- **Q-LEAP (Quantum Leap Flagship Program) 2018-2028 https://www.q-leap.org/**
  - ✓ Deal with broad area of quantum technology including quantum computers
  - ✓ Prof. Nakamura (Riken) and Prof. Fujii (Osaka-U) are project leaders of hardware and software
- **Q-STAR (Quantum STrategic industry Alliance for Revolution) 2021 https://qstar.jp/**
  - ✓ Accelerates the shift to quantum technology through industry-government-academia collaboration
  - ✓ 17 Special member companies: KYOCERA, Canon, NEC, Hitachi, Fujitsu, Fixstar, Toyota and etc. Many corporate and start-up members
- **Moonshot Goal 6, 2020-2030 https://www.jst.go.jp/moonshot/en/program/goal6/**
  - ✓ Only focus on FTQC

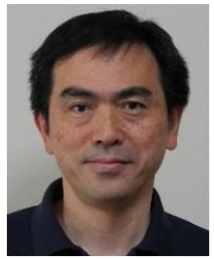
Moonshot Goal 6 "Realization of a fault-tolerant universal quantum computer that will revolutionize economy, industry, and security by 2050."

Program Director
Prof. Kitagawa
(QIQB, Osaka-U,)

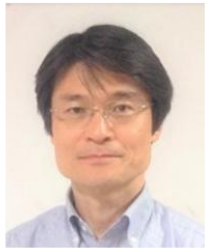
- **2020-2030**
  - ✓ Kobayashi joined in 2022
- **12 project managers (PMs)**
- **Total Budget is 30B JPY (200M USD)**

List of Project Managers

Quantum Computer Hardware

Superconducting	Trapped ion	Photon	Si MOS	Si/SiGe	Neutral atom	Neutral atom
						
Dr. YAMAMOTO Tsuyoshi	Dr. TAKAHASHI Hiroki	Dr. FURUSAWA Akira	Dr. MIZUNO Hiroyuki	Dr. TARUCHA Seigo	Dr. OHMORI Kenji	Dr. AOKI Takao
NEC Corporation	Okinawa Institute of Science and Technology	University of Tokyo	Hitachi, Ltd.	RIKEN	Institute for Molecular Science	Waseda University

Quantum Communications

NV quantum interface	Interfaces	Networking
		
Dr. KOSAKA Hideo	Dr. YAMAMOTO Takashi	Dr. NAGAYAMA Shota
Yokohama National University	Osaka University	Keio University

Quantum fault-tolerance

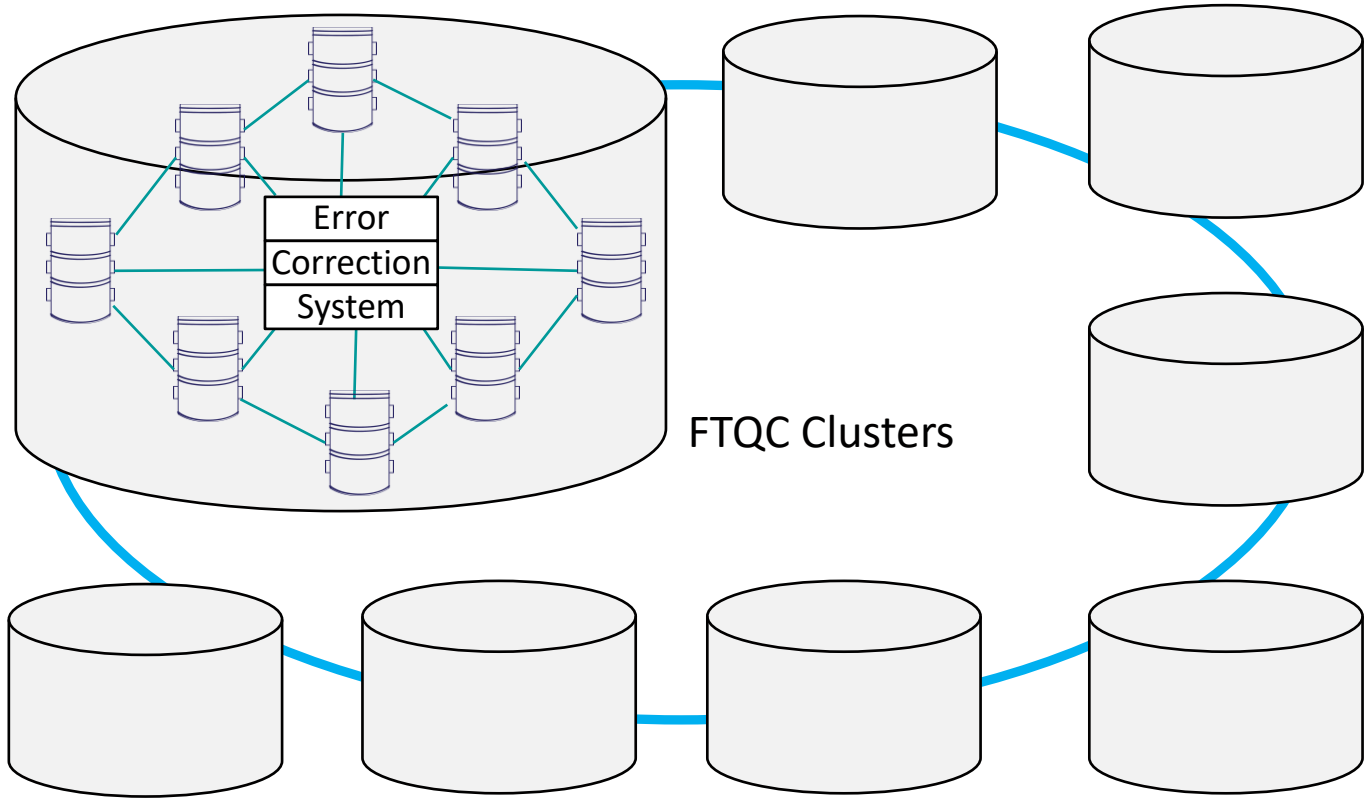
Theory / Software	QEC system
	
Dr. KOASHI Masato	Dr. KOBAYASHI Kazutoshi
University of Tokyo	Kyoto Institute of Technology

PIs of MS6: Prof. Fujii, Prof. Tanaka, Dr. Tabuchi etc..

Current & Future Quantum Computers

Quantum Computer “Ei” at Riken

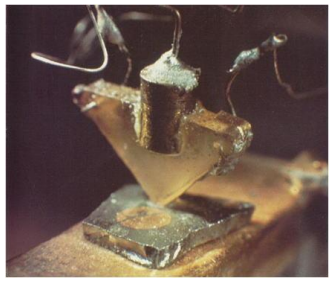
64 Qubits without error correction



Fault Tolerant Quantum Computer

> 1,000,000 Qubits with error correction

Requirement for FTQC



Ge point contact transistor in 1940's

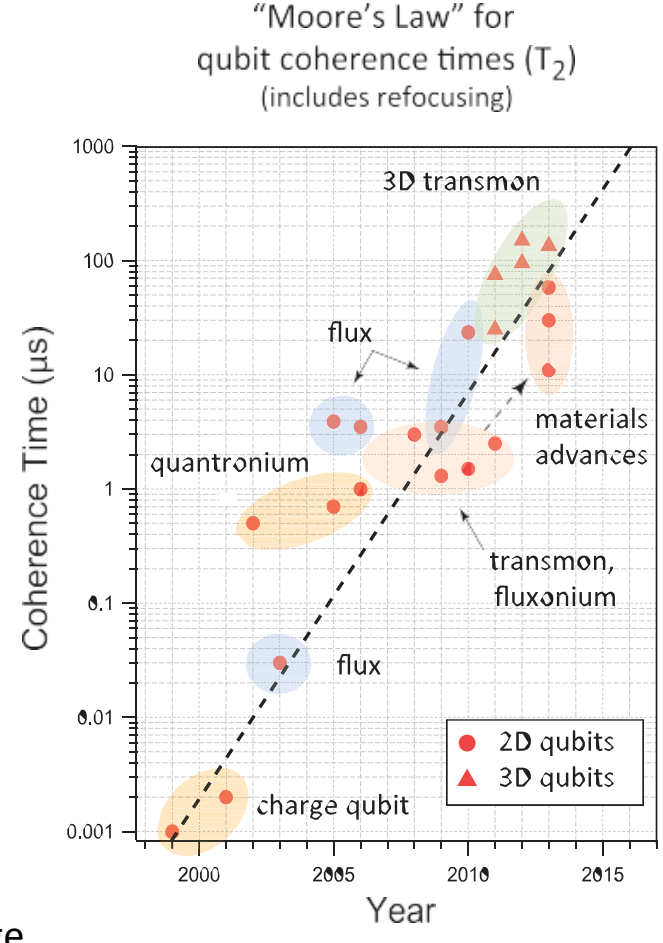
- **Fidelity (error rate) and variation of Qubit**
  - ✓ Current error rate of superconducting qubits is around > 1e-2 (1%)
    - ➢ Early FTQC with 1e4 physical qubits requires 1e-4 error rate [arXiv:2303.13181]
    - ➢ True FTQC must have less than 1e-5 error rates. Very hard barrier to establish superconducting qubit with 1e-5 error rate. We must assume 1e-4 error rate for true FTQC (by Prof. Kitagawa from Osaka U.)
    - ➢ Huge variation of qubit → fine/delicate control
    - ➢ Similar to the early days of semiconductor chips
      - ◘ Ge (GeO_2 is water-soluble) → Si (SiO_2 is dielectric)

or vacuum tube?

- **Latency and code cycle of error correction**
  - ✓ Less than 10us. 500 ns code cycle (1/1000 of T1 or T2)
- **Ultra low power operation for scalable qubit control over 1,000 qubit in a fridge**
  - ✓ 1W/1,000qubit=1mW/qubit

	Cooling Power
50K	30W
4K	1-1.5W

Cooling power of fridge.



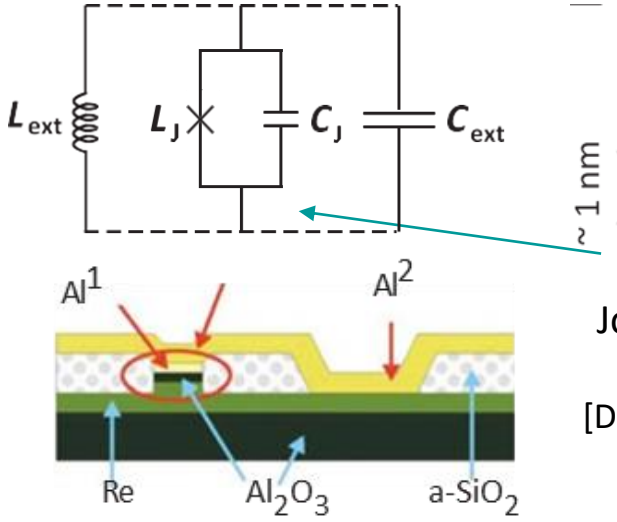
[DOI: 10.1557/mrs.2013.229]

Fidelity and Scalability of Superconducting Qubits

- Superconducting qubit is a mechanical oscillator.
  - ✓ Josephson Junction (JJ) works as a nonlinear inductive element (L_J+C_J)
  - ✓ JJ is an insulator (Al_2O_3 amorphous)
- Si can be formed as “Perfect Crystal” (Similar to Diamond)
  - ✓ Si is a gift to form semiconductor chips w/ high fidelity (<10^{-15})
  - ✓ SiO_2 has many defects to cause noise and degradations (RTN and BTI)

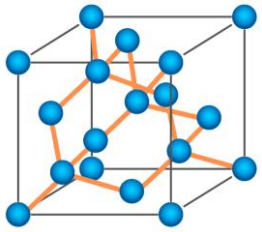
RTN and BTI are within my expertise

IRPS International Reliability Physics Symposium

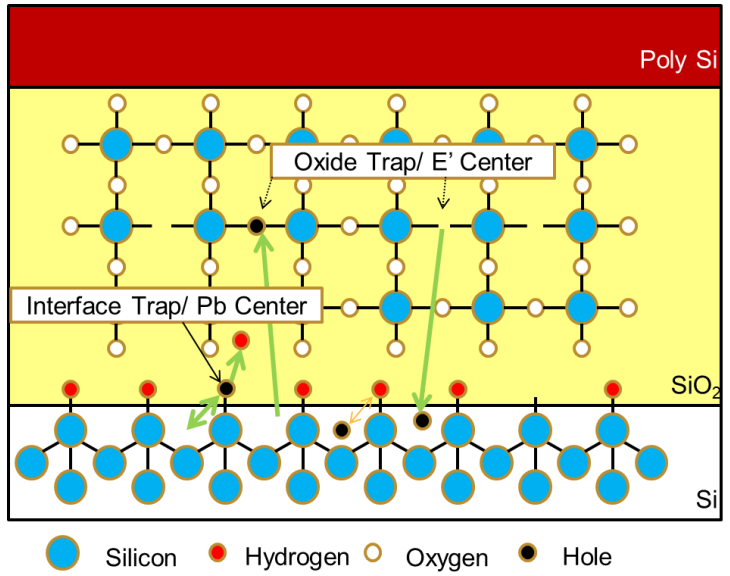


Josephson Junction (JJ)

[DOI: 10.1557/mrs.2013.229]



Si Crystal

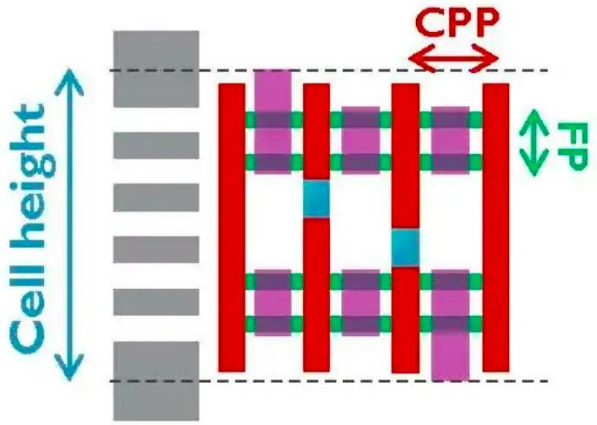


Cross section of MOS transistor

“The most widespread and robust process for fabricating JJ involves the diffusion-limited oxidation of an aluminum base layer to form a relatively uniform amorphous oxide tunnel barrier.” [M. Gurvitch et. al. , Appl. Phys. Lett. 42 , 472 (1983).]

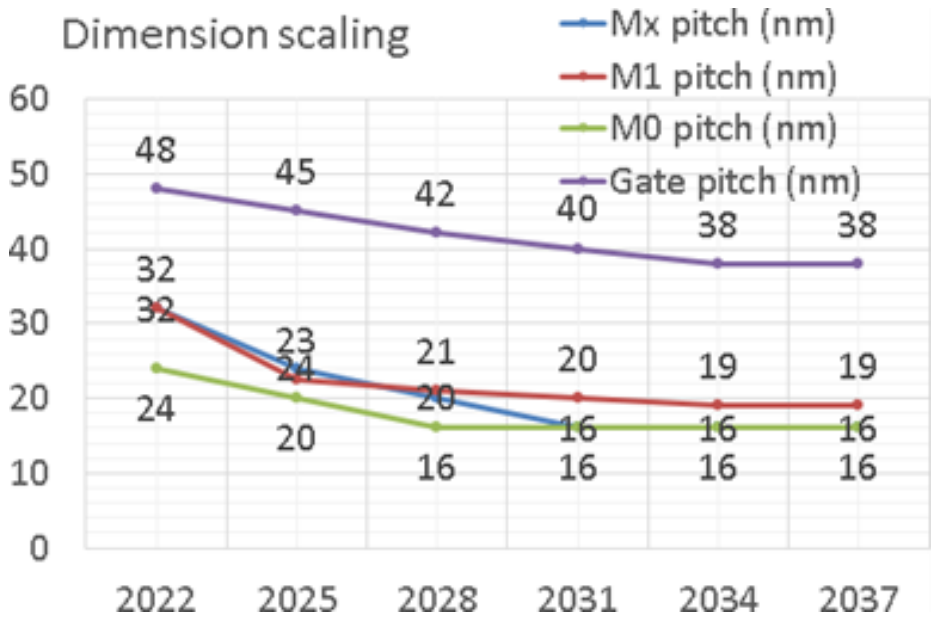
Recent Advances of Si-based Semiconductor Chips

- **“The 7nm process chip has no 7nm dimension.” by Prof. Hiramoto**
- **Wavelength of EUV (Extremely ultra-violet) exposure is 13.5 nm**
- **7nm, 5nm, 3nm are just code names**
  - ✓ Integrated density of transistors are increased to minimize cell height



Structure of a logic gate in FinFET and later: CPP (Contacted poly pitch), FP (Fin pitch)

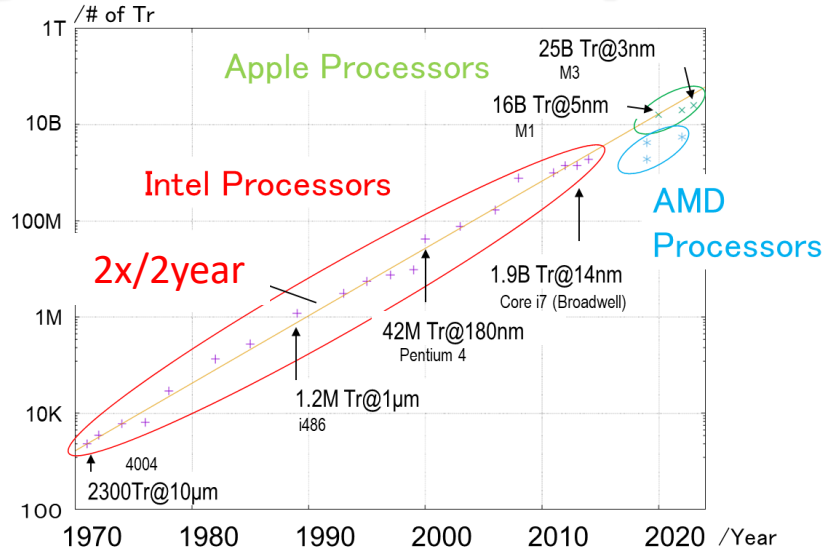
https://www.angstronomics.com/p/the-truth-of-tsmc-5nm

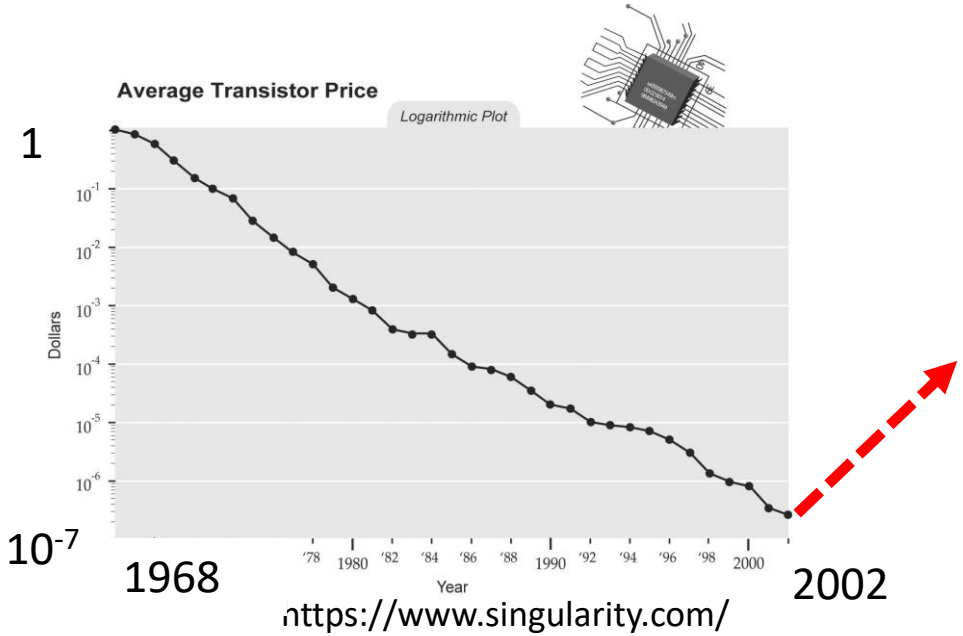


From IRDS (International roadmap for devices and systems): Gate pitch = CPP

Future of Semiconductor chips & Quantum Computers

- **Moore's Law: Gordon Moore predicted that the number of transistors on an integrated circuit will double every two years with minimal rise in cost**
  - ✓ Recent advances come from high-cost production method like "EUV" and etc.
- **Power and prices/tr are incredibly increased!**
  - ✓ iPhone 5: $199 (2012) vs iPhone 15 Plus: $899 (2023) Computer resources for AI consumes huge power
    - ➢ Neuman computers equivalent to a human brain will consume 2.4 BW (= 3 atomic power plants)
  - ✓ Rapidus (2nm fab in Hokkaido, Japan) will consume 10% electric power in Hokkaido.
- **Quantum computer may be a help for power crisis for AI and power-hungry applications**



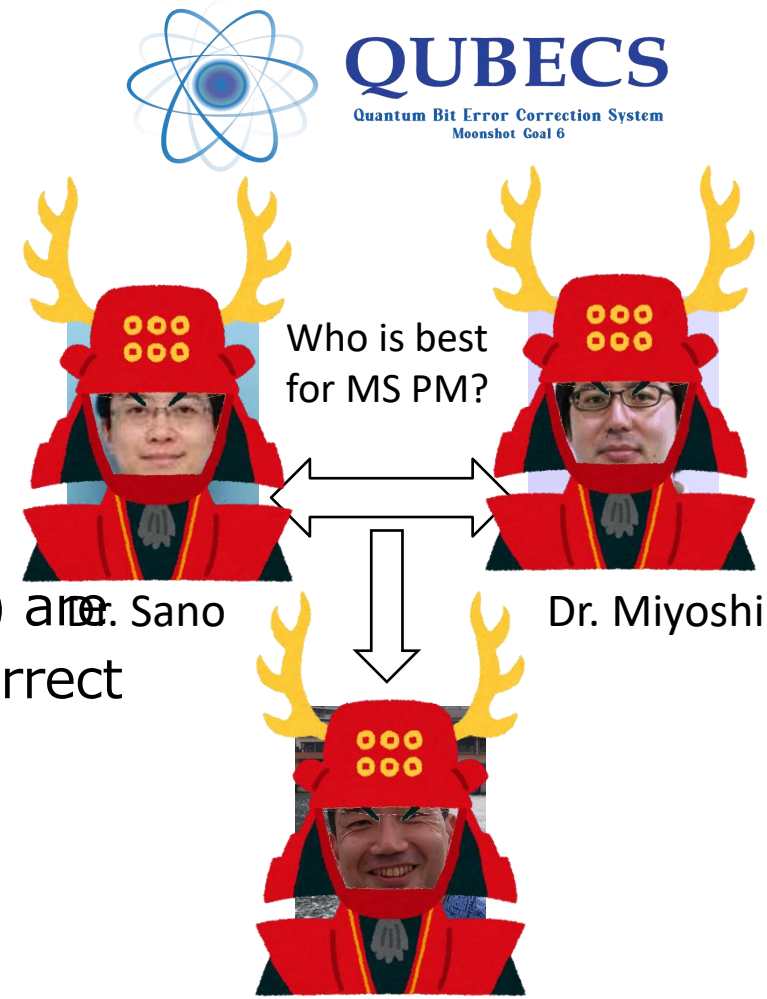


Agenda

- **Self Introduction**
- **Introduction**
  - ✓Moonshot Goal 6 for quantum computers
  - ✓Integrated circuits (Classical electronics) and quantum computers
- **QUBECS**
  - ✓Overview of my project for developing an FTQC (Fault-tolerant quantum computer)
- **Conclusion**

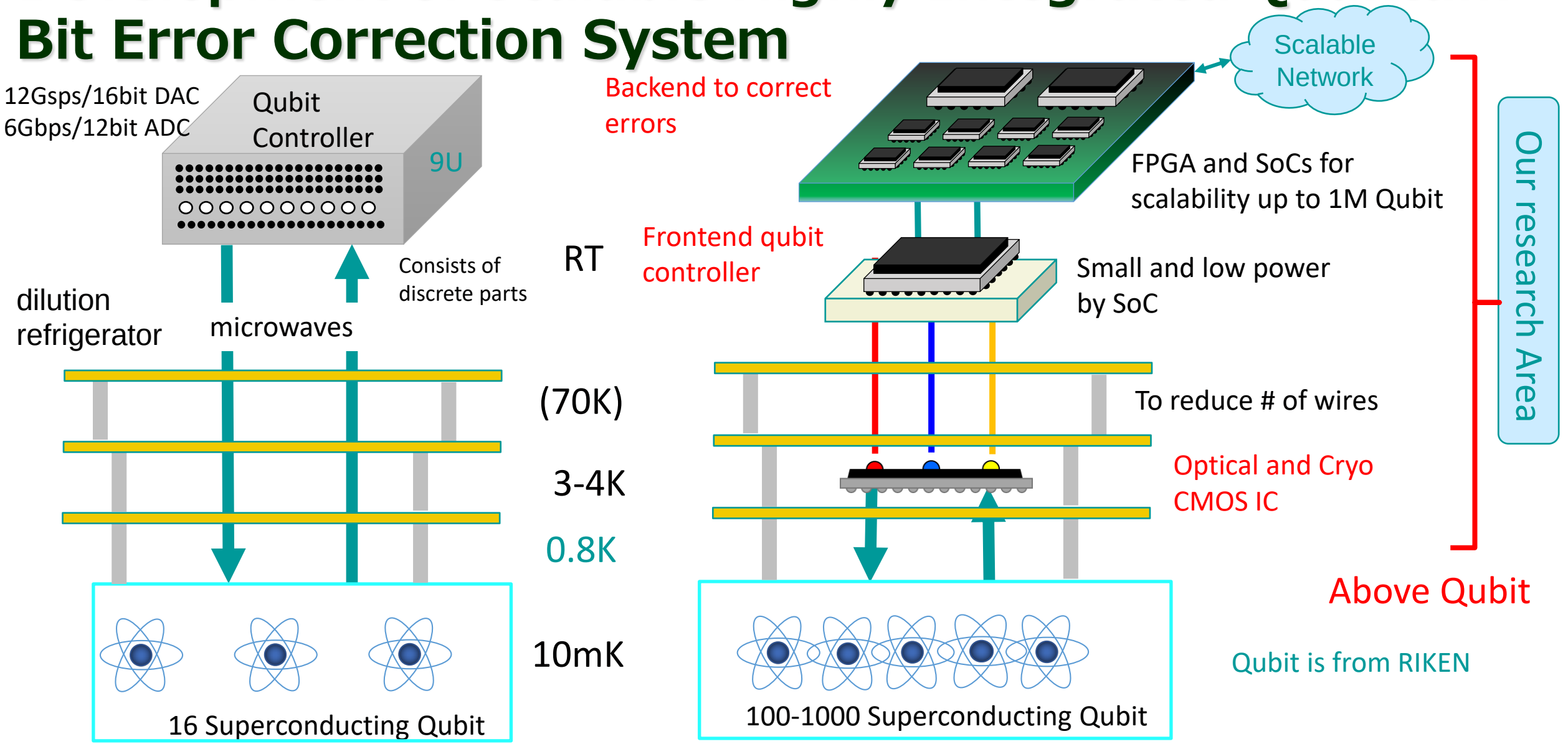
QUBECS: Quantum Bit Error Correction System

- **Acronym of my project**
  - ✓ Officially entitled “Development of Scalable Highly Integrated Quantum Bit Error Correction System”
- **To develop Fault-Tolerant Quantum Computer (FTQC)**
  - ✓ Our target is above qubits.
  - ✓ Classical electronics (integrated circuits, semiconductor chips) are going to be used to control semiconductor (+α) qubits and correct errors.
- **Two key persons**
  - ✓ Dr. Sano: Advisor of Moonshot Goal 6
  - ✓ Dr. Miyoshi: Developing qubit controllers with Riken and Osaka U.



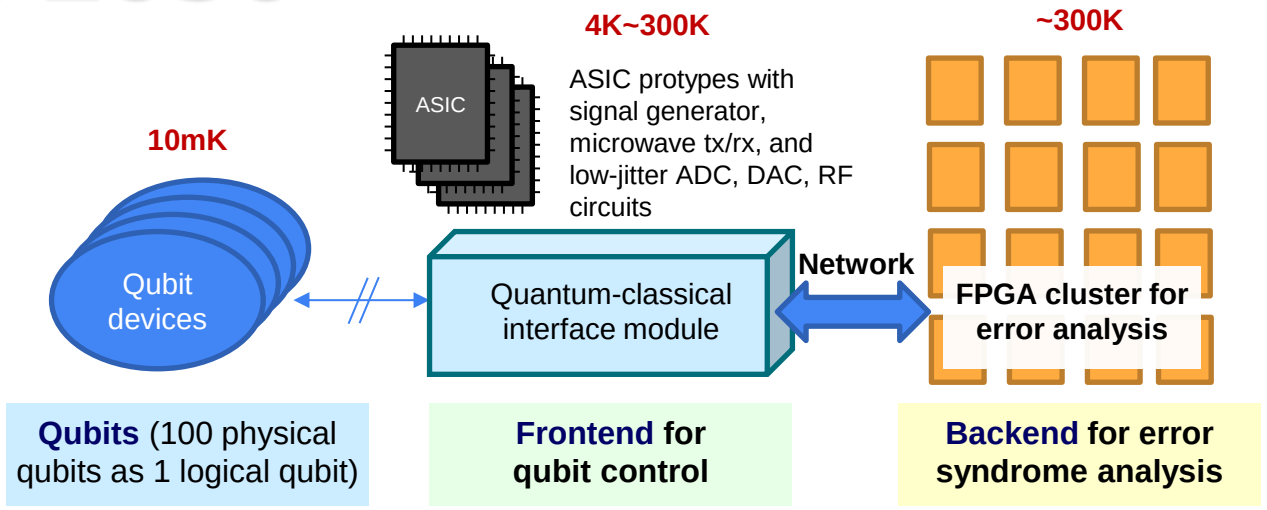
3 Samurais to realize FTQC

Development of Scalable Highly Integrated Quantum Bit Error Correction System

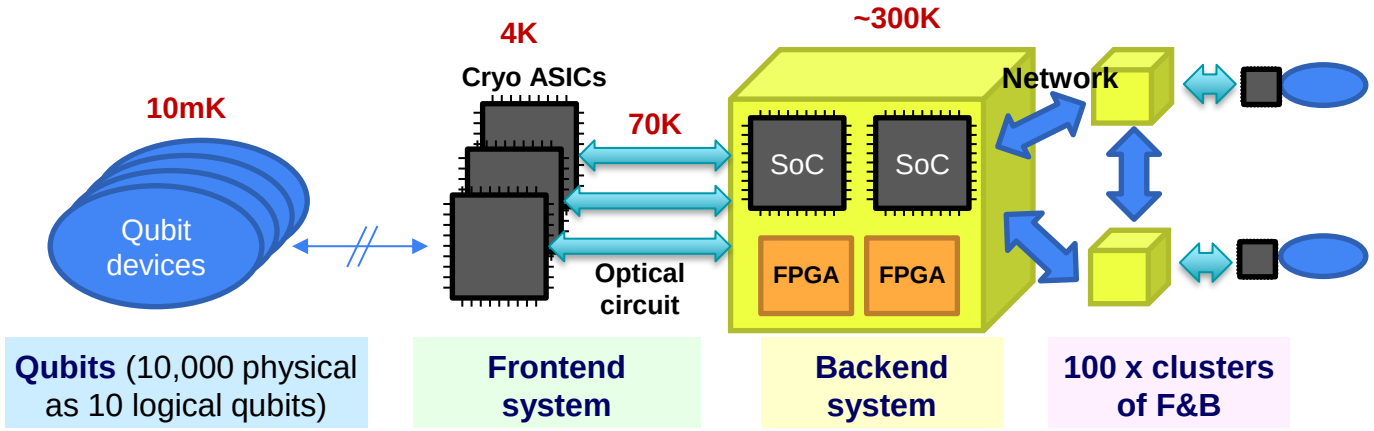


Our Goals in 2025 and 2030

- **2025**
  - ✓ Develop a prototype system for FTQC with ~100 physical qubits
- **2030**
  - ✓ Develop a system for FTQC scalable up to 1M physical qubits



2025: Prototype system for FTQC with ~100 physical qubits



2030: System for FTQC scalable up to 1,000,000 physical qubits

Principal Investigators

*: Subject Leader

Dr. Sano*
(RIKEN)

Prof. Kadomoto
(U. Tokyo)

Prof. Osana
(Kumamoto U.)

Subject 1: Backend for error correction

Dr. Miyoshi*
(Quel-inc)

Subject 2: Advanced Qubit Control Frontend

Quel-1: Qubit controller

Prof. Shiomi*
(Osaka U.)

Prof. Shintani
(KIT)

Prof. Sato
(Kyoto U.)

Subject 3: Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits

Mr. Igarashi*
(Socionext)

Subject 5: Frontend RF LSI at room temperature

Prof. Kobayashi
(KIT)

Prof. Tsuchiya
(Shiga PU)

Prof. Takai
(KIT)

Prof. Miyahara
(KEK)

Prof. Imagawa
(Meiji U)

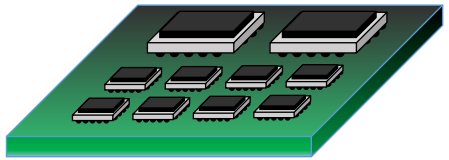
Prof. Kishida
(Toyama PU)

Subject 4: Cryo CMOS ASICs for Frontend/backend

14 PIs with 153 researchers of qubit-controllers, computer architectures and IC

Relationship among All Subjects

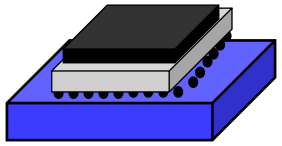
Cryogenic: extremely cold



Subject1：Backend for error correction

Sano (Riken), Osana (Kumamoto U), Kadomoto (U Tokyo)

Frontend/backend Codesign



Subject 2 ：Advanced Qubit Control Frontend

Miyoshi (Quel)

Subject 5：Frontend Analog RF LSI at Room Temperature

Igarashi (Socionext)

Specification of Frontend

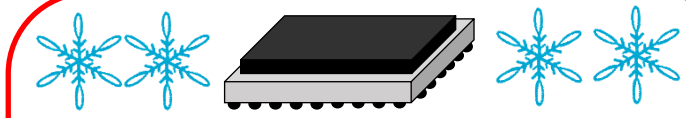
ASIC/SoC

HW Archi. and RTL

Photonic-CMOS Interface

Specification of Frontend

ASIC/SoC



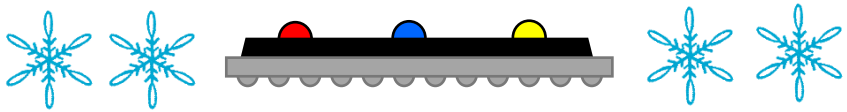
Subject 4 ：Cryo CMOS ASICs for Frontend/backend

Overview:

Kobayashi, Takai (KIT), Tsuchiya (Shiga PU), Miyahara (KEK), Imagawa(Meiji U), Kishida (Toyama PU)

Cryo PDK

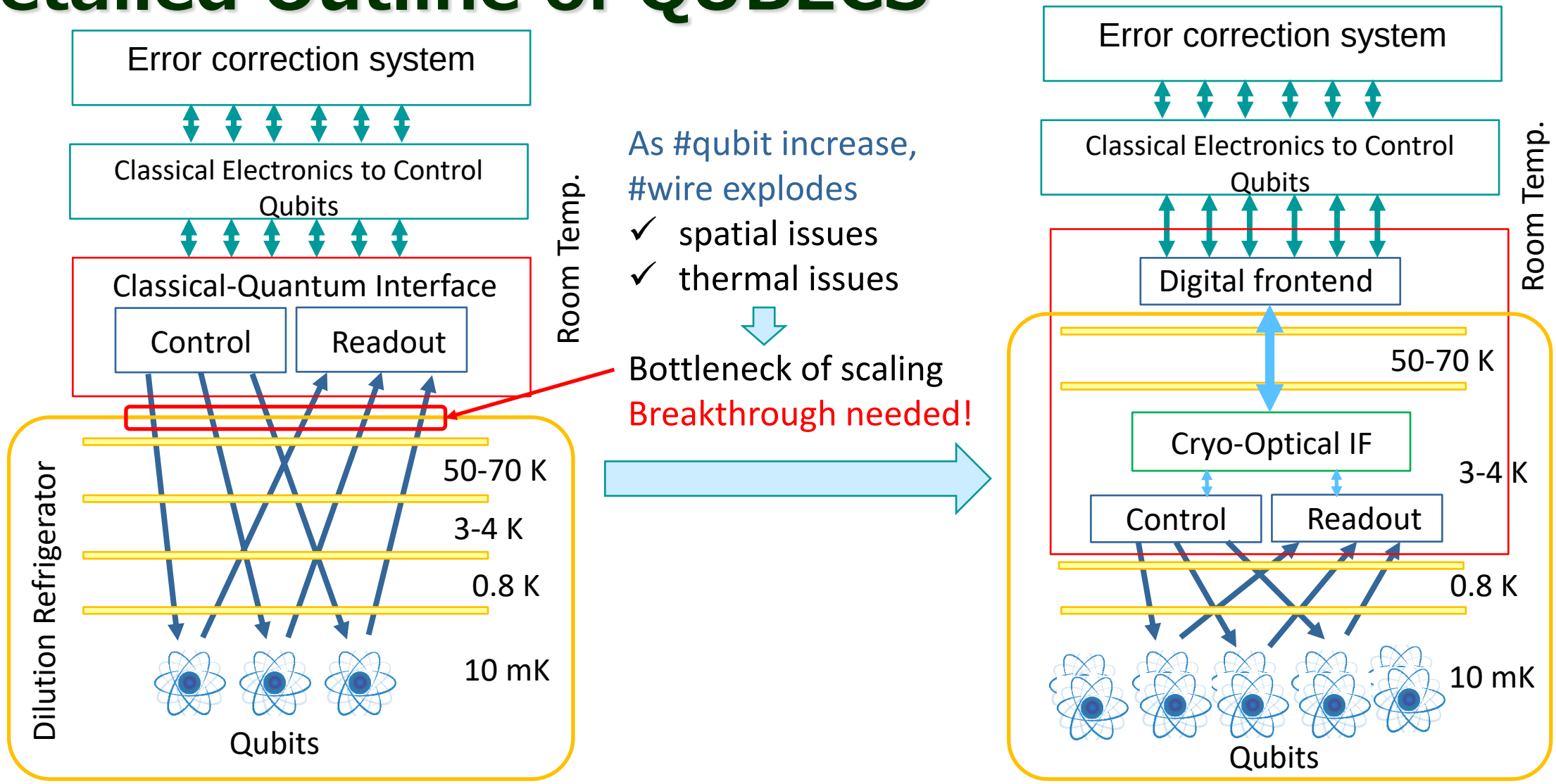
Analog/RF Frontend IP



Subject 3 ：Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits

Shiomi (Osaka U), Shintani (KIT), Sato (Kyoto U)

Detailed Outline of QUBECS

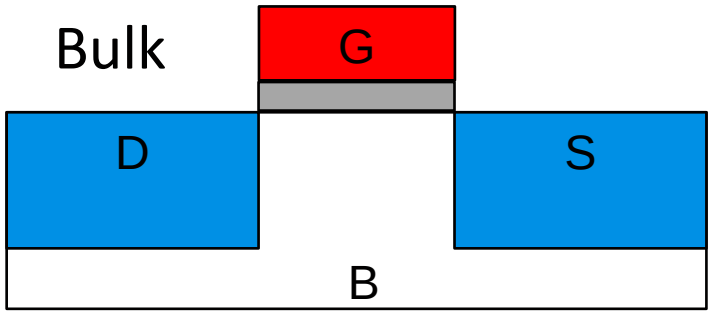


Challenges of Our Project

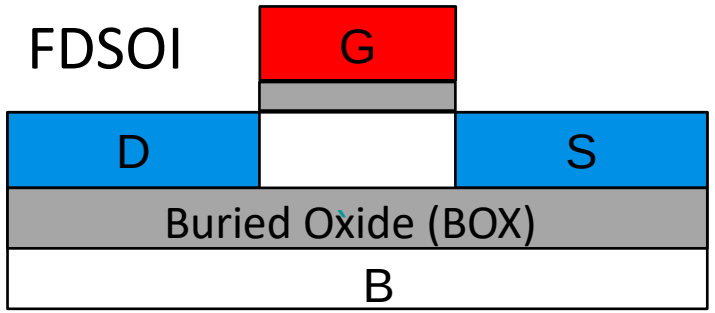
- **Subject 1 & 2: Scalable error correction system**
  - ✓ How to correct errors of millions of physical qubits
  - ✓ Low-latency network among distributed quantum error correction systems
- **Subject 2 & 5: Accurate but low-power qubit controller at room temp.**
  - ✓ Ensure accuracy for current superconducting qubit with huge variation and low fidelity
  - ✓ Low-power SoC to control qubits at room temp.
  - ✓ Universal qubit controller for any qubit
- **Subject 1 & 2 & 3 & 4: Scalable qubit control and error correction at cryo. temp.**
  - ✓ Ultra Low-power SoC to control qubits at cryo. temp. including digital/analog/RF building blocks
  - ✓ Simplified qubit control method for future stable qubits with higher fidelity
  - ✓ Optical interface between cryo. and room temp. to reduce # of wires and heat dissipation

Selection of Process Technology

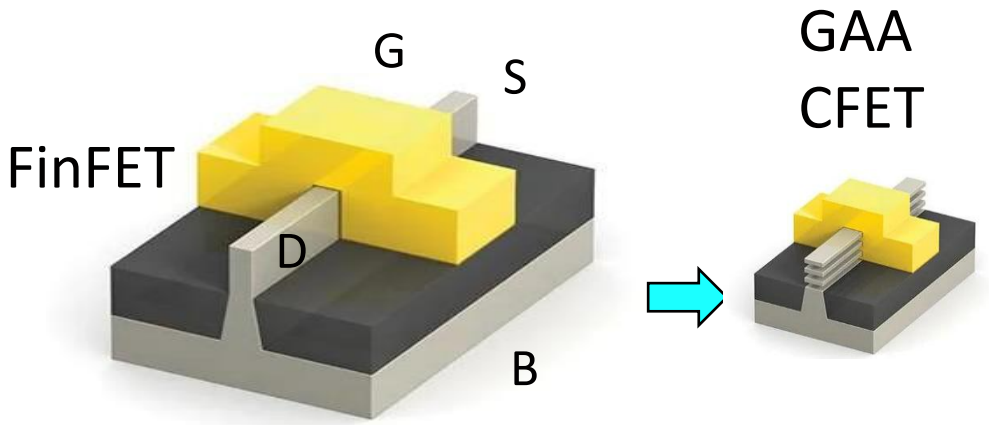
- **Subject 3 & 4 : TSMC 22nm Bulk**
  - ✓ Cheapest transistor cost
    - ➢ 7M JPY / 2mmx3mm chip (Up to 100M Tr /chip, 7 JPY/Tr)
  - ✓ Short TAT (Chip delivery after 70 days of tapeout)
  - ✓ Difficult to design
- **Subject 5: GlobalFoundries 22 nm FDSOI**
  - ✓ Lower noise and power than 22 nm bulk
  - ✓ More expensive than bulk



Cheap but leaky



Low power but expensive



High speed but very expensive

MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

QUBECS
Quantum Bit Error Correction System
Moonshot Goal 6

Subject 1: Backend for Error Correction

Theme 1: Scalable backend system for error correction by Dr. Sano

Theme 2: ASIC implementation of QEC cores by Prof. Kadomoto

Theme 3: Dependable error correction backend by Prof. Osana



Subject 1 (Backend for error correction): Goal

Goal

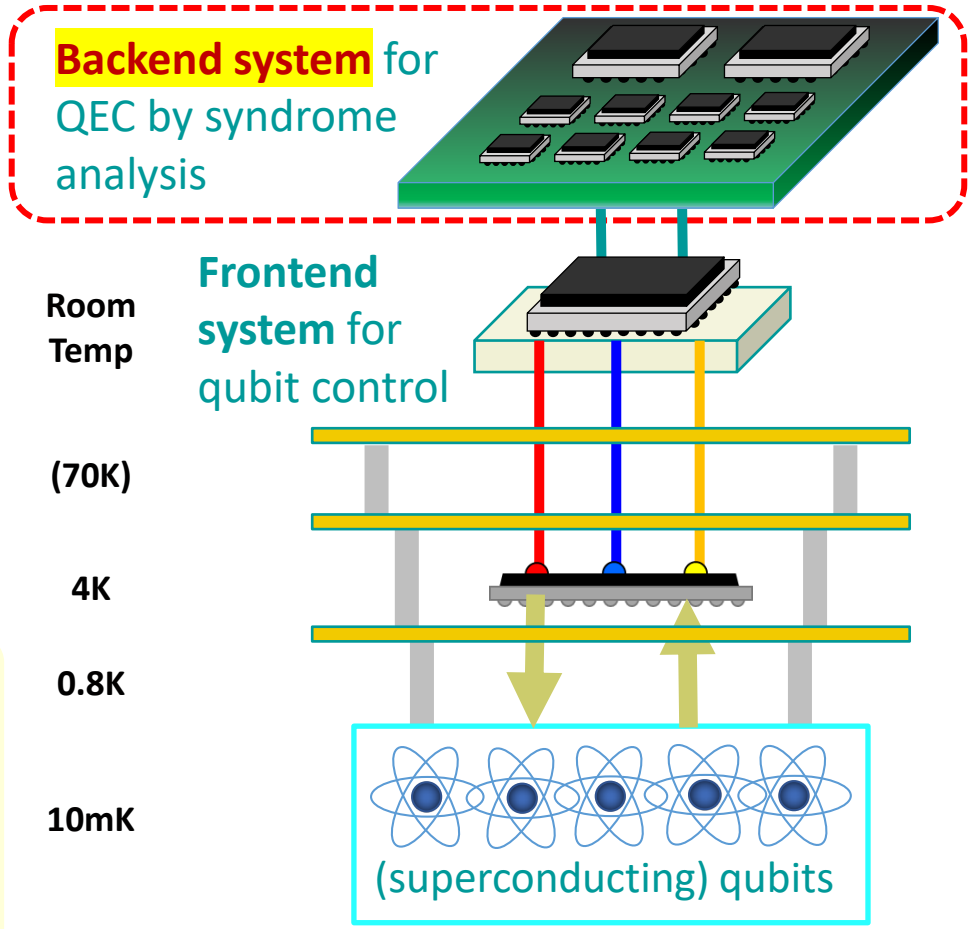
- ✓ **QEC Backend system with scalable HW algorithm**
- ✓ **Feasibility of backend system** scalable to 1000 logical qubits for their QEC and operation

Milestones

- ✓ **Develop QEC algorithm and HW design** considering performance required by frontend (latency, throughput)
- ✓ **Demonstrate QEC backend system with FPGAs** for 1 logical qubit with 100 physical qubits (d=7 ~ 11)

Organization

Theme 1	HW-oriented QEC algorithm and backend system with FPGAs	[Sano]
Theme 2	Error correction algorithm for ASIC	[Kadomoto]
Theme 3	Dependable backend for QEC	[Osana]



System organization of FTQC

Backend for Error Correction

Sano

- **Goal** **Establish QEC algorithm and its dedicated hardware design for high-throughput, low-latency, and scalable backend system**

- **Sub themes and progress**

1) Algorithm and hardware for QEC decoder

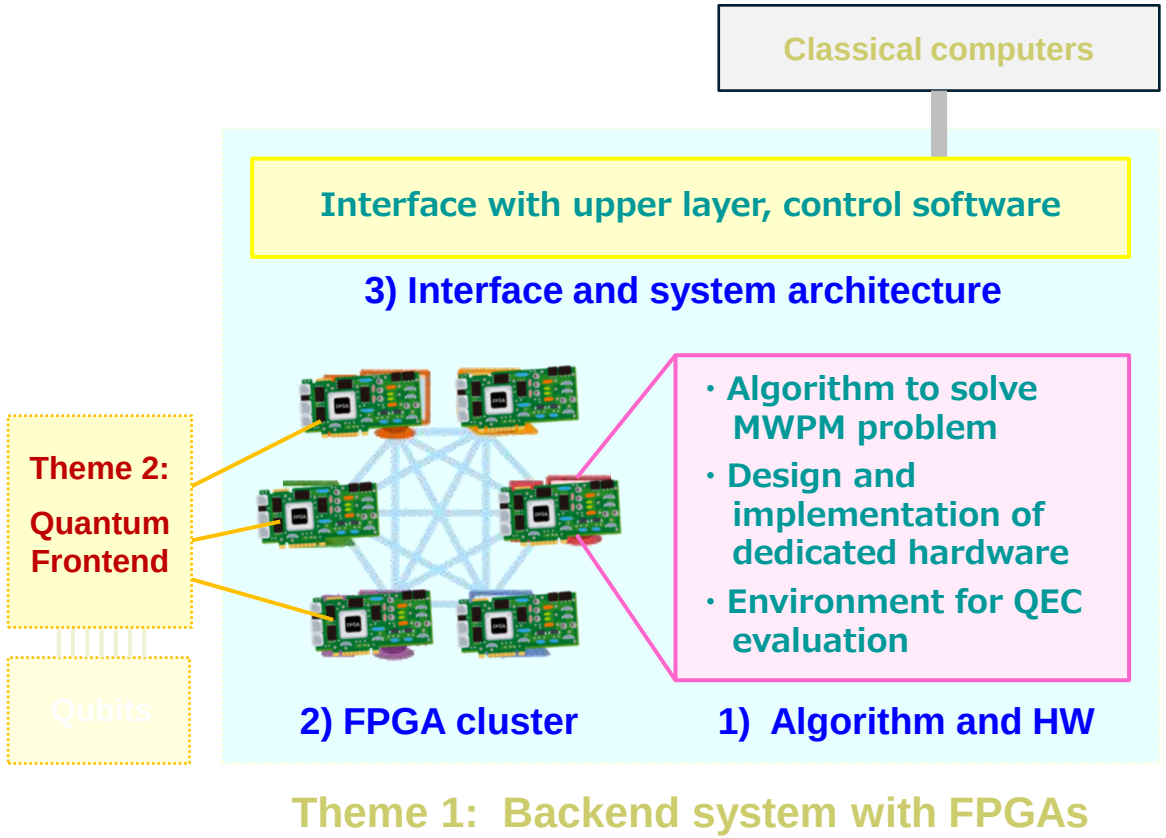
- Syndrome subgraph decoder
- Hardware design and software simulator
- FPGA prototype

2) FPGA cluster for backend system

- Requirement and specification for FPGAs
- Procurement process will start soon.

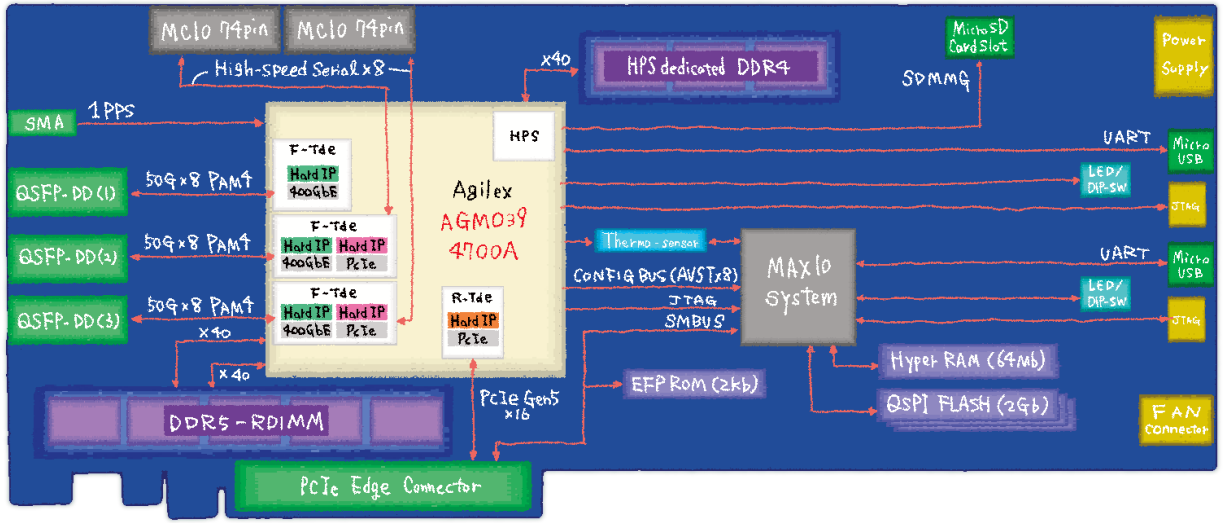
3) Interface and system architecture

- Network with frontend units (together with Theme 3)



FPGA Cluster for QEC Backend

- **Requirement and specification for FPGA**
  - ✓ High-end and large-scale FPGA, fabricated in state-of-the-art CMOS technology
  - ✓ HBM2 memory with high bandwidth
  - ✓ 400Gbps port for high-speed network
  - ✓ PCIe Gen5 x8 or 16 for fast communication with CPU
  - ✓ MCIO port for extension (e.g., ASICs)
  - ✓ OFS (Open FPGA Stack) support
- **New FPGA board will be delivered soon**
  - ✓ **A 32-FPGAs Cluster will be available**



Example of FPGA cards to satisfy the requirement

Dependable Error Correction Backend

Osana

- **Goal** **Achieve highly-reliable FPGA cluster and its interconnect for error correction backend**

- **Sub-themes and progress**

1) Ethernet-based scalable interconnect (latency: mid-high)

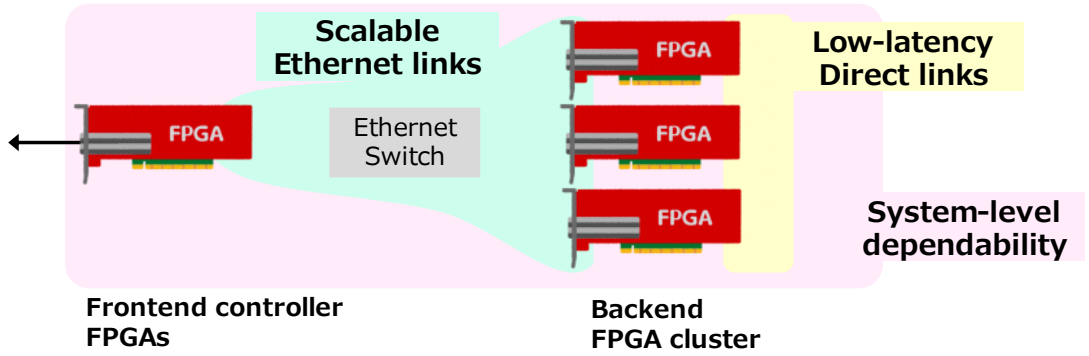
- Portable **100Gbit Ethernet** controller for the current and upcoming frontend and backend FPGAs
- Frontend emulator for operation test of backend cluster
- Dependable transport over Ethernet (similar to RoCE), with high-level flow control in progress

2) Ultra-low latency interconnect

- 100G point-to-point transport within 100ns
- 100G simultaneous multi-point interconnect implementation and proof-of-concept test in progress

3) System-level dependability

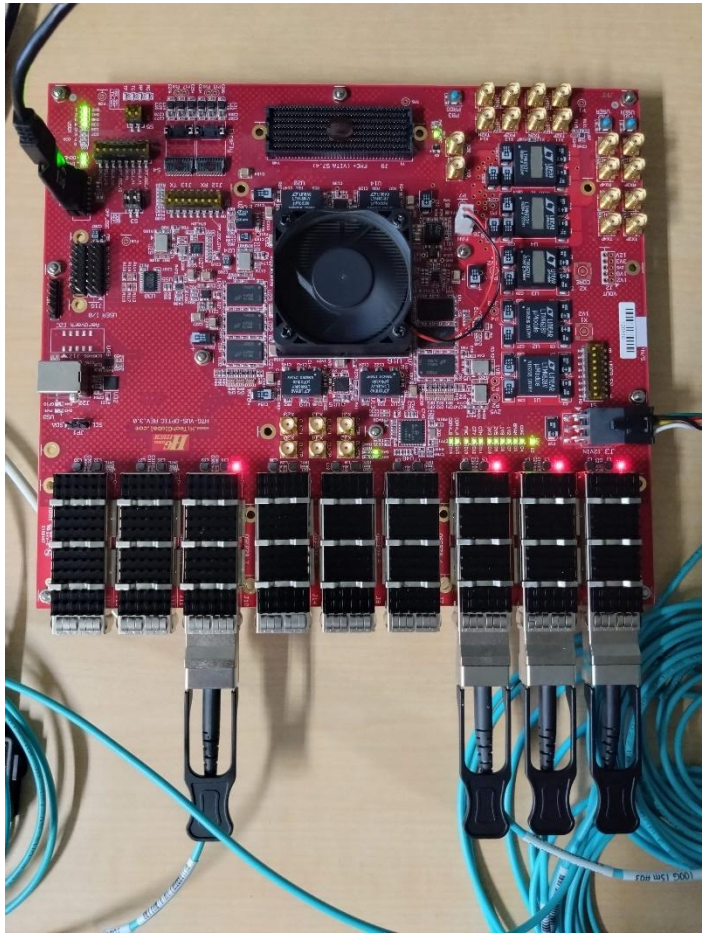
- Portable SEU mitigation framework development in progress (e.g., Correction of config registers in FPGAs)



Theme 3: Interconnect and system-level dependability

1) Ethernet-based Scalable Interconnect

- **Portable Ethernet controller for BE/FE FPGAs**
  - ✓ Implementation and basic tests are done, **will be integrated to RIKEN FPGA cluster**
- **Advanced flow control=Lossless ethernet on FPGAs**
  - ✓ Used in RoCE: RDMA over Converged Ethernet
  - ✓ Built a Linux-based RoCE test system
    - ➢ Intensive packet analysis is done
    - ➢ Working on FPGA implementation (in UDP like RoCE)
    - ➢ This **will help large-scale FPGA clusters in near future**
- **FEU emulator for QEC backend test / demo**
  - ✓ 16 FEUs for d=5, 36 FEUs for d=11
  - ✓ Emulator with 36 10GbE ports is now ready
  - ✓ Will be available in Aug

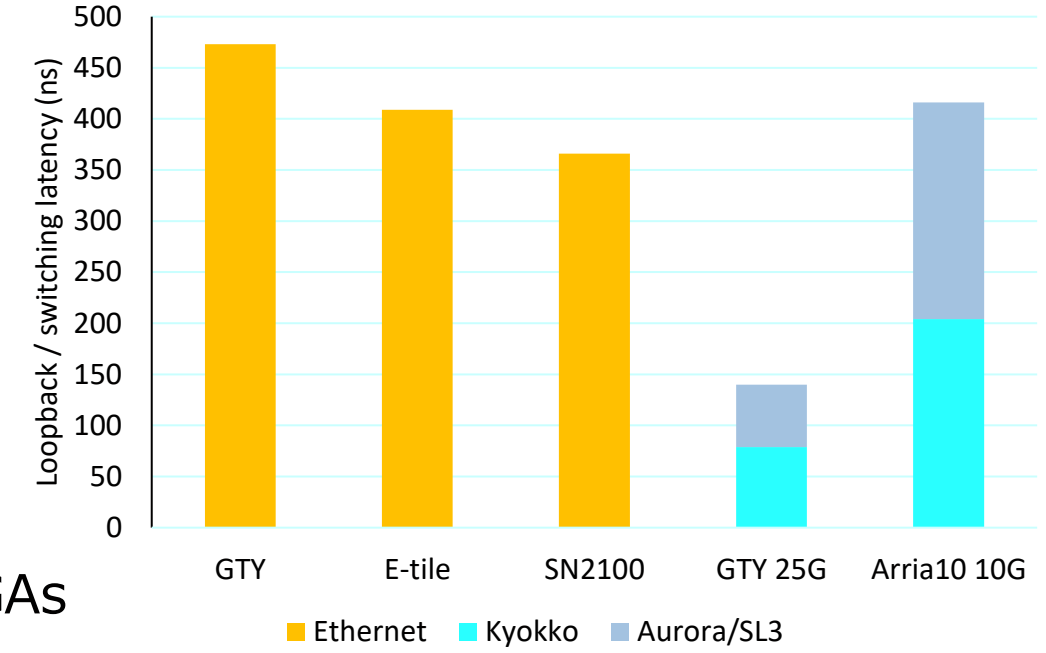


Emulate 4 FEUs per port

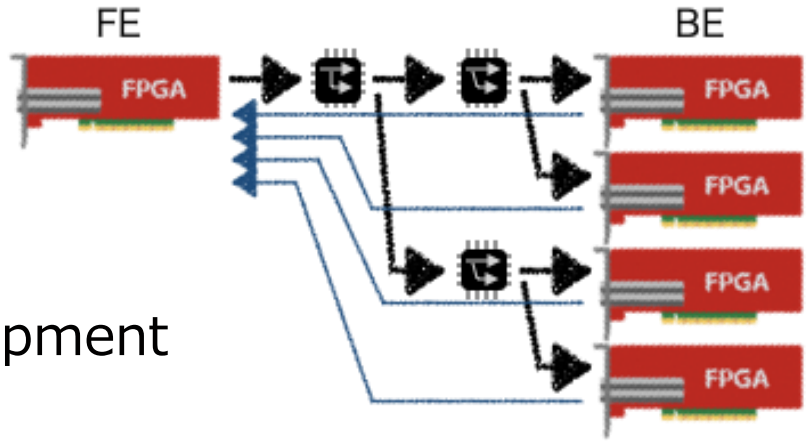
2) Ultra-Low Latency Interconnect

- **Ethernet latency is too large**
  - ✓ End-to-end latency > 1μs

- **P2P protocols are better in latency**
  - ✓ Proprietary Aurora / SL3 has latency < 400us.
  - ✓ Our Kyokko core has latency < 100us.
  - ✓ But it's point-to-point: can't connect multiple FPGAs



- **Multipoint extension**
  - ✓ Signal distributor board + extended P2P protocol
  - ✓ Enables to connect multiple FEUs + backend FPGAs
  - ✓ Distributor board for Proof-of-concept test is under development



MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

QUBECS
Quantum Bit Error Correction System
Moonshot Goal 6

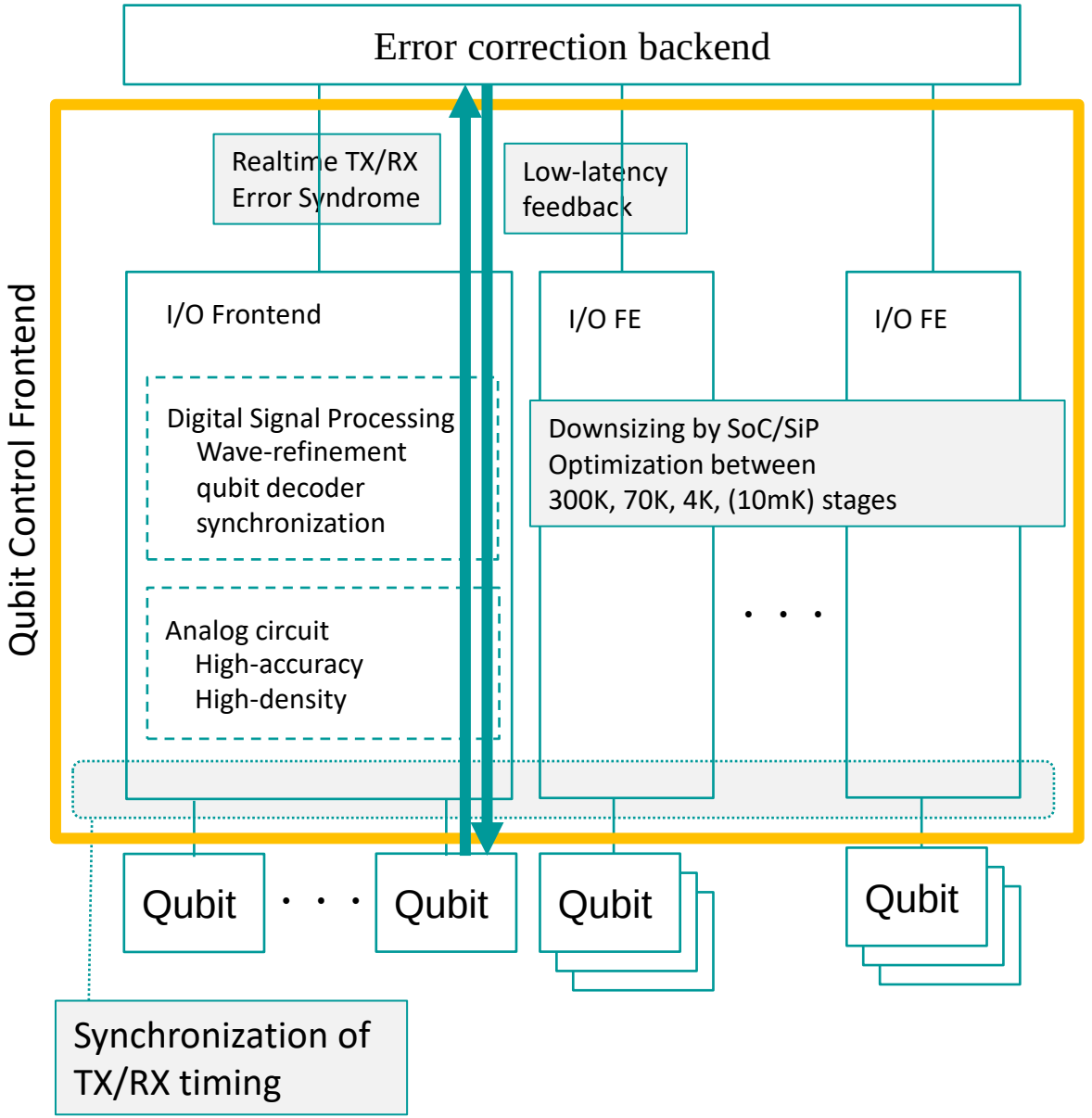
Subject 2: Advanced Qubit Control Frontend

By Dr. Miyoshi

Dr. Miyoshi*
(Quel-inc)

Subject 2: Advanced qubit control frontend

- **Goal: Establish the qubit control and measurement frontend system**
  - ✓ Realtime TX/RX qubit data b/w frontend-backend
  - ✓ Highly-accurate signal transmission
  - ✓ Synchronization for scalability
- **Issues**
  - ✓ Signal quality and stability
  - ✓ How to synchronize
  - ✓ Efficient connection with backend
    - ➢ Low-latency feedback
    - ➢ Optimized data scatter/gather
  - ✓ Downsizing (Currently 9 U/4 qubit)
  - ✓ Optimization in 300K, 70K, 3-4K, (10mK)

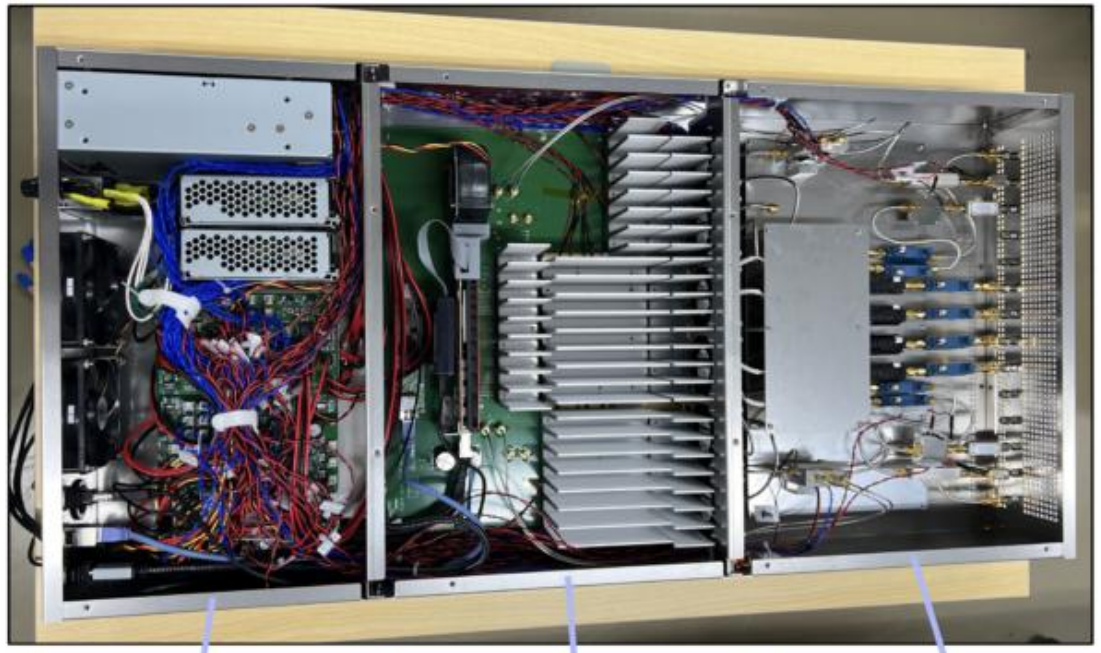


Current System

Subject 5: To integrate multiple RF components on a chip

socionext™
Celebrating A New Milestone

Transmitter	8 channels Resolution : 16 bit Sampling rate : 12 GSPS Bandwidth: 500 MHz – 2.0 GHz Frequency: 7-11 GHz (19-22 GHz with multiplier option)
Receiver	4 channels Resolution : 12 bit Sampling rate : 6 GSPS Bandwidth: 500 MHz – 2.0 GHz Frequency: 7-11 GHz



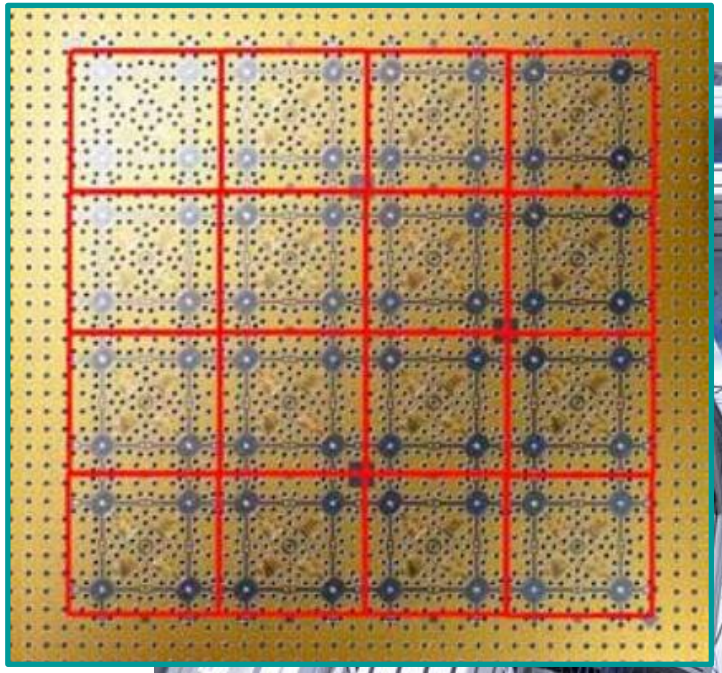
Board for DC supply and temperature control

System board
FPGA
ADC/DAC
Mixer + LO

Residual MW components
Bandpass filters
Multipliers (option)
Combiners, etc.

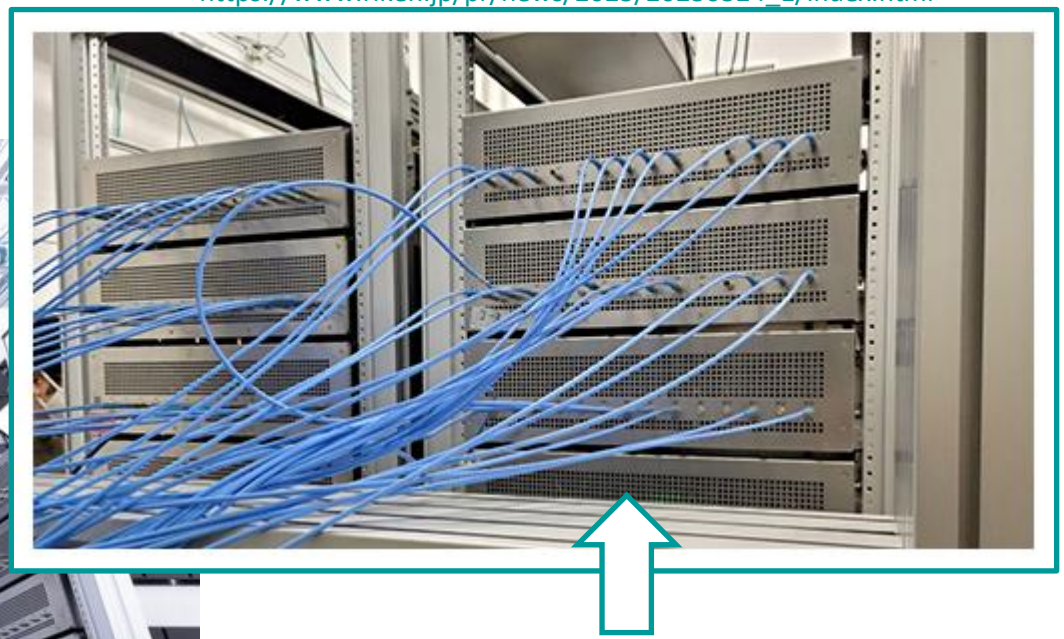
March 2023

https://www.riken.jp/medialibrary/riken/pr/videos/q_com.pdf



https://pc.watch.impress.co.jp/img/pcw/docs/1488/658/html/101_o.jpg.html

https://www.riken.jp/pr/news/2023/20230324_1/index.html



Qubit control units made by Quel

MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

QUBECS
Quantum Bit Error Correction System
Moonshot Goal 6

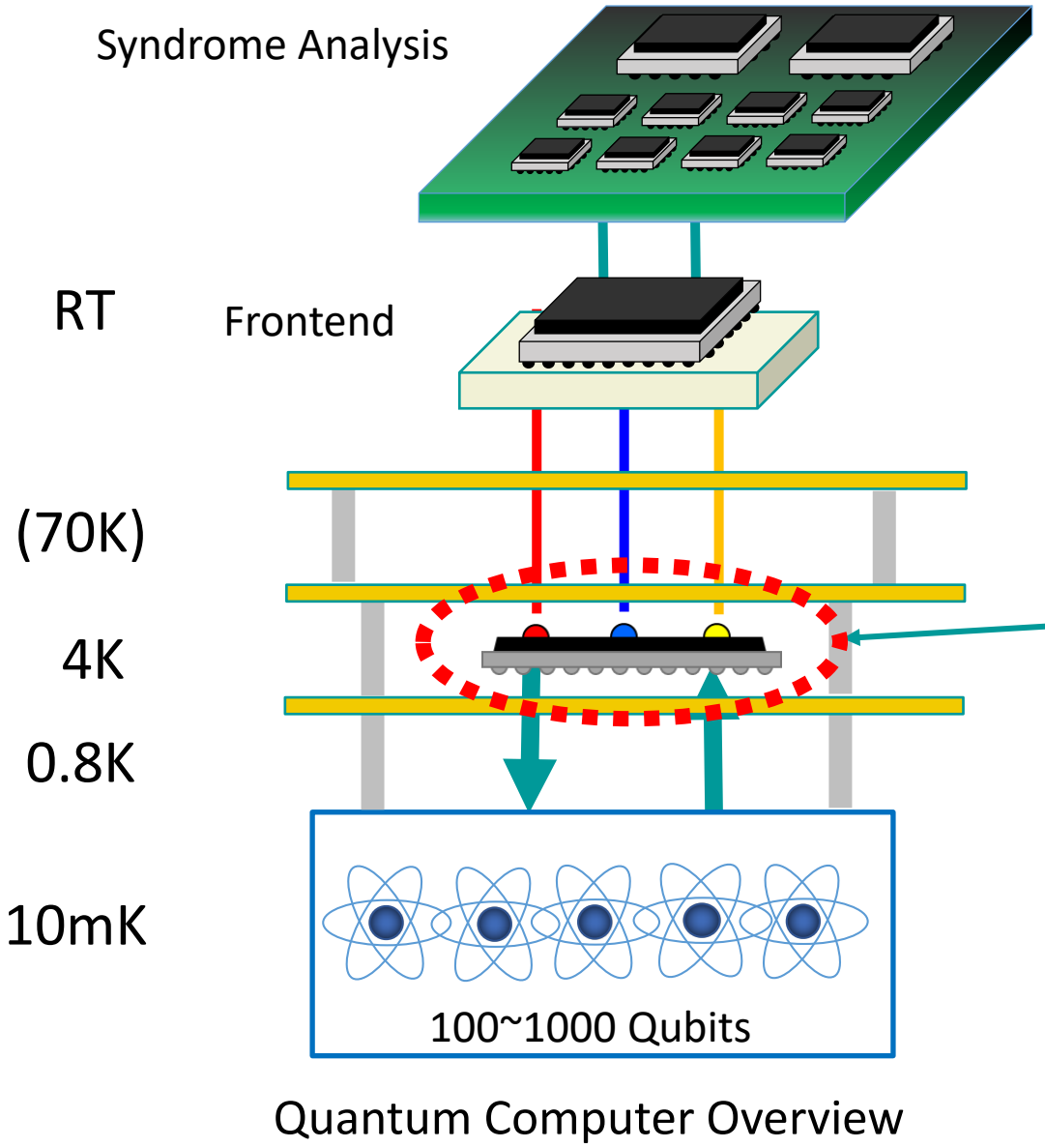
Subject 3: Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits

Theme 1: Exploring photonic integrated circuits operating in the extremely low-temperature environment by Prof. Shiomi

Theme 2: Development of transistor model for Si CMOS devices in the extremely low-temperature range of 4K to 70K by Prof. Shintani

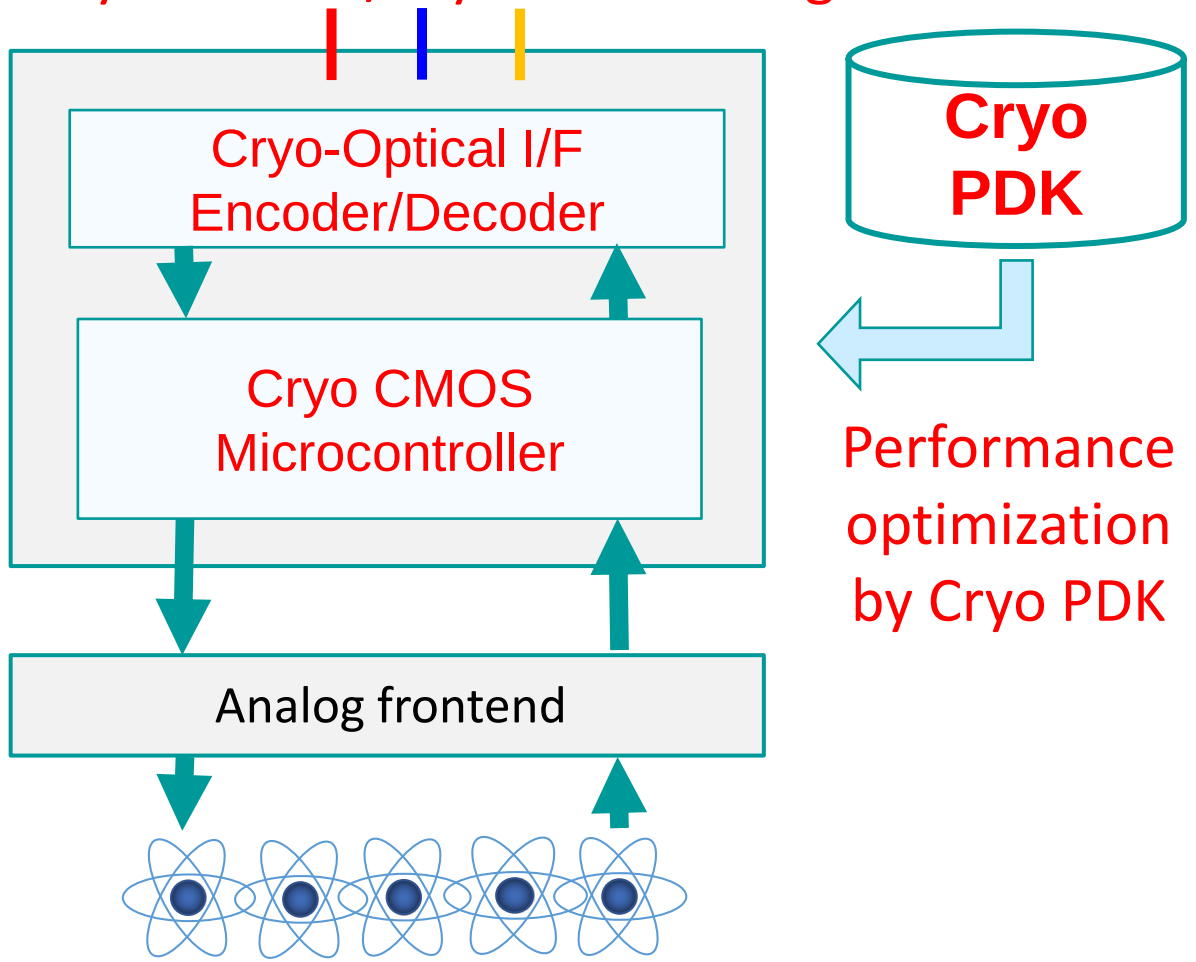
Theme 3: Cryo-CMOS integrated circuits with extremely low power consumption by Prof. Sato

Subject 3 (Scalable C-Q Interface by Ph-/Cryo-CMOS ICs): Goal



Quantum Computer Overview

✓ Scalable Classical-Quantum Interface
by Photonic/Cryo-CMOS Integrated Circuits

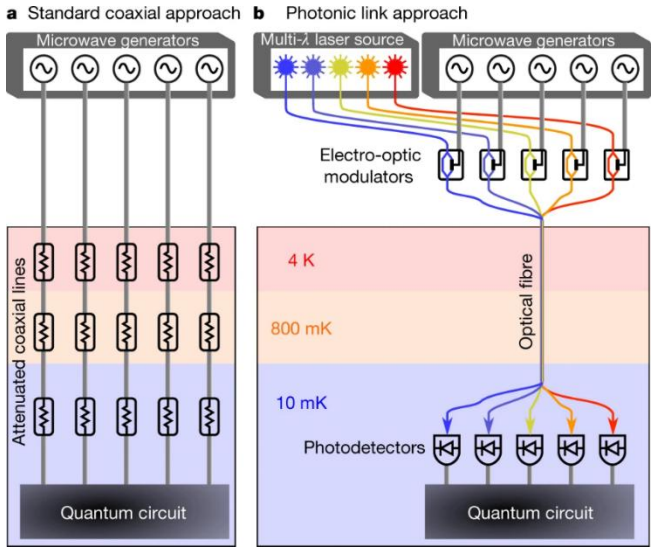


Cryogenic Photonics

Shiomi

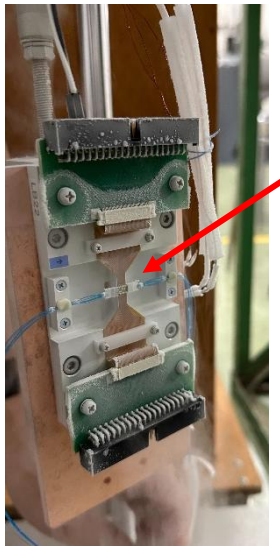
- **Cryo optical link for qubit control**
  - ✓ Operation at 10 mK region

    [1] Lecocq, F., Quinlan, F., Cicak, K. *et al.* Control and readout of a superconducting qubit using a photonic link. *Nature* **591**, 575–579 (2021)

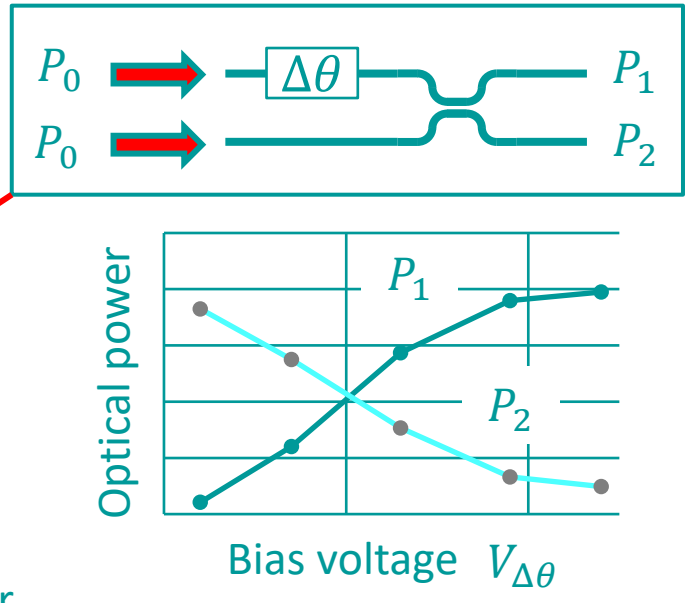


  - ✓ Optical Link for qubit controllers operating in 4 K
    - ➢ Low heat load, high speed
    - ➢ Researchers at Intel and EPFL plan to employ SiPh receivers/transmitters

- **Power consuming cryo CMOS circuits needed for scalable FTQC design**
  - ✓ Simplify CMOS controlling circuits to reduce power/area
  - ✓ Replace power consuming analog circuits with power-efficient optical devices



SiPh chip after cyro experiment



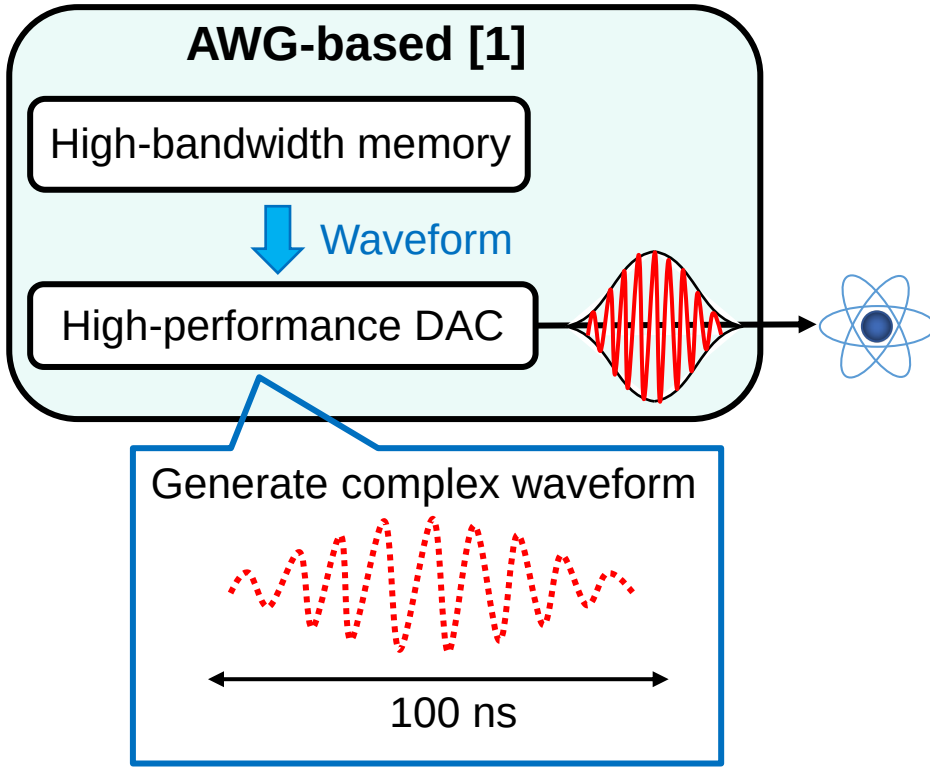
70 K operation confirmed

Circuit Cost Reduction towards Cryogenic Implementation

Issue of conventional AWG-based transmon qubit controller [1]:
•Cryo implementation is difficult due to cost of DAC and memory
➡ Propose a low-cost architecture (SPulseGen [2])

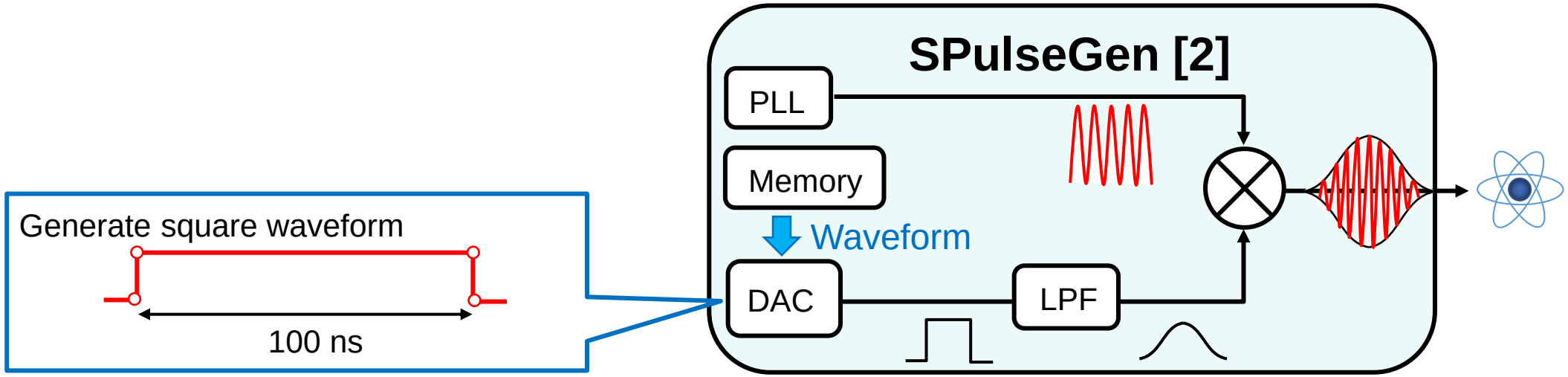
Related work of low-cost architecture [3]:
•Target qubit is fluxonium qubits
➡ Enable to utilize low-cost circuit
(Target of SPulseGen: Transmon qubits)

Fluxonium qubits:
•Advantage: Low resonant frequency and large anharmonicity
•Disadvantage: Low scalability and low connectivity



[1] D.J.Frank, et al. “A Cryo-CMOS Low-Power Semi-Autonomous Qubit State Controller in 14nm FinFET Technology,” *ISSCC*, 2022.
[2] R. Matsuo, et al. “SPulseGen: Succinct pulse generator architecture maximizing gate fidelity for superconducting quantum computers,” *arXiv*, URL: https://arxiv.org/abs/2312.08699.
[3] L. L. Guevel, et al. “A 22 nm FD SOI < 1.2 mW/active qubit AWG free cryo CMOS controller for fluxonium qubits,” *ISSCC*, 2024

Circuit Cost Reduction towards Cryogenic Implementation



◯ Circuit costs:
•DAC sampling rate
•Memory access frequency } Reduced by three orders of magnitude
➡ Reduce the power consumption and area

•Memory capacity Reduced by three orders of magnitude
➡ Increase the type of available pulses, which enables to compensate qubit variation and reduce quantum circuit depth

◯ Gate fidelity simulation:
•2-qubit gate fidelity is comparable with AWG-based architectures considering other error source in practical circuits

○ To do: Replace power consuming parts (analog circuits) with optical devices. For example, PLL output signals is generated as optical signals. The signals are then fed from the room temperature region to cryogenic region.

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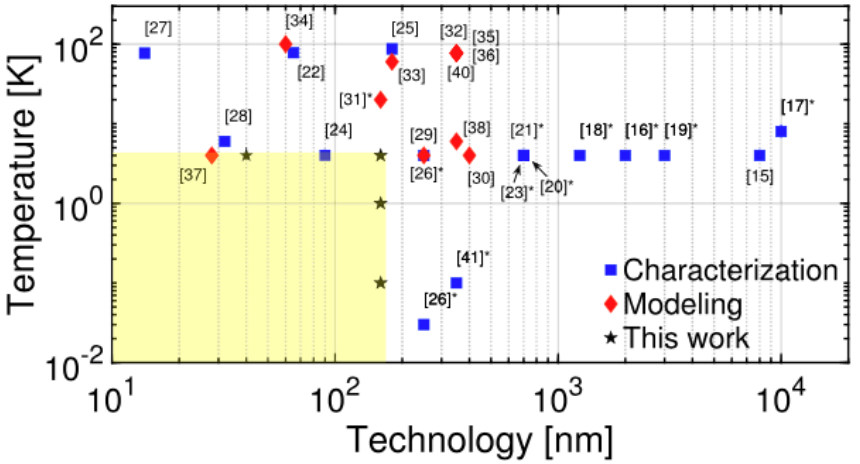
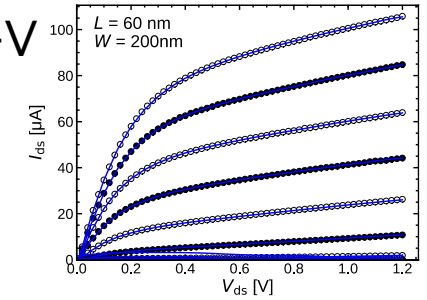
Cryogenic Compact Modeling

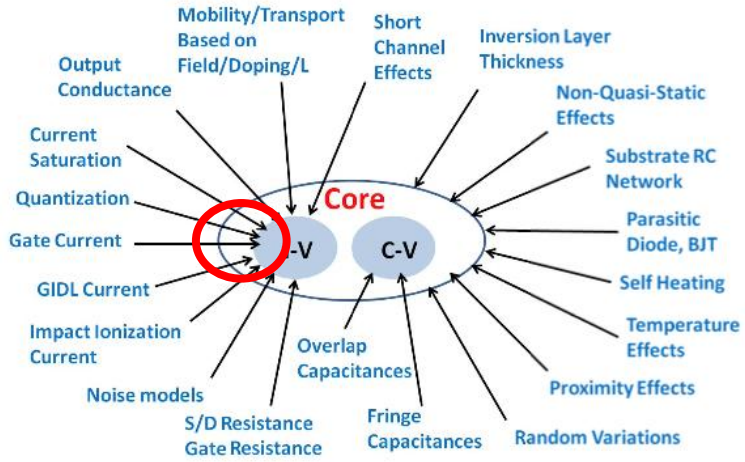
- **Tr. model from fab: -40℃ - +125℃**
- **Still under development**
  - ✓ Extremely low temperature at 4K
  - ✓ Extremely small technology node below 22 nm
  - ✓ Unknown physical mechanism
- **Focus on only drain current**
  - ✓ Esp., mobility, threshold voltage, and subthreshold slope
  - ✓ Even the core characteristic, only I-V, no C-V
- **No temperature scaling**
  - ✓ Fit to only specific temperatures, e.g., 4K
  - ✓ Assume no modulation due to self-heating
  - ✓ Most critical for Cryo-VLSI design because of limited power budget

Shintani



[IEEE J. Electron Devices Soc. 2018]

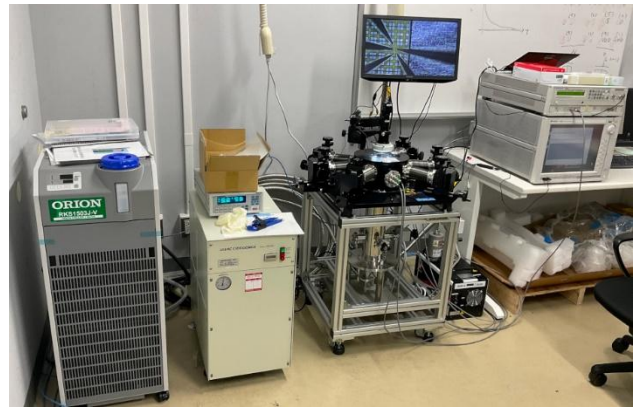




Characteristics to be considered as transistor model

Approaches

- **Our objective: Develop device-physics-based transistor model**
  - ✓ Measure and model C-V @ Cryogenic temperatures
  - ✓ Clarify and model leakage current characteristics, which is essential for power prediction
  - ✓ Develop unified model that can account for room-to-cryogenic temperatures using device-physics and machine learning
- **Current status and future prospects**
  - ✓ Characterizing and modeling via the measurement of transistor array cd TEG
  - ✓ Extending HiSIM (most physically sound model) considering cryogenic temperatures with Kioxia Corporation
    - ➢ https://www.kioxia.com/ja-jp/about/news/2024/20240517-1.html
    - ➢ https://www.kit.ac.jp/2024/05/news240517/



Cryogenic measurement system

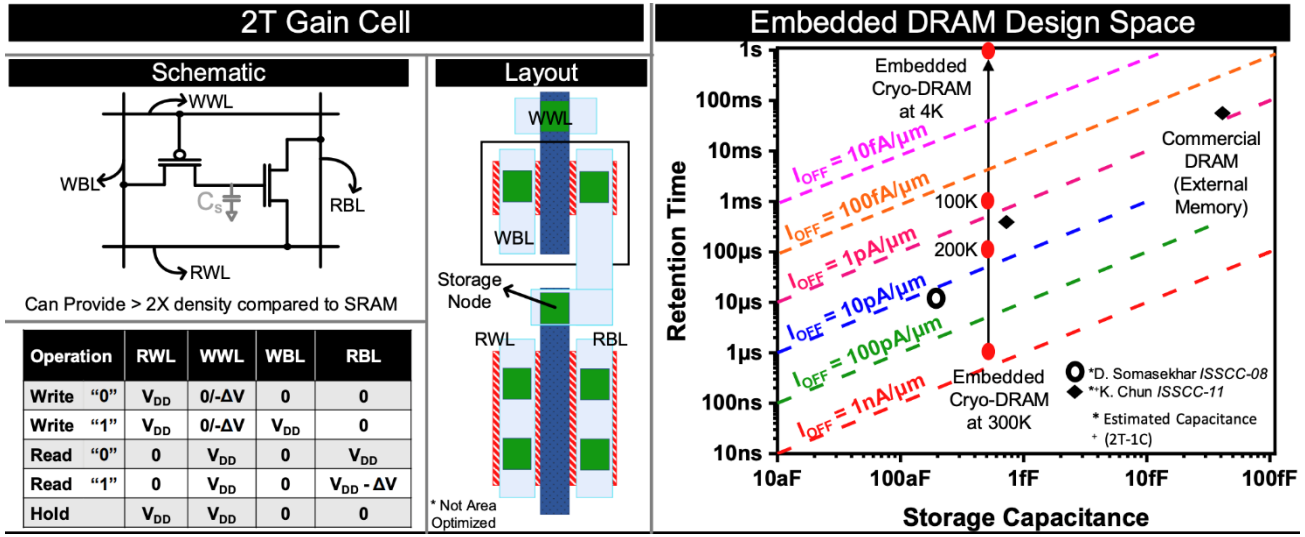
Prof. Shintani, Prof. Tanaka and Prof. Navarro

Existing work of Cryogenic Circuit Architecture

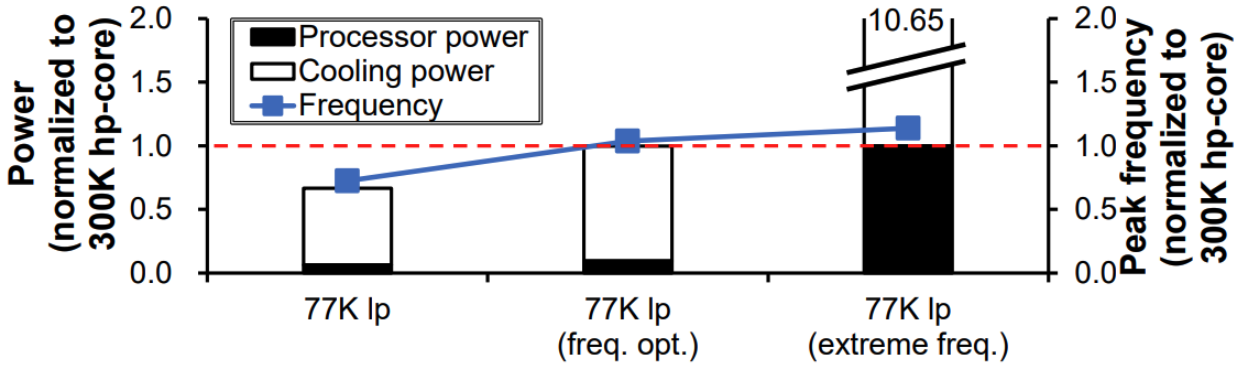
- **Memory elements**
  - ✓ 28nm 2T Gain Cell embedded Dynamic RAM (eDRAM) operated at 4K [JSSCL2021]
  - ✓ 65nm Mixed-2T Gain Cell eDRAM [TVLSI2021]
  - ✓ 40nm 4T Gain Cell eDRAM [ISCAS2023]

- **Logic gates**
  - ✓ Dynamic logic exhibit 53% power efficiency improvement compared to CMOS [TCAS2024]

- **Processor microarchitecture design**
  - ✓ CryoCore [ISCA2020]



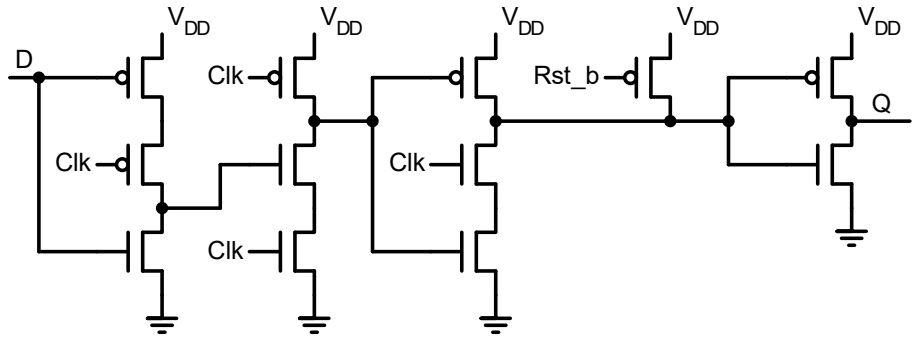
Operation	RWL	WWL	WBL	RBL
Write "0"	V_{DD}	0/-ΔV	0	0
Write "1"	V_{DD}	0/-ΔV	V_{DD}	0
Read "0"	0	V_{DD}	0	V_{DD}
Read "1"	0	V_{DD}	0	V_{DD} - ΔV
Hold	V_{DD}	V_{DD}	0	0



Dynamic Circuits at Cryogenic Temp.

Sato

- **Design methodologies at cryogenic temp. is unexplored**
  - ✓ Dynamic logic gates and microarchitectures are being studied intensively, however
    - ➢ methodology of compiling primitives to build a larger scale circuits has yet to be established
    - ➢ hardware-software co-design for cryo environment is also important
- **Our objective: design technology bridging primitives, architecture, and software**
  - ✓ modeling for primitive circuits
  - ✓ P&R that minimizes dynamic power
  - ✓ processor-middleware considering cryo. operation



Dynamic DFF w/o clkb

- **Current status and future prospects**
  - ✓ characterization and modeling via the design and measurement of primitive circuits
  - ✓ in plan: cryo-oriented P&R and compiler

MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

QUBECS
Quantum Bit Error Correction System
Moonshot Goal 6

Subject 4: Cryo CMOS ASICs for Frontend/backend



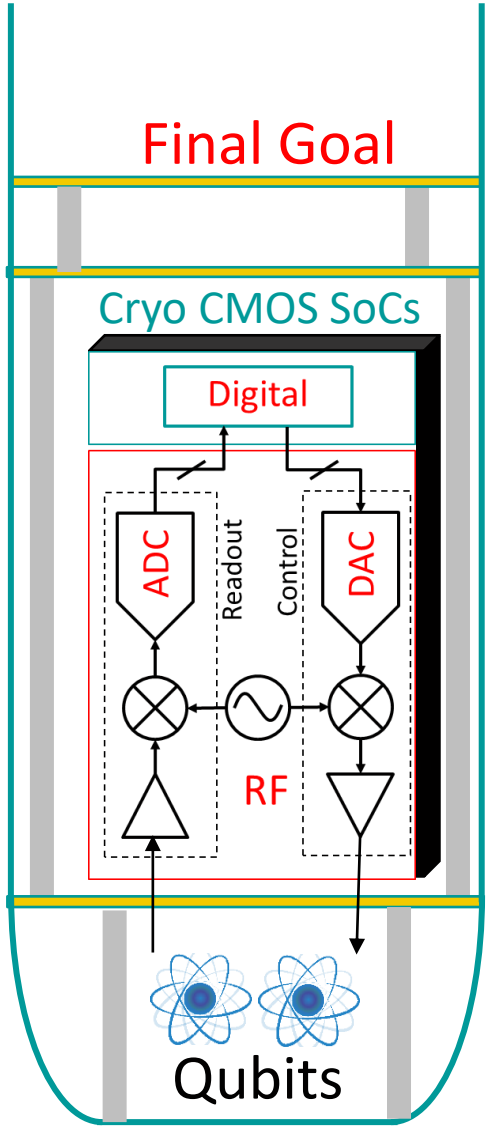



Theme 1: Digital circuit implementation and reliability enhancement techniques by Prof. Kobayashi
Theme 2: RF frontend circuit by Prof. Tsuchiya
Theme 3: High-speed DAC for frontend by Prof. Takai
Theme 4:High speed ADC for frontend by Prof. Miyahara
Theme 5: RTL design of digital circuits for frontend by Prof. Imagawa
Theme 6: Layout design of digital circuits for frontend by Prof. Kishida

Subject 4: Cryo CMOS ASICs for Frontend/backend

- **Goal: To implement ASICs operating at a cryogenic temperature to control qubits (Frontend) and to correct errors (Backend)**

- **Research items**
  - ✓ Digital circuit implementation and reliability enhancement techniques (Prof. Kobayashi, Prof. Kishida, Prof. Imagawa)
  - ✓ RF frontend circuit (Prof. Tsuchiya)
  - ✓ High-speed DAC for frontend (Prof. Takai)
  - ✓ High speed ADC for front end (Prof. Miyahara)



Research Trend: RF frontend

Around 2020:

Full-integration was reported 2021 [Intel/TU Delft, ISSCC2021][Google, ISSCC2023]
Basic architecture and challenges [Google, IEEE J. Microwaves 2021]

Cooling capacity of fridge (4 K stage): 1 - 2 W
Target: 1 mW/qubit for 1,000 qubits

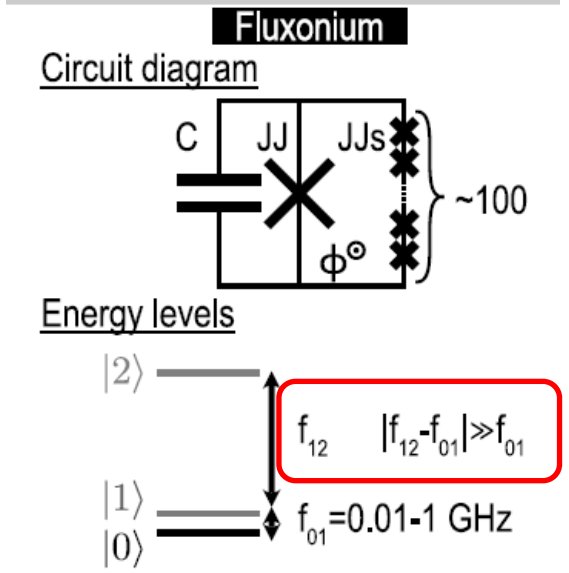
Improved architectures

Phase-shifter base [Tshinghua U., ISSCC2024] 10 mW/qubit
Memory-less AWG [POSTECH, ISSCC2023] 10 mW/qubit

With new qubits, qubit-specific RF font-end architecture

AWG-less with fluxonium qubit [Google, ISSCC2024] 1.2 mW/qubit

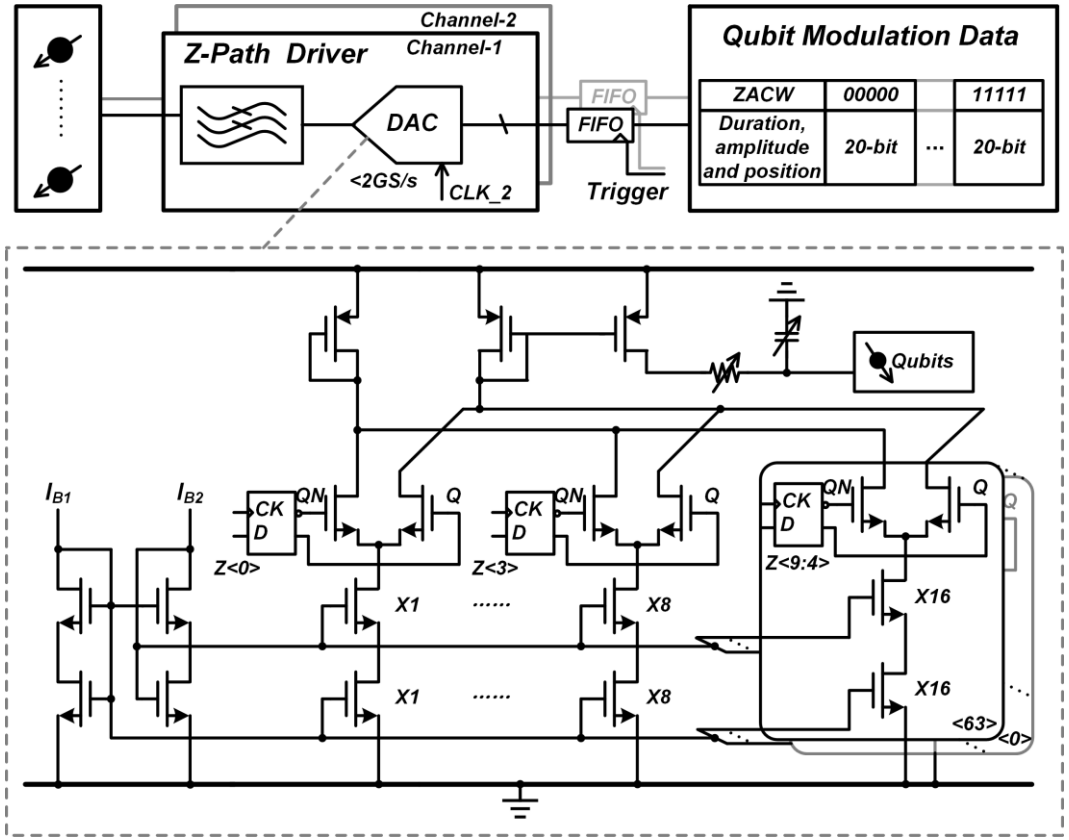
frontend architecture development considering qubit is needed



Tolerant against error
➔ simplified RF pulse
(Fig. [Google, ISSCC2024])

Cryo DAC Research Trends

- Current steering DACs are the mainstream (RF)
- Unit current is designed to be small (650 nA) and output current is amplified by current mirror to control Qubit. (Ex. 10bit 650nA×1024 = 665.6μA)



- 10-bit resolution for RF applications, 14 to 20 bits for bias control
- Mostly used at 1GS/s to 2.5GS/s for RF applications.

Y. Guo et. al," A Polar-Modulation-Based Cryogenic Transmon Qubit State Controller in 28 nm Bulk CMOS for Superconducting Quantum Computing," IEEE J-SCC, VOL. 58, NO. 11, NOV. 2023

Specifications		This work	ISSCC'22 [23]	ISSCC'21 [19]	ISSCC'20 [18]	ISSCC'23 [22]	ISSCC'22 [21]	ISSCC'23 [17]	ISSCC'19 [16]
Operating Temperature		3.5K	3K	4K	3K	3.5K	3.5K	3K	3K
Qubit Platform		Transmon	Transmons	Spin Qubits	Transmons & Spin Qubits	Transmon	Transmon	Transmon	Transmon
Technology		28nm Bulk CMOS	14nm FinFET CCMOS	22nm FinFET CMOS	22nm FinFET CMOS	40nm Bulk CMOS	40nm Bulk CMOS	28nm Bulk CMOS	28nm Bulk CMOS
Architecture		**Polar**	I/Q SSB	I/Q SSB	I/Q SSB	I/Q SSB	I/Q SSB	I/Q Direct Conversion	I/Q Direct Conversion
RF Freq. Range		4-6GHz	4.5-5.5GHz	11-17GHz	2-20GHz	5-6.5GHz & 7-8GHz	4.5-8GHz	4-8GHz	4-8GHz
DAC/DPA Speed		Up to 2GS/s	1GS/s	Up to 2.5GS/s	1GS/s	Up to 2GS/s	Up to 2GS/s	1GS/s	1GS/s
DAC/DPA Resolution		10bits	10bits	10bits	10bits	10bits	10bits	10bits	N/A
SNR/SFDR		>40dB	[g]~49dB	N/A	45dB	[g]~45dB	[g]~42dB	N/A	N/A
Data Bandwidth		N/A	N/A	Up to 2GHz	1GHz	N/A	N/A	N/A	N/A
Output Power		>-15dBm	-16dBm	-10dBm	-17.5dBm	-20dBm	-17dBm	N/A	N/A
On-chip LO Generation		**Yes, IL-LO**	No, Off-chip	No, Off-chip	No, Off-chip	Yes, PLL	Yes, PLL	No, Off-chip	No, Off-chip
Z-Path Power/Channel		0~7.5mW	N/A	[a]2.9mW	N/A	N/A	0-10mW	[c]0.4mW	N/A
XY-Path Power /Channel	Analog	[b]3.9mW	12.7mW	[b]83mW	54mW	[b]6.7mW	[b]7.8mW	[c]1.9mW	2mW
	Digital	2.4mW @ 1GHz	10.4mW @ 1GHz	10-140mW @ 1.6GHz	330mW @ 1GHz	12.4mW	3.8mW @ 1.25GHz	[c]2.3mW	N/A
	LO	[d]7.4mW	N/A	N/A	N/A	N/A	12.5mW	N/A	N/A
	Total	**13.7mW**	23.1mW	93-223mW	384mW	19.1mW	24.1mW	[c]4.2mW	[e]2mW
Waveform Type		Arbitrary	Arbitrary	Arbitrary	Arbitrary	Rect./Raised cosine	Rect./Raised cosine	Cosine	Symmetric pulse
Target Fidelity		99.9%	99.99%	99.99%	99.99%	99.99%	N/A	99.99%	99.99%
DRAG Pulse Generation		No	Yes	No	No	Yes	No	Yes	No
[1]Chip Area/Channel		0.9mm²	[f]1.61mm²	[f]4mm²	4mm²	1.04mm²	[f]1.3mm²	3.5mm²	1.6mm²
[2]Power/qubit under active control		[h]13.7mW/qubit (w/ LO)	23.1mW/qubit (w/o LO)	[i]3-7mW/qubit (w/o LO)	[i]12mW/qubit (w/o LO)	19.1mW/qubit (w/o LO)	24.1mW/qubit (w/ LO)	[c]4.2mW/qubit (w/o LO)	[e]2mW/qubit (w/o LO)

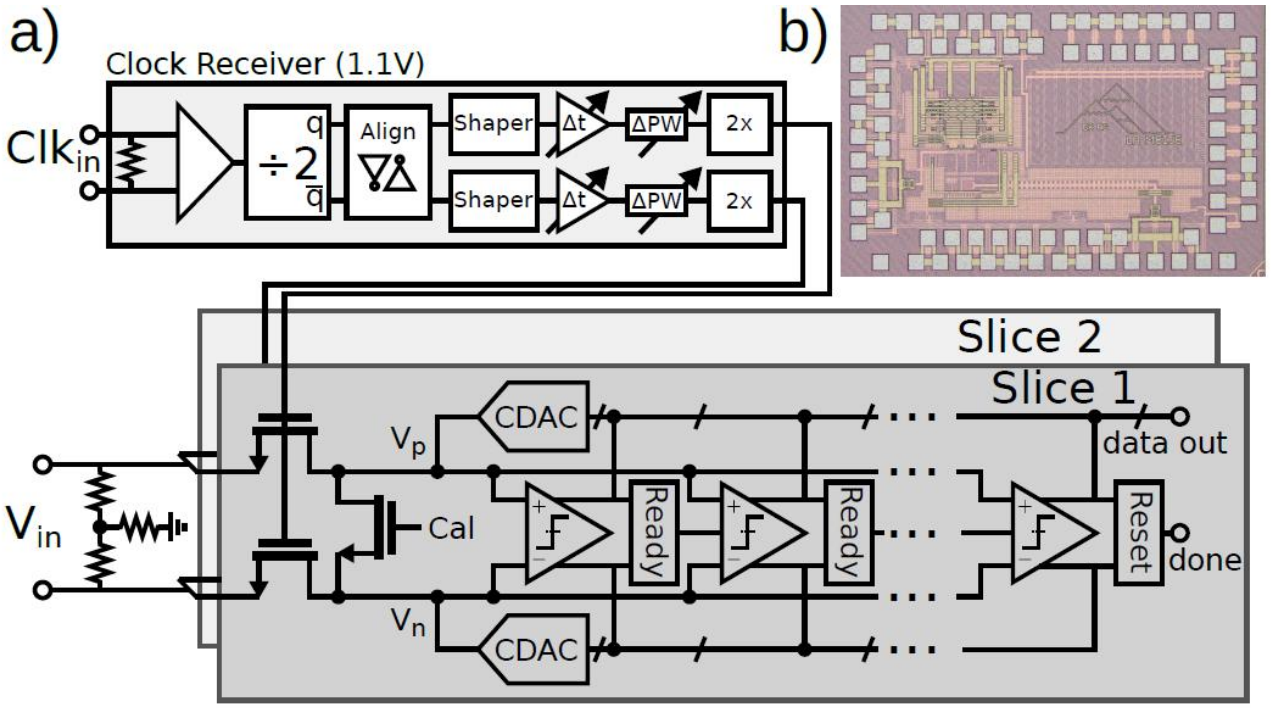
[1] The chip area includes the area of analog, digital and LO.
[2] The power is the total power of one channel including analog, digital and LO (if integrated on-chip).

[a] Gate pulsing for spin qubits.
[b] Tested with continuous output at max. output power.
[c] The power is the average power with a non-continuous quantum gate operation.
[d] Including the power of the clock generator and LO buffer.
[e] This IC only generates 16 types of fixed length symmetric driving pulse.
[f] Estimated from the chip microphotographs.
[g] Estimated from the relative measurement results.
[h] The power consumption of a 500 MHz external reference is not included.
[i] The power consumption is calculated for 32 time-frequency multiplexed qubits under active control.

Cryo ADC Research Trends

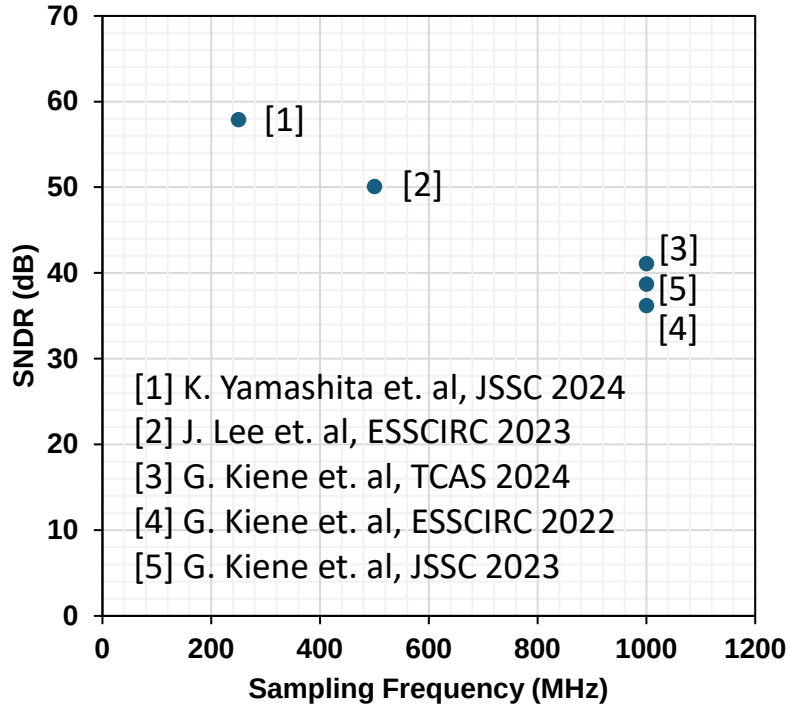
- Interleaved SAR ADCs are the mainstream
- F_S < 1GS/s, ENOB = 6～9bit

  This is due to significant power consumption constraints and the difficulty of making high-precision measurements.



2x Interleaving SAR ADC [4]

Ref	Fs (MS/s)	SNDR (dB)	Power (mW)	FoMw (fJ/c.-s.)	FoMs (dB)
[1]	250	57.9	24.7	154	154.9
[2]	500	50.1	5.91	45.1	156.4
[3]	1000	41.1	1.94	20.9	155.2
[4]	1000	36.2	10.6	100	142.9
[5]	1000	38.7	1.79	25.4	153.2

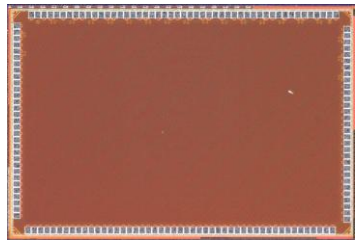


Digital Circuit Implementation



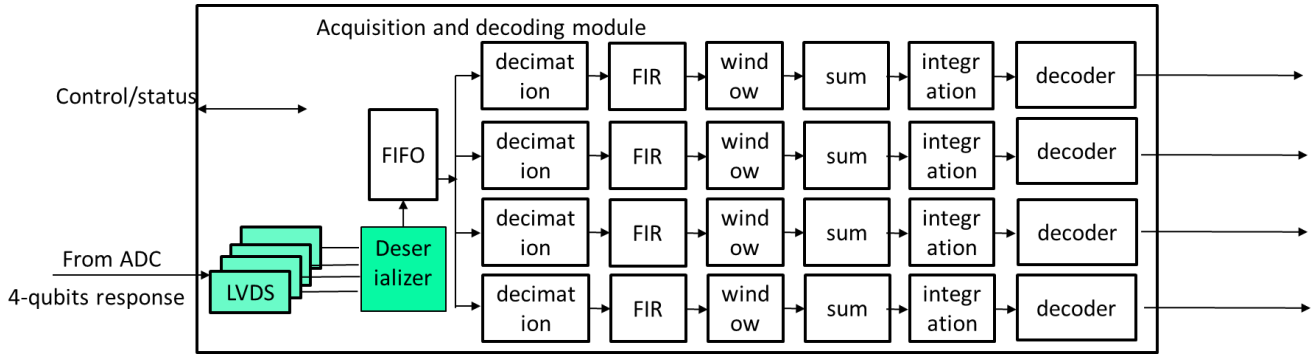
Kobayashi
Imagawa
Kishida

- **For frontend**
  - ✓ Migrate FPGA-based design by Quel (Miyoshi) to ASIC
    - ➢ Not easy-going. Synchronous reset on FPGA vs Asynchronous reset on ASIC. IP on FPGAs must be replaced by random logics.
    - ➢ LVDS interface from qubit by Prof. Miyahara



Die Photo

For 4 qubit	Power	
Clock Network	575 mW	→ Gated Clock
Memory	156 mW	→ GCDRAM
Others	17 mW	
Total	748 mW	



- **For backend**
  - ✓ A greedy error correction decoder to ASIC
    Smaller area and power than Kyushu-U's
    [Nakamura et. al, 2023/03 ARC-252]

		Power	Area
Kyushu-U's	180um	130 mW	6.83mm^2
Our Impl.	180um	25 mW	1.87mm^2
	22nm	685 µW	0.0163mm^2

RF Frontend

Tsuchiya

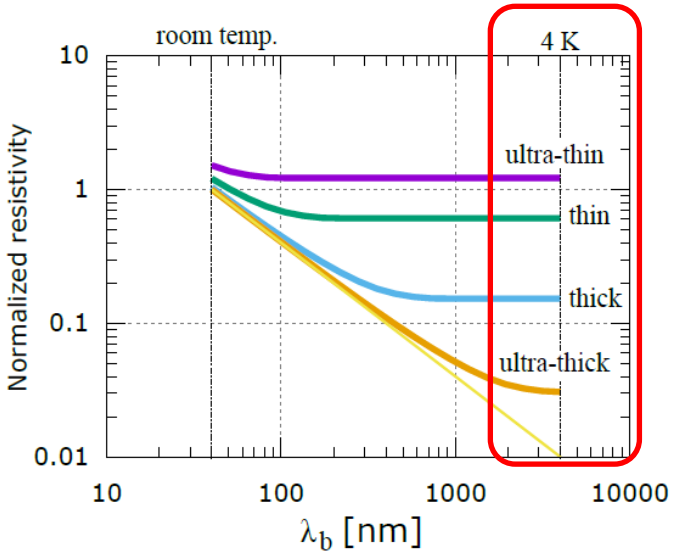
Mission 1: Cryo-RF Device model (-2025)

Cryo-RF device model is essential for future circuit design

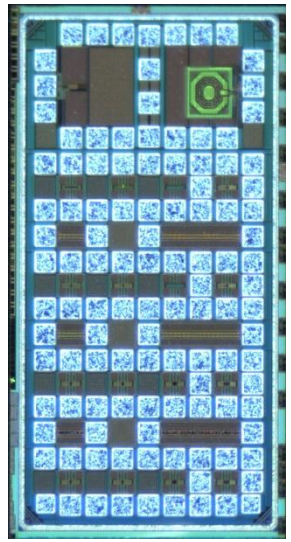
Current status: Numerical evaluation [SPI2024]

Measurement in progress

Resistance of thinner wires are still high at 4K



Numerical model of size-dependent ρ [IEEE SPI2024]



Chip for device modeling

Mission 2: Scalable RF frontend by Cryo-CMOS

Cryo-RF circuit design including PLL and mixer

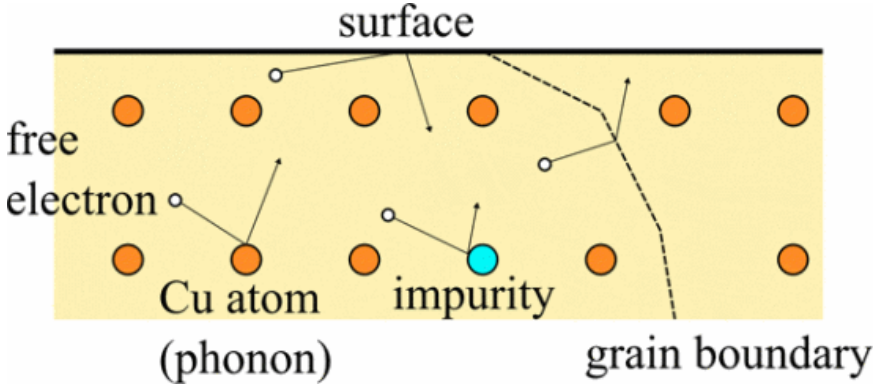
Current status: 1st test chip (PLL) in under measurement

2024-2025: PLL and mixer design (2024), Integration in a frontend ASIC (2025)

Milestone (-2030): Scalable RF frontend architecture

Current status: Survey and discussion with Subject 3

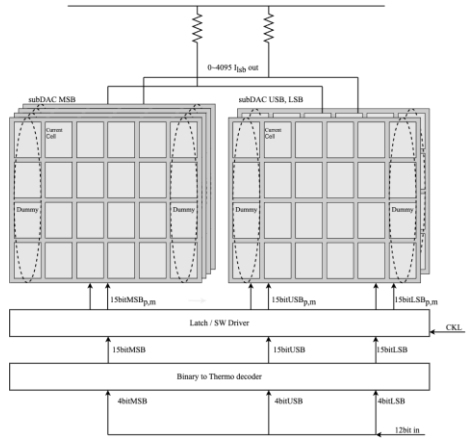
-2030: Propose scalable frontend/qubit architecture



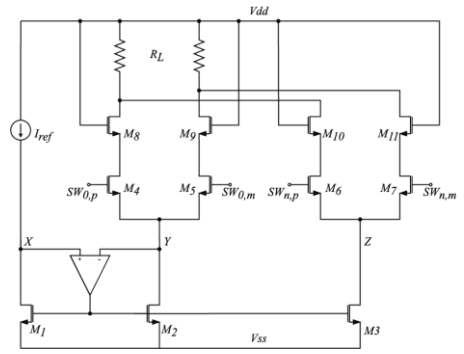
High-speed low-power DAC

Takai

- **Goal: Automatic design of High-speed DAC operating at a cryogenic temperature.**
- **Backgroud & Challenges**
  - ✓ Automatic design can vary parameters in the circuit more broadly than human design
  - ✓ Simulation of a DAC is time consuming, making it impractical to calculate rewards from simulation results of a DAC.
  - ✓ DAC consists of many identical circuits whose scale is small, so the simulation time of the identical circuit can be shortter.
- **Results & Future Works**
  - ✓ Automatic design program achieved a DAC with a power consumption of 4.35 mW and SFDR of 94.4dB in an execution time of 1,058 seconds.
  - ✓ Automatic design of a DAC using CMOSFET parameters compatible with a cryogenic temperature..



Scheme of 12bit DAC



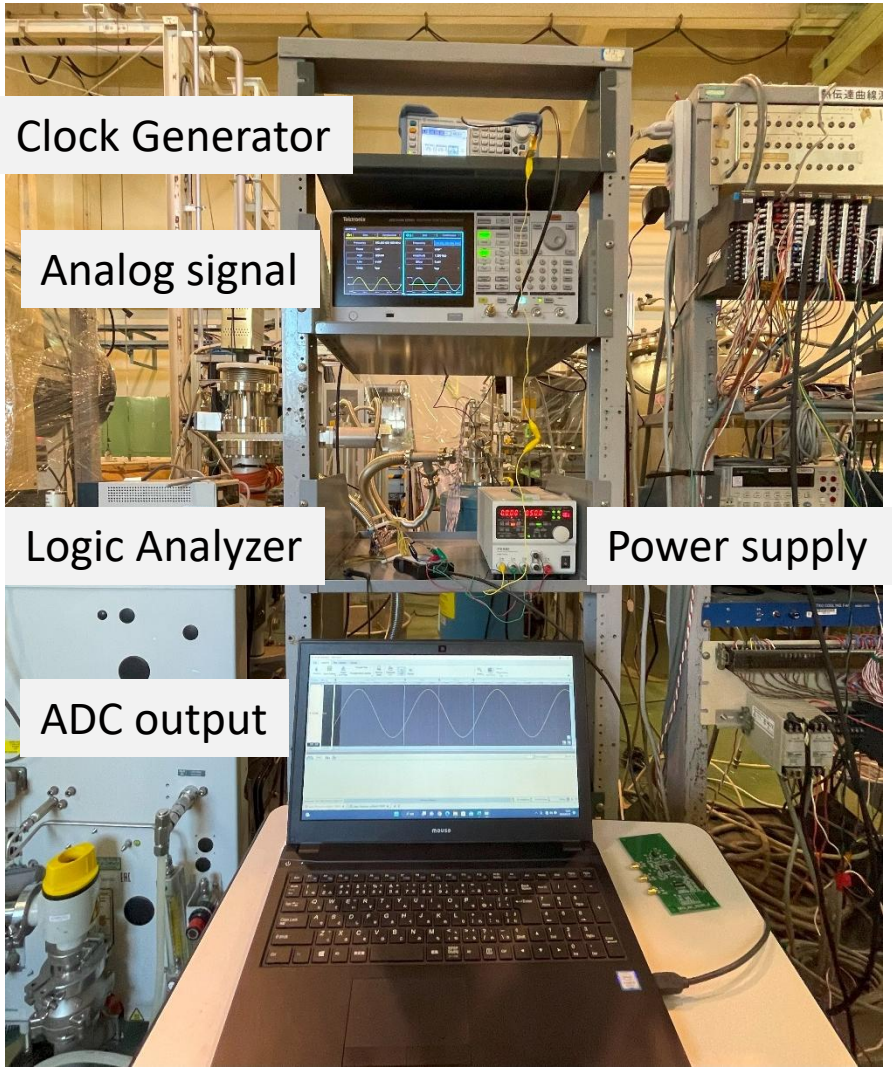
Element Circuit of 12bit DAC

Theme 4: High-speed ADC

- **Goal**
  - ✓ Development of a scalable Cryo ADC
    - ➢ Resolution ～12bit
    - ➢ Sampling rate ～6GS/s

Miyahara

- **Challenges**
  - ✓ Development of scalable ADC architecture suitable for interleaved operation
  - ✓ Development of calibration techniques for channel-to-channel mismatches with flexibility
- **Current Status**
  - ✓ Successfully design and evaluated of a high-speed, low-power single Cryo ADC using 22nm bulk CMOS
  - ✓ Currently designing an interleaved ADC aiming for 2GS/s operation



10bit, 300MS/s, 2.5mW @4.2K

Agenda

- **Self Introduction**
- **Introduction**
  - ✓Moonshot Goal 6 for quantum computers
  - ✓Integrated circuits (Classical electronics) and quantum computers
- **QUBECS**
  - ✓Overview of my project for developing an FTQC (Fault-tolerant quantum computer)
- **Conclusion**

Conclusion

- **Classical electronics (semiconductor chips) must be used to develop an FTQC**
  - ✓ To control qubits and correct errors
  - ✓ Current advances of Si-based integrated circuits are not based on Moore's law. High-cost and power-hungry → QC may be a help
- **Fidelity and Scalability of qubits are insufficient to develop an FTQC**
  - ✓ Reliability, Reproducibility, and Mass-productivity must be incorporated
- **QUBECS in the Moonshot Goal 6**
  - ✓ 14 PIs mainly for classical electronics. No quantum physicists
  - ✓ Theme 1 for error correction by using FPGA cluster
  - ✓ Theme 2 & 5 for a qubit controller at room temperature
  - ✓ Theme 3 & 4 for integrated and optical circuits working at cryogenic temperature to control qubits and correct errors

Thank you!

QUBECS
Quantum Bit Error Correction System
Moonshot Goal 6

- **Question or comment**

Search “QUBECS”

https://www.greenlab.kit.ac.jp/qubecs/