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A Three-Level GaN Driver for High False Turn-ON Tolerance with Minimal Reverse Conduction Loss

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ABSTRACT This paper presents a three-level gate driver for GaN HEMTs (Gallium Nitride High Electron Mobility Transistors) for high false turn-on tolerance and low reverse conduction loss during both dead time at turn-on and turn-off. The proposed gate driver reduces the reverse conduction loss by clamping between the gate and source terminals only during dead time. It has a capacitor which works as a negative voltage source and prevents from the false turn-on phenomenon. It operates only with a single voltage source and a PWM (Pulse Width Modulation) output signal. The proposed gate driver is implemented on a 48V-to-12V synchronous rectifier buck (SR-buck) converter and compared with other countermeasure methods for the false turn-on phenomenon. At the condition of 1 MHz, 30 ns dead time, and 120 W output power, the efficiencies of the proposed and conventional operations are 95.1% and 92.8% respectively. The margin between the threshold voltage and the peak of oscillated voltage of the proposed method becomes 1.3 times larger than that of the conventional method on average.

INDEX TERMS GaN HEMT, gate driver, three-level, false turn-on, reverse conduction loss, dead time

I. Introduction

Nowadays, power converters with high efficiency and density are required to reduce carbon dioxide. Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have excellent device characteristics such as fast switching capability, low on-resistance, and zero reverse recovery loss. Thanks to these characteristics, switching and conduction losses can be reduced, and power converters implemented by GaN HEMTs can operate at high frequency with smaller passive elements [1], [2], [3], [4]. Since GaN HEMTs have similar properties to Silicon-based power MOSFETs except for those excellent characteristics, it is also advantageous that existing technologies are easy to migrate.

However, GaN HEMTs are vulnerable to the false turn-on phenomenon [5], [6], [7], [8] [9]. If the false turn-on phenomenon occurs, the power loses due to the short-circuit current. In the worst case, the power devices may be broken. GaN HEMTs have lower threshold voltage $V_{\rm th}$ than Silicon-based power MOSFETs. Thus, for GaN HEMTs, the false turn-on phenomenon is more likely to occur than Silicon-based power MOSFETs.

One of general driving method to prevent from the false turn-on phenomenon is to apply a negative bias voltage during off-state [10], [11]. Increasing the margin between the driving voltage during off-state and $V_{\rm th}$ improves the tolerance of the voltage oscillation at the gate terminal. However, applying a negative voltage to the gate terminal increases the reverse conduction loss due to the unique I-V curve of GaN HEMTs [12], [13] [14]. The larger negative $V_{\rm GS}$ becomes, the larger source-to-drain voltage $V_{\rm SD}$ becomes, increasing the reverse conduction loss. Therefore, there is a trade-off between prevention from the false turn-on phenomenon and reduction of the reverse conduction loss.

To resolve them, various three-level gate drivers have been proposed [15], [16], [17], [18], [19], [20], [21], [22]. In these driving methods, negative voltage is applied to the gate terminal at turn-off. After the period when the false turn-on phenomenon may occur, the gate-to-source voltage $V_{\rm GS}$ goes to 0 V to reduce the reverse conduction loss during turn-on dead time. However, since GaN HEMTs turns off with negative voltage, the reverse conduction loss during turn-off dead time remains to increase. In [23], a three-level gate

driver to reduce the reverse conduction loss during both dead time has been proposed. However, additional voltage source and control signal are required.

To reduce the reverse conduction loss, the adaptive dead time control techniques have been proposed [24], [25], [26], [27]. In these methods, dead time is optimized by feedback, resulting in reducing the reverse conduction loss. However, accurate dead time control requires high performance control circuit and gate drivers. The performance variation and production cost must be considered. Thus, a simple and inexpensive method to reduce the reverse conduction loss is mandatory.

In this paper, we propose a three-level gate driver for high false turn-on tolerance to minimize increase of the reverse conduction loss. The proposed gate driver can reduce the reverse conduction loss to equalize the voltage levels of the gate and source terminals during both dead time periods. To prevent from the false turn-on phenomenon, the negative voltage applies to the gate terminal at the same time that the voltage oscillation occurs. Since the dead time is over, the large negative voltage can be used, and the tolerant for the false turn-on phenomenon can be improved. The proposed gate driver has a capacitor that works as a negative voltage supply to generate the third level voltage. Thus, it does not require any additional voltage source. In addition, the control signals for the proposed three-level gate driving method can be generated by a general dead time controller using a PWM output signal. Thus, it can operate only with a single PWM output signal. Since it can be also configured to other countermeasure driving methods, we compared them under the same conditions except for gate driving methods.

This paper is organized as follows. We explain the issues of GaN HEMTs and the related works in Section II. Section III presents the proposed three-level gate driver and its operation principle. Section IV shows an experimental setup and measurement results. Finally, the conclusions are given in Section V.

II. Preliminaries

A. Switching issues of GaN HEMTs

1) False turn-on phenomenon

In many power converters, phase-leg configurations are used. Regardless of the kind of power devices, the false turn-on phenomenon may cause in these circuits. Due to the false turn-on, there are risks of power loss by the simultaneous turn-on of both switches and power device failure in the worst case.

Fig. 1 shows the mechanism of the false turn-on phenomenon in the case of a SR-buck converter described as follows.

(a) When the low-side switch is off-state and the high-side switch turns on after the dead time is over, high positive dv/dt from the drain to source terminal of the low-side switch is generated.

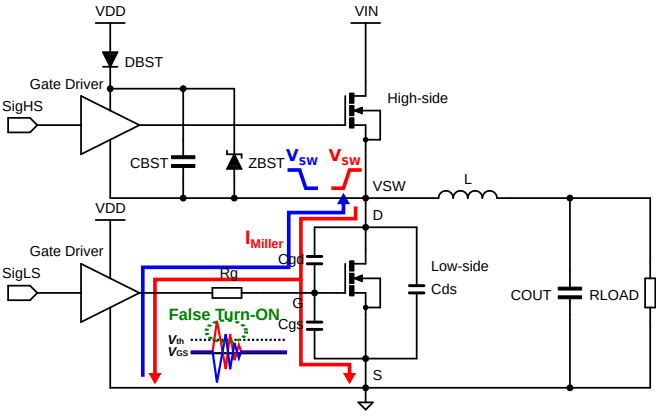


FIGURE 1. The mechanism of the false turn-on phenomenon in a SR-buck converter.

(b) By the dv/dt, the Miller current I_{Miller} flows to the gate and source terminals of the GaN HEMT through the Miller capacitor C_{GD}.

(c) Due to I_{Miller} and the gate resistor R_{G}, voltage oscillation beginning at the positive edge occurs at the gate terminal.

If the voltage oscillation exceeds V_{th} of the low-side switch, it turns on undesirably. This is called the false turn-on phenomenon. V_{th} of Si and SiC power MOSFETs are typically around 3 V to 4 V, while that of GaN HEMT is typically around 1 V to 2 V. Thus, GaN HEMTs are more likely to suffer from the false turn-on than Si and SiC power MOSFETs. Moreover, GaN HEMTs have a higher dV/dt at the drain terminal than other power MOSFETs due to their fast-switching capability. Thus, the amplitude of the voltage oscillation may be large.

When the high-side switch turns off, high negative dv/dt from the drain to source terminal of the low-side switch is generated. For the similar reason, current flows from the gate terminal to the drain terminal and the voltage oscillation beginning at the negative edge occurs. If the high-side switch is still off-state, both switches will not turn on simultaneously. However, if it exceeds the threshold voltage of the low-side switch when the high-side switch is not completely off-state, both switches could simultaneously turn on.

The general method to prevent from the false turn-on phenomenon is to drive the GaN HEMT by a negative voltage during off-state. By this method, the margin between off-state driving voltage and V_{th} increases and the tolerance for the voltage oscillation improves. However, an additional voltage source to apply a negative voltage is required, resulting in circuit area increase.

2) Reverse conduction loss

GaN HEMTs have another issue to increase the reverse conduction loss due to the unique reverse conduction mode. MOSFETs have a parasitic diode between the source and

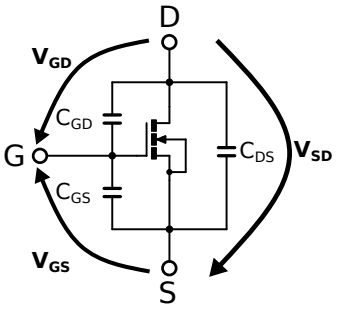


FIGURE 2. An equivalent model of GaN HEMTs.

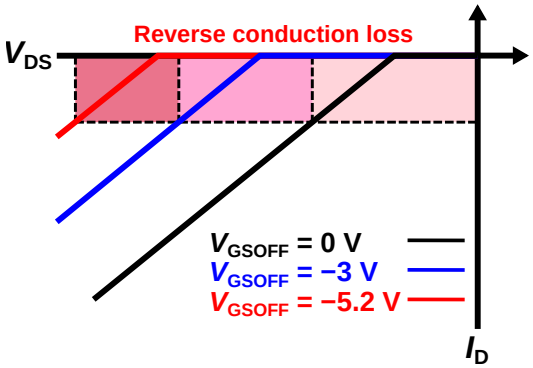


FIGURE 3. The third quadrant in the I-V curve of GaN HEMTs.

drain terminals called body diode. Drain current I_{D} flows through a body diode in the reverse conduction mode. Thus, source to drain voltage V_{DS} is equal to the forward voltage of the body diode. On the other hand, GaN HEMTs do not have a body diode. However, GaN HEMTs can behave like a diode in the reverse conduction mode. Fig. 2 shows an equivalent model of GaN HEMTs. Since GaN HEMTs have a symmetrical structure, the channel of GaN HEMTs is formed when V_{GS} or V_{GD} exceeds their V_{th}. In the reverse conduction mode of GaN HEMT, the parasitic capacitor C_{GD} and C_{DS} are charged. After V_{GD} reaches V_{th} of GaN HEMTs, I_{D} flows through the channel. V_{SD} is expressed as

$$V_{\mathrm{SD}} = V_{\mathrm{GD}} - V_{\mathrm{GS}}. \tag{1}$$

In addition, the effective channel resistance R_{SD} occurs the voltage drop. Because V_{GD} is equal to V_{th} in the reverse conduction mode, V_{SD} is expressed as

$$V_{\mathrm{SD}} = V_{\mathrm{th}} - V_{\mathrm{GS}} + R_{\mathrm{SD}} \cdot I_{\mathrm{D}}. \tag{2}$$

As the result, the I-V curve of GaN HEMTs in the third quadrant is illustrated as shown in Fig. 3. In a SR-buck converter, I_{OUT} and I_{D} are approximately equal in the reverse conduction mode. Thus, the reverse conduction loss $P_{\mathrm{T_{D(OFF)}}}$ during turn-off dead time $T_{\mathrm{D(OFF)}}$ is expressed as

$$P_{\mathrm{T_{D(OFF)}}} = V_{\mathrm{SD}} \cdot I_{\mathrm{OUT}} \cdot T_{\mathrm{D(OFF)}} \cdot f_{\mathrm{SW}}, \tag{3}$$

where f_{SW} is the operation frequency. In the condition of the same I_{OUT}, applying a negative V_{GS} in the reverse conduction mode increases V_{SD}, leading to the increase of the reverse conduction loss. Therefore, there is a trade-off between the false turn-on prevention and the reverse conduction loss increase.

B. Related works

1) Three-level gate driver

To prevent from the false turn-on phenomenon and reduce the reserve conduction loss at the same time, the three-level gate drivers have been proposed [15]–[23]. As an example, Figs. 4 and 5 show a capacitor-based three-level gate driver and the operating waveforms of the GaN HEMTs in a SR-buck converter in [18]. To prevent from false turn-on, the GaN HEMT turns off with a negative voltage. After that, the gate terminal goes back to 0 V to reduce the reverse

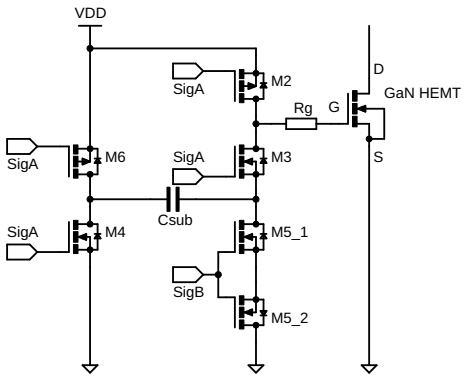


FIGURE 4. A capacitor-based three-level gate driver [18].

conduction loss during turn-on dead time. To go back to 0 V, they have a Miller clamp circuit or a RC discharge circuit.

However, in these methods, the reverse conduction loss during turn-off dead time is still large because the GaN HEMT is driven by a negative voltage during turn-off dead time. In addition, some proposed gate drivers require an additional voltage source and control signal, resulting in increase in circuit size. Moreover, it is required to adjust the parameters of the components such as resistors, capacitors, and zener diode. If more components must be adjusted, it is hard to guarantee the reliability of operation.

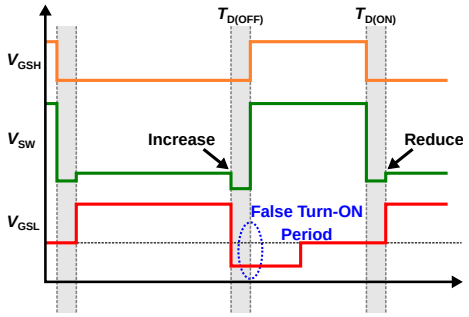


FIGURE 5. Operating waveforms of the GaN HEMTs for the Capacitor-based three-level gate driver in a SR-buck converter in Fig. 4.

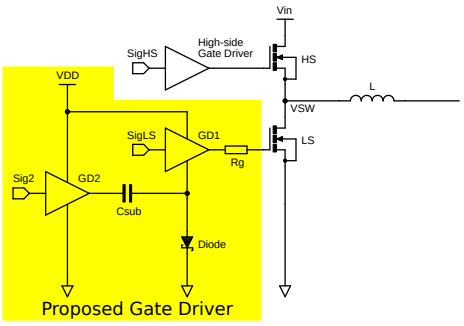


FIGURE 6. **The schematic of the proposed three-level gate driver.**

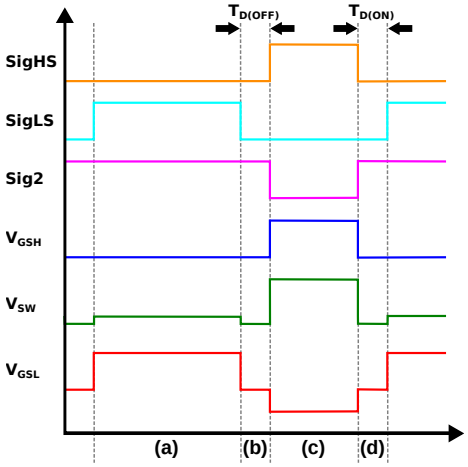


FIGURE 7. **Control signals and operating waveforms of the proposed gate driver.**

2) Adaptive dead time control

To reduce the reverse conduction loss, the dead time must be optimized. The dead time is generally fixed. However, the slew rate of the voltage at the switching node depends on the load current. Since the dead time is set for the load current with the smaller slew rate, the dead time is longer for load currents with the larger slew rate, resulting in increasing the reverse conduction loss.

To resolve it, the adaptive dead time control methods have been proposed [24]–[27]. In these methods, dead time is optimized by feedback to reduce the reverse conduction loss. However, to prevent from the false turn-on phenomenon, an additional voltage source is required. In addition, accurate dead time control requires high performance control circuit and gate drivers, resulting in higher cost. The performance variation at production must be also considered.

III. Proposed three-level gate driver

A. Gate Driving Stage

We propose a capacitor-based 3-level gate driver to address the aforementioned issues with high false turn-on tolerance, the reverse conduction loss reduction, and ease to drive. The schematic of the proposed gate driver is depicted in Fig. 6. The gate driver (GD2), the capacitor ($C_{\rm sub}$), and the diode (Diode) are added to the 2-level gate driver. The

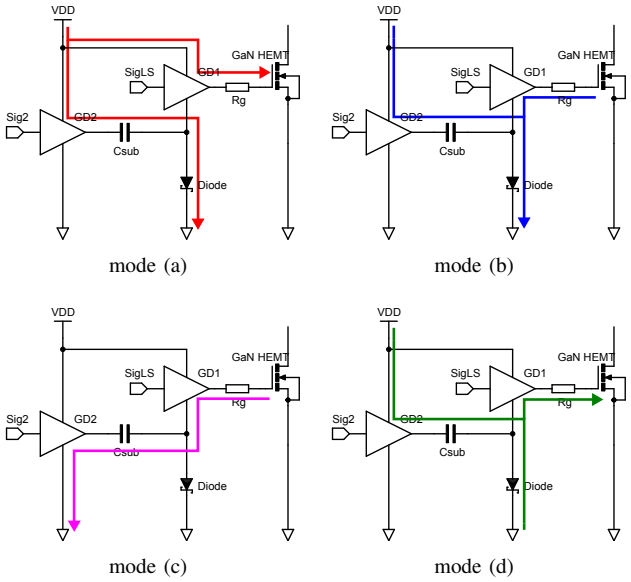


FIGURE 8. **Operation principle of the proposed gate driver.**

capacitor $C_{\rm sub}$ works as the negative voltage source. Thus, the proposed gate driver operates only with a single voltage source. It works with two control signals and a negative voltage is applied to the gate terminal at the period when Sig2 is low.

The waveforms of the control signals for the proposed 3-level gate driving method are shown in Fig. 7. To reduce the reverse conduction loss, $V_{\rm GS}$ is set to 0 V during the turn-on dead time $T_{\rm D(ON)}$ and turn-off dead time $T_{\rm D(OFF)}$. On the other hand, in order to prevent from the false turn-on phenomenon, the proposed 3-level method applies a negative voltage to the gate terminal from the end of $T_{\rm D(OFF)}$ to the beginning of $T_{\rm D(ON)}$.

Figs. 8 show the operation principle of the proposed gate driver described as follows.

(a) GaN HEMT turns on. At the same period, current flows to the ground through $C_{\rm sub}$ and Diode, and energy to use during off-state is stored in $C_{\rm sub}$.

(b) GaN HEMT turns off. To reduce the reverse conduction loss during the turn-off dead time, the gate terminal of GaN HEMT is clamped to the source terminal through Diode.

(c) Simultaneously turning on of high-side switch, to prevent from false turn-on, a negative voltage is applied to the gate terminal of GaN HEMT. In this period, $C_{\rm sub}$ works as a negative voltage supply.

(d) To reduce the reverse conduction loss during dead time just before turn-on, the gate terminal of GaN HEMT is clamped to the source terminal through Diode again.

In the conventional 3-level gate driver, the component parameters must be adjusted to achieve the recommended

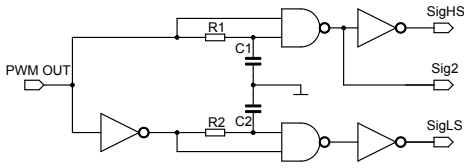


FIGURE 9. A schematic of a general dead time controller using a PWM output signal.

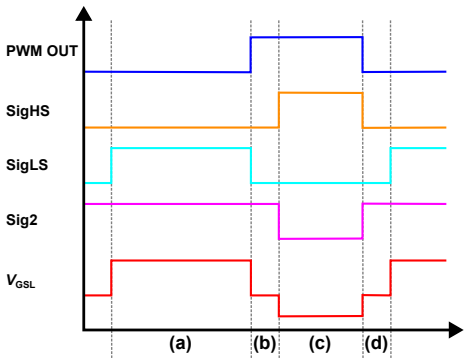


FIGURE 10. Diagram of generating a control signal for the proposed 3-level method.

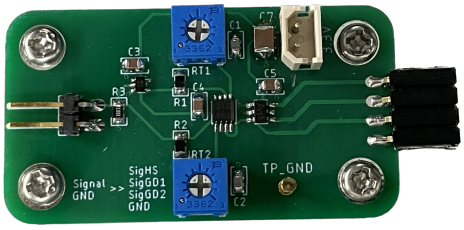


FIGURE 11. The circuit board of the signal generator for the proposed 3-level method.

negative voltage (from -2 V to -3 V) because large negative voltage during dead time increases the reverse conduction loss [28]. On the other hand, in the proposed 3-level method, the component parameters do not have to be optimized because the dead time is over and the reverse conduction loss does not increase. In addition, the high false turn-on tolerance can be achieved by applying a large negative voltage to the gate terminal. Therefore, in order to apply enough negative voltage, $C_{\rm sub}$ should be larger than the input capacitance of GaN HEMT in use.

Since the proposed gate driver changes $V_{\rm GS}$ back to 0 V at the same time as the high-side switch turns off, the false turn-on phenomenon may be less likely occur due to the negative $V_{\rm GS}$ during the initial phase of the voltage at the switching node $V_{\rm SW}$ transition.

A concern is switching characteristics degradation. Compared with a general 2-level gate driver, the rise time are not affected because the turn-on path is the same. However, the fall time is predicted to be slow due to added diode on turn-off path. Therefore, Diode is desirable to have a low forward voltage because it may affect the turn-off voltage.

B. Signal generator for the proposed 3-level method

Because the conventional 3-level method clamps the gate terminal to the source terminal during off-state, it needs to generate the dedicated signal such as activating a miller clamp circuit in that time. Thus, the controller could be complex. On the other hand, the proposed 3-level method clamps the gate terminal to the source terminal at the start of the turn-on dead time. The control signal Sig2 can be generated by inverting the control signal of the high-side switch SigHS. Sig2 is easily generated from a general dead time controller using a PWM output signal. The schematic of the general dead time controller is shown in Fig. 9. It generates signals with dead time for the low-side and high-side switches. In the process of generating these signals, the inverting signal for the high-side switch is already generated. Therefore, the proposed 3-level gate driver can operate at the proposed 3-level method by a single control signal PWM OUT in Fig. 10. In the measurement results described in the next section, the proposed 3-level method can be implemented with this signal generator (Fig. 11).

IV. Measurement results

In this section, measurement results are shown when the proposed gate driver is implemented to a resistive load circuit and a 48V-to-12V SR-buck converter.

A. Switching characteristics

To compare the switching characteristics of the proposed and other gate driving methods, the proposed gate driver is implemented on the resistive load circuit. The resistive load circuit for the proposed gate driver is illustrated in Fig. 12. The component names and experimental setups are shown in Tables 1 and 2. The GaN HEMT used is GS61004B (GaN Systems, $V_{\rm th.min} = 1.1$ V). The gate resistor is set to 1 Ω. We measured $V_{\rm GS}$ and the drain-to-source voltage $V_{\rm DS}$. From the results, switching characteristics are compared for the proposed 3-level method (P3L method) and conventional methods such as the 2-level method (0 V/5 V) (2L method)

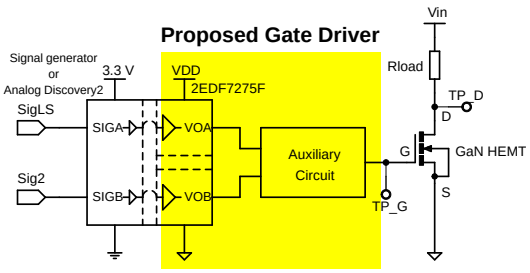


FIGURE 12. Resistive load circuit for the proposed gate driver.

TABLE 1 **Specification of the proposed gate driver.**

Symbol	Description	Value	Manufacturer
GD1	Isolated gate drivers	2EDF7275F(CH1)	Infineon
GD2	Isolated gate drivers	2EDF7275F(CH2)	Infineon
C_{SUB}	Ceramic capacitor	3.3 nF	TDK
Diode	Schottky barrier diode	RBR2MM40ATR	Rohm

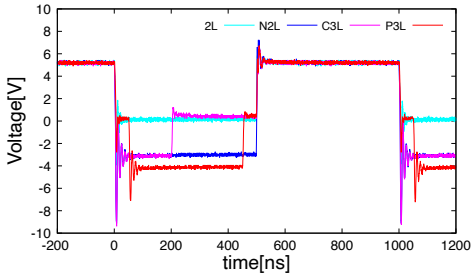
TABLE 2 **Measurement equipments.**

Instrument	Product	Manufacturer
Oscilloscope	DPO7054C	Tektronix
Signal Generator	Analog Discovery2	Digilent
DC High Voltage Supply	PR500-10	Matsusada Precision
DC Voltage Supply	P4K-80M	Matsusada Precision

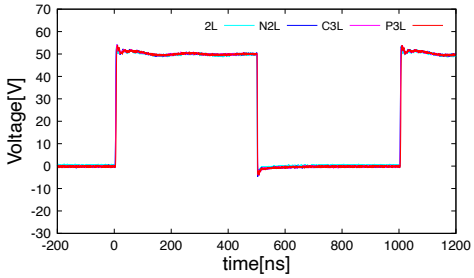
the negative bias 2-level method (−3 V/5 V) (N2L method), and the conventional 3-level method (C3L method) [18]. All methods can be measured on the same print circuit board. N2L, C3L, and P3L methods are changed by Sig2. P3L method can be implemented with the signal generator in Fig. 11. 2L method is configured by replacing Diode to 0 Ω resistor and removing C_{sub}. The measurement conditions are at 48 V of input voltage V_{IN}, 12 Ω of R_{load}, 1 MHz operation frequency, and 50% duty ratio. The periods of mode (b) and mode (d) for P3L method are set to 50 ns. C_{sub} is adjusted to −3 V of the recommended negative voltage in the conventional methods.

Figs. 13 and 14 show the entire and all magnified switching waveforms of V_{GS} and V_{DS} for all methods. According to Fig. 14(a), GaN HEMT is driven by 0 V during 50 ns just after turn-off by P3L method. After that, a larger negative voltage than that of the other methods is applied to the gate terminal. Therefore, it is expected to reduce the reverse conduction loss during not only turn-on dead time but also turn-off dead time and improve the tolerance for the false turn-on phenomenon.

Table 3 shows the evaluation results of switching characteristics. 2L, C3L, and P3L methods have the same rise time T_{rise} because the turn-on path is common and their V_{GS} start up from the same voltage 0 V. T_{rise} for P3L method is 40% slower than that for N2L method because V_{GS} starting up from a negative voltage gives high dV_{GS}/dt. On the other hand, the fall time T_{fall} for P3L method is 11%, and 9.3% slower than those for N2L and C3L methods respectively because the negative voltage discharges the input capacitance of GaN HEMTs faster. T_{fall} for P3L method is 3.5% slower than that for P3L method. Because the gate terminal is clamped to the source terminal via a diode, P3L method becomes slower. Therefore, it is predicted that P3L method increases switching loss at turn-off more than the conventional methods.

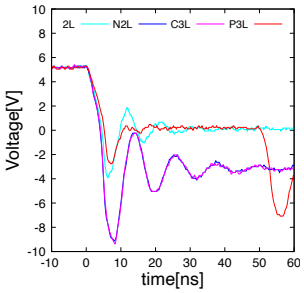


(a) V_{GS}.

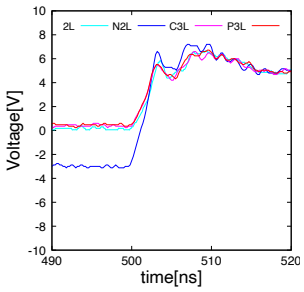


(b) V_{DS}.

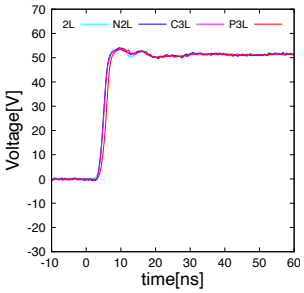
FIGURE 13. **The whole waveform of V_{GS} and V_{DS} by resistive load circuit.**



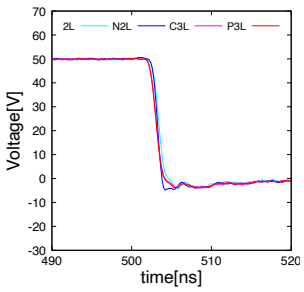
(a) V_{GS} at turn-off.



(b) V_{GS} at turn-on.



(c) V_{DS} at turn-off.



(d) V_{DS} at turn-on.

FIGURE 14. **Magnified waveforms of V_{GS} and V_{DS}.**

B. 48V-to-12V SR-Buck converter

To evaluate the tolerance for the false turn-on phenomenon, reverse conduction loss during dead time, and power conversion efficiency, the proposed 3-level gate driver is implemented on the 48V-to-12V SR-buck converter. A schematic

TABLE 3 Evaluation results of switching characteristics for all methods compared with C3L.

	2L	N2L	C3L	P3L
$T_{\rm rise}$	1.30 ns	0.93 ns	1.30 ns	1.30 ns (+0%)
$T_{\rm fall}$	2.26 ns	2.11 ns	2.14 ns	2.34 ns (+9.3%)

TABLE 4 The specifications of SR-Buck converter.

$V_{\rm IN}$	48 V
$V_{\rm OUT}$	12 V
Frequency $f_{\rm SW}$	1 MHz
Power	24 W - 120 W
Input capacitance	44 μF
Output capacitance	32 μF
Inductance	10 μH

of the SR-buck converter including gate drivers are shown in Fig. 15. The tolerance for the false turn-on phenomenon is evaluated by the margin voltage $V_{\rm margin}$ between $V_{\rm th}$ of GaN HEMT and the peak of the oscillated voltage at $V_{\rm GS}$ of low-side switch $V_{\rm GL}$.

The high-side gate driver is a conventional gate driver. To drive a high-side switch, high-side gate driver has a bootstrap circuit composed of capacitor $C_{\rm BST}$, fast recovery diode $D_{\rm BST}$, zener diode $Z_{\rm BST}$, and resistor $R_{\rm BST}$. The turn-on and turn-off resistors for the high-side switch are set to 10 Ω and 1 Ω, respectively. The low-side gate driver is the proposed 3-level gate driver. As well as the resistive load circuit, all methods are measured on the same print circuit board. The measurement conditions are described as below.

(1) Output power is fixed to 48 W, and dead time is swept from 10 ns to 50 ns (every 10 ns)
(2) Dead time is fixed to 30 ns, and output power is swept from 24 W to 120 W (every 24 W)

By the measurement condition (1), the dead time dependence of the power conversion efficiency is evaluated. By the measurement condition (2), the load dependence of the power conversion efficiency is evaluated.

The specifications of the SR-buck converter are shown in Table 4. The photograph of the SR-buck converter is shown in Fig. 16.

Figs. 17 show the magnified waveforms of gate voltages for all methods. The evaluation results of $V_{\rm margin}$ are shown in Figs. 18 and 19. At the condition (1), the $V_{\rm margin}$ of P3L method is 1.5 times larger than that of C3L method. At the condition (2), the $V_{\rm margin}$ of P3L method is 1.3 times larger than that of C3L method. The negative voltage for C3L method is about −3 V, while that for P3L method is about −4 V. Thus, the proposed 3-level method can improve the tolerance for the false turn-on phenomenon compared to the conventional 3-level method.

Figs. 20 show the magnified waveforms of $V_{\rm SW}$ and $V_{\rm GL}$ at the condition of 120 W output power and 30 ns dead time. In all methods, $V_{\rm GL}$ does not exceed $V_{\rm th}$ before the time $V_{\rm SW}$

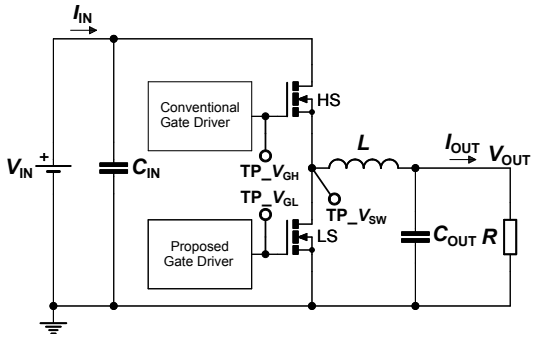


FIGURE 15. A schematic of the measurement SR-buck converter.

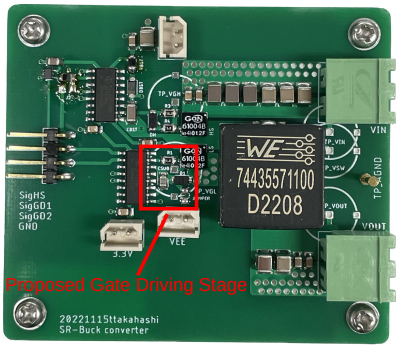
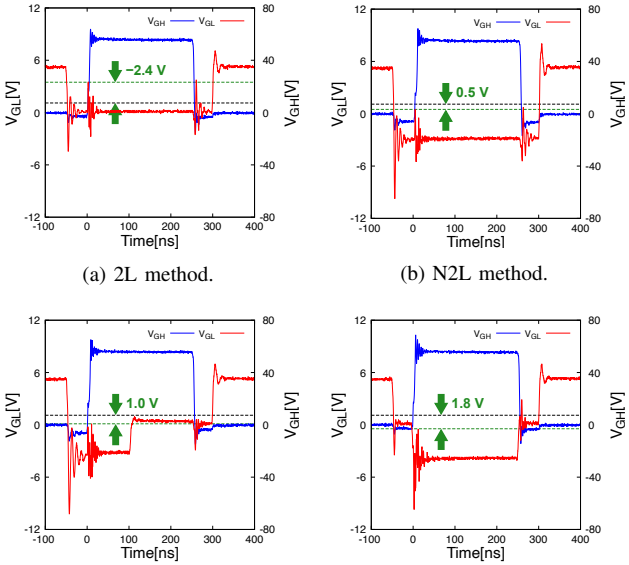


FIGURE 16. The measurement SR-buck converter.

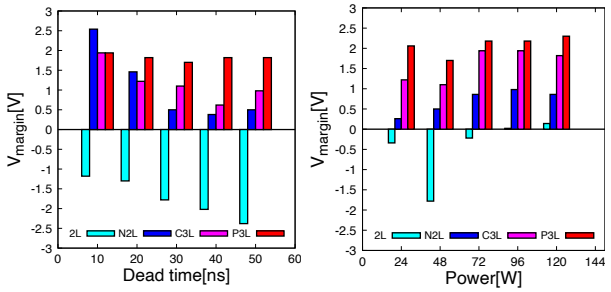
reaches 10%. After that, $V_{\rm GL}$ exceeds $V_{\rm th}$ and all methods take 2.0 ns to 2.8 ns to exceed $V_{\rm th}$ due to the high speed turn-off of GaN HEMT and the negative edge beginning of voltage oscillation. Thus, simultaneously turning on of both



(a) 2L method. (b) N2L method.

(c) C3L method. (d) P3L method.

FIGURE 17. Magnified waveform of gate voltages for all methods at the condition (1) at 50 ns dead time.



(a) Condition(1). (b) Condition(2).

FIGURE 18. V_{margin} **at all conditions.**

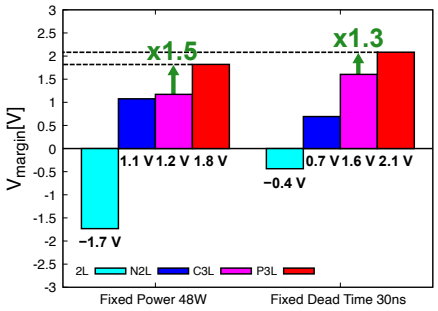
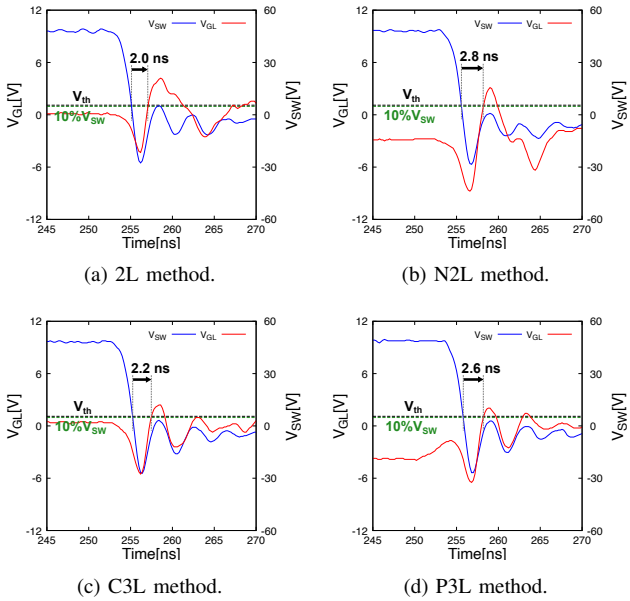


FIGURE 19. V_{margin} **at all conditions on average.**

switches is unlikely to occur due to the high negative edge dV/dt at V_{SW}.

Fig. 21 shows the waveforms of the output current I_{OUT} and the voltage at switching node V_{SW} during dead time at the condition of 48 W output power and 50 ns dead time. The evaluated results are shown in Table 5. The V_{SW} during turn-off dead time $T_{\mathrm{D(OFF)}}$ for P3L and C3L methods are



(a) 2L method. (b) N2L method.

(c) C3L method. (d) P3L method.

FIGURE 20. Magnified waveforms of V_{SW} and V_{GL} at the condition (2) at 120 W output power.

TABLE 5 Voltage at switching node during dead time compared with N2L method.

	2L	N2L	C3L	P3L
$T_{\mathrm{D(OFF)}}$	−3.0 V	−6.0 V	−6.0 V	−3.0 V (−50%)
$T_{\mathrm{D(ON)}}$	−4.1 V	−7.2 V	−4.1 V	−4.1 V (−43%)

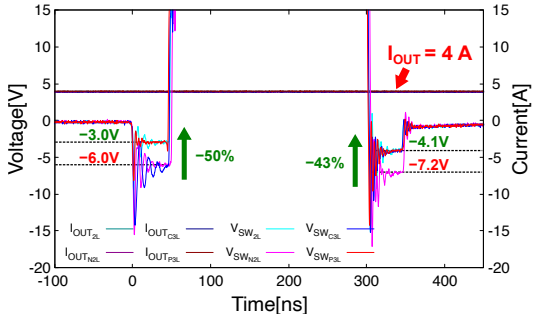


FIGURE 21. I_{OUT} **and** V_{SW} **waveforms during dead time for all methods.**

−3 V and −6 V, respectively. Thus, the reverse conduction lose during $T_{\mathrm{D(OFF)}}$ is reduced by 50%. The V_{GL} of C3L method during $T_{\mathrm{D(OFF)}}$ is −3 V, while that of P3L method during $T_{\mathrm{D(OFF)}}$ is 0 V. Thus, from Eq. (2), the V_{SW} during $T_{\mathrm{D(OFF)}}$ for P3L method is 3 V smaller than that for C3L method, resulting in reducing the reverse conduction loss.

The efficiencies of all methods except for 2L method without the tolerance for the false turn-on at the condition (1) and condition (2) are shown in Figs. 22 and 23. At the condition (1), efficiencies of all methods are improved as the dead time becomes shorter. This is because shorter dead time directly reduces the reverse conduction loss. In particular, shorter dead time is effective for N2L and C3L methods. However, even at a shorter dead time, the efficiencies of P3L method are the highest of all. At the condition of 50 ns dead time, the efficiencies of P3L and C3L methods are 94.8% and 92.6%, respectively. Thus, the proposed 3-level method improves the efficiency by 2.2%. From Eq. (3), the difference of $P_{\mathrm{T_{D(OFF)}}}$ between C3L and P3L methods is 0.6 W, which is equal to 1.2% of the input power. According to Fig. 21,

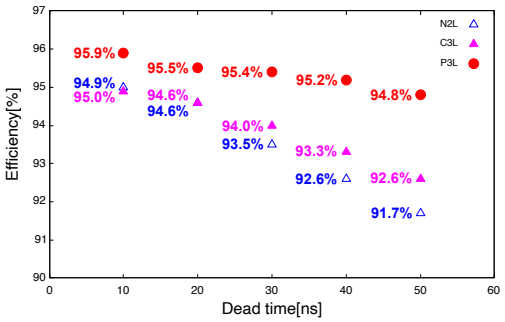


FIGURE 22. Power conversion efficiencies for all methods at the condition (1).

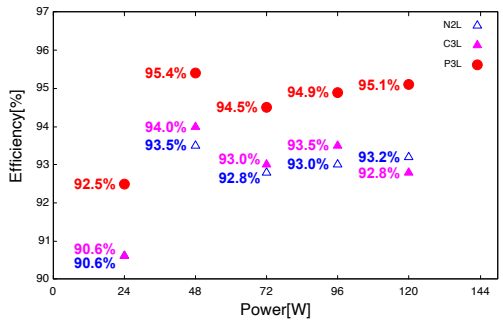


FIGURE 23. Power conversion efficiencies for all methods at the condition (2).

the spike voltage and ringing are caused at V_{SW}. Thus, it is expected that the difference of $P_{\mathrm{T_{D(OFF)}}}$ between C3L and P3L methods is more than 0.6 W. Since the measurement condition is the same except for the driving method, the power conversion efficiency is improved due to reduction of the reverse conduction loss.

At the condition (2), according to Fig. 23, the efficiencies of P3L method are the highest of all. As well as at the condition (1), the power conversion efficiency is improved due to reduction of the reverse conduction loss.

Therefore, by using the proposed 3-level method and gate driver without any precise dead time control and multiple control signals, the tolerance for the false turn-on phenomenon and power conversion efficiency can be improved due to the reduction of the reverse conduction loss.

V. Conclusion

In this paper, we propose the capacitor-based 3-level gate driver for GaN HEMTs effective in a circuit with a phase-leg configuration. The proposed gate driver can prevent from the false turn-on phenomenon and reduce the reverse conduction loss during both dead time periods only with a single voltage source and PWM output signal.

The efficiencies of the proposed and conventional 3-level methods implemented with the 48V-to-12V SR-buck converter are 94.8% and 92.6% respectively at the condition of 48 W output power, 50 ns dead time, and 1 MHz operation frequency. Even with a shorter dead time, the efficiencies of the proposed 3-level method are the highest of all. The tolerance for the false turn-on phenomenon is 1.5 times larger than conventional methods on average. By using the proposed gate driver without precise dead time control and multiple control signals, the tolerance for the false turn-on phenomenon and power conversion efficiency are improved due to reduction the reverse conduction loss.

REFERENCES

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014.

[2] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, B. Liu, and R. Ren, "Characterization of an enhancement-mode 650-V GaN HFET," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 400–407.

[3] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, 2016.

[4] K. J. Chen, O. Häberlen, A. Lidow, C. l. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 779–795, 2017.

[5] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Cross conduction analysis for enhancement-mode 650-V GaN HFETs in a phase-leg topology," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 98–103.

[6] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An analytical model for false turn-on evaluation of GaN transistor in bridge-leg configuration," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–6.

[7] F. Zhao, Y. Li, Q. Tang, and L. Wang, "Analysis of oscillation in bridge structure based on GaN devices and ferrite bead suppression method," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 391–398.

[8] T. Iwaki, S. Ishiwaki, T. Sawada, and M. Yamamoto, "An analysis of false turn-on phenomenon of GaN HEMT with parasitic components," in *2017 IEEE International Telecommunications Energy Conference (INTELEC)*, 2017, pp. 347–350.

[9] B. Li, G. Wang, S. Liu, N. Zhao, G. Zhang, X. Zhang, and D. Xu, "Modeling and Analysis of Bridge-Leg Crosstalk of GaN HEMT Considering Nonlinear Junction Capacitances," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4429–4439, 2021.

[10] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent Gate Drive for Fast Switching and Crosstalk Suppression of SiC Devices," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9319–9332, 2017.

[11] B. Zhang, S. Xie, J. Xu, Q. Qian, Z. Zhang, and K. Xu, "A Magnetic Coupling Based Gate Driver for Crosstalk Suppression of SiC MOSFETs," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9052–9063, 2017.

[12] GaN Systems Inc., "An Introduction to GaN Enhancement-mode HEMTs," GN001 Application Guide[Online], Mar. 2022, Available:https://gansystems.com/wp-content/uploads/2022/03/GN001_An-Introduction-to-GaN-E-HEMTs_220308.pdf.

[13] C. Sørensen, M. L. Fogsgaard, M. N. Christiansen, M. K. Graungaard, J. B. Nørgaard, C. Uhrenfeldt, and I. Trintis, "Conduction, reverse conduction and switching characteristics of GaN E-HEMT," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2015, pp. 1–7.

[14] W. Lee, D. Han, W. Choi, and B. Sarlioglu, "Reducing reverse conduction and switching losses in GaN HEMT-based high-speed permanent magnet brushless dc motor drive," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 3522–3528.

[15] Z.-L. Zhang, Z. Dong, D.-D. Hu, X.-W. Zou, and X. Ren, "Three-Level Gate Drivers for eGaN HEMTs in Resonant Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5527–5538, 2017.

[16] A. Seidel and B. Wicht, "A fully integrated three-level 11.6nC gate driver supporting GaN gate injection transistors," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 384–386.

[17] Y. Chen, R. Wang, X. Liu, and Y. Kang, "Gate-Drive Power Supply With Decayed Negative Voltage to Solve Crosstalk Problem of GaN Synchronous Buck Converter," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 6–11, 2021.

[18] J. Nagao, J. Furuta, and K. Kobayashi, "Capacitor-Based Three-Level Gate Driver for GaN HEMT Only with a Single Voltage Supply," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1–7.

[19] C. Liu, Z. Zhang, Y. Liu, Y. Si, and Q. Lei, "Smart Self-Driving Multilevel Gate Driver for Fast Switching and Crosstalk Suppression

of SiC MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 442–453, 2020.
[20] H. Zhou, M. Priestley, J. Fletcher, and K. Sun, "A Gate Driver with a Negative Turn Off Bias Voltage for GaN HEMTs," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 1083–1086.
[21] T. Takahashi, J. Nagao, J. Furuta, and K. Kobayashi, "A Capacitor-Based Multilevel Gate Driver for GaN HEMT Only with a Single Voltage Supply," in *2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2021, pp. 158–163.
[22] B. Li, G. Zhang, C. Li, G. Wang, S. Liu, and D. Xu, "Crosstalk Suppression Method for GaN-Based Bridge Configuration Using Negative Voltage Self-Recovery Gate Drive," *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4406–4418, 2022.
[23] X. Ren, D. Reusch, S. Ji, Z. Zhang, M. Mu, and F. C. Lee, "Three-level driving method for GaN power transistor in synchronous buck converter," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 2949–2953.
[24] Z. Chen, Y.-T. Wong, T.-S. Yim, and W.-H. Ki, "A 12A 50V half-bridge gate driver for enhancement-mode GaN HEMTs with digital dead-time correction," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 1750–1753.
[25] M. Zhou, Q. Low, and L. Siek, "A high efficiency synchronous buck converter with adaptive dead-time control," in *2016 International Symposium on Integrated Circuits (ISIC)*, 2016, pp. 1–4.
[26] M. Asad, A. K. Singha, and R. M. S. Rao, "Dead Time Optimization in a GaN-Based Buck Converter," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2830–2844, 2022.
[27] C.-J. Chen, P.-K. Chiu, Y.-M. Chen, P.-Y. Wang, and Y.-C. Chang, "An Integrated Driver With Adaptive Dead-Time Control for GaN-Based Synchronous Buck Converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 2, pp. 539–543, 2022.
[28] GaN Systems Inc., "100V enhancement mode GaN transistor," GS61004B datasheet, Apr. 2020 [Revised Dec. 2021].

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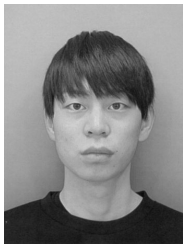

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