

Modeling of Random Telegraph Noise under Circuit Operation - Simulation and Measurement of RTN-induced delay fluctuation

Kyosuke Ito*, Takashi Matsumoto*, Shinichi Nishizawa*, Hiroki Sunagawa*,
Kazutoshi Kobayashi† and Hidetoshi Onodera*‡
*Kyoto University, †Kyoto Institute of Technology, ‡JST, CREST, Japan
{kyosuke_ito, tmatsumoto, onodera}@vlsi.kuee.kyoto-u.ac.jp
kobayasi@kit.ac.jp

Abstract

This paper presents a new model for the statistical analysis of the impact of Random Telegraph Noise (RTN) on circuit delay. This RTN-aware delay model have been developed using Pseudo RTN based on a Markov process with RTN statistical property. We have also measured RTN-induced delay fluctuation using a circuit matrix array fabricated in a 65nm process. Measured results include frequency fluctuations that have power spectrum density of $1/f^2$ property, which clearly indicates the effect of RTN-induced delay fluctuations. From the comparison of the maximum frequency shifts obtained by measurements and simulations, the V_{gs} -dependency of RTN-induced ΔV_{th} attenuates the RTN impact on delay around by half.

1 Introduction

With recent aggressive technology scaling of LSI for power reduction and die shrink, designing reliable systems becomes more challenging. Besides conventional problems such as transistor leakage, degradation and variation of transistor performance have severe impact on the dependability of VLSI systems [1, 2, 3]. In this paper, we deal with Random Telegraph Noise (RTN) which has attracted much attention as a temporal variation enlarged with scaling [4]. It is well known that RTN has a severe impact on CMOS image sensors [5], Flash memories [6], SRAMs [7]. However, the impact of RTN on CMOS logic circuits has not been well addressed. We therefore investigate the impact of RTN on the delay of combinatorial circuits. We have measured RTN-induced delay fluctuation using a circuit matrix array fabricated in a 65nm process, and developed an RTN-aware delay model based on a Markov process with RTN property for the statistical analysis of the impact of RTN on circuit delay. From the statistical data of measured and simulated

RTN-induced delay fluctuation, the impact of RTN under circuit operation is analyzed.

The remainder of this paper is organized as follows. In Section 2, we will show an RTN-aware model based on a Markov process with RTN statistical property. Section 3 shows the evaluation of RTN-induced delay fluctuation on combinatorial circuits from simulation using the RTN-aware model and measurement using a circuit matrix array in 65nm process. Finally, Section 4 summarizes this paper.

2 RTN-aware simulation

In this Section, we explain an RTN-aware delay model based on a Markov process with RTN statistical property. First, we show the distribution of RTN-parameters : the fluctuation of the threshold voltage ΔV_{th} and two time constants of emission time τ_e and capture time τ_c . Next, we describe RTN-aware simulation based on a Markov process with the distribution of measured RTN parameters.

2.1 Statistical property of RTN

A. RTN

As shown in Fig. 1, RTN is a temporal variation in the threshold voltage V_{th} caused by the capture and emission of mobile charge carriers by defects inside the dielectric. In recent reports, the mechanism of RTN is considered as complex of carrier-number fluctuation and mobility fluctuation [8]. RTN-induced ΔV_{th} , the emission time τ_e (averaged time of high V_{th} state) and the capture time τ_c (averaged time of low V_{th} state) are known to vary largely depending on devices [4].

B. Distribution of RTN-induced ΔV_{th}

Fig. 2 shows the statistical property of RTN-induced ΔV_{th} from measurement of 80 nMOSFETs ($W/L = 240$

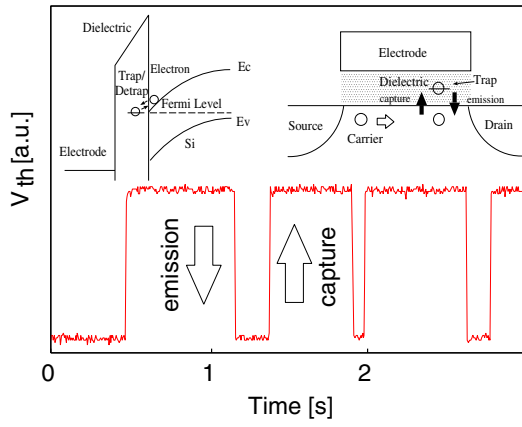


Figure 1. Temporal variation in the threshold voltage caused by the capture and emission of mobile dielectric charge carriers.

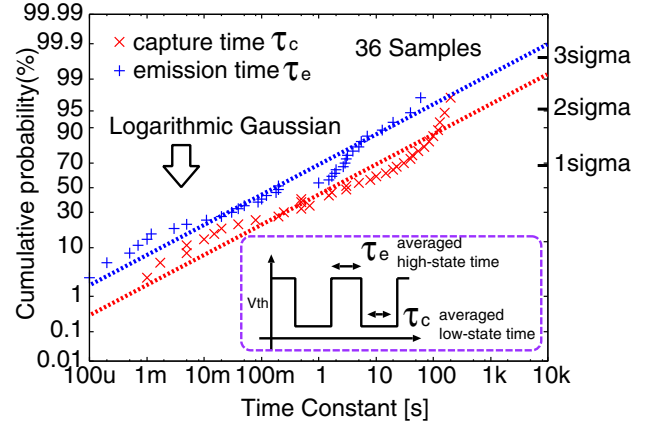


Figure 3. Distribution of time constants (τ_e and τ_c). They have very wide range and can be fitted as a logarithmic Gaussian.

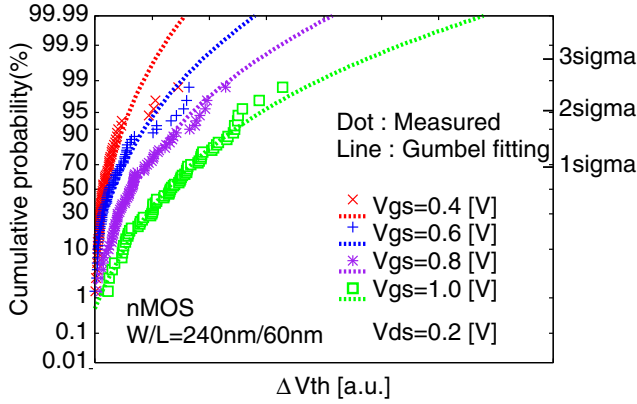


Figure 2. Distribution of RTN-induced ΔV_{th} . The fitting line is Gumbel distribution known as an extreme distribution.

nm/60nm). The long-tailed fitting line has Gumbel distribution known as an extreme distribution [4, 6, 8, 9]. By this property and the size-dependence of ΔV_{th} ($\propto 1/WL$), RTN is believed to be comparable to Random Dopant Fluctuation known as a major source of within die (WID) variation in more scaled technologies [9].

C. Distribution of emission time τ_e and capture time τ_c

Fig. 3 shows the statistical property of the emission time τ_e and the capture time τ_c at $V_{gs}=1.0$ V and $V_{ds}=0.2$ V. As reported in [4, 7], the distribution of time constants can be fitted as a logarithmic Gaussian.

2.2 RTN-aware simulation

To evaluate the impact of RTN on circuit performance, we have developed an RTN-aware model based on a Markov process. In the following, we will show the simulation of pseudo RTN based on a Markov process and an RTN-aware delay model using the pseudo RTN.

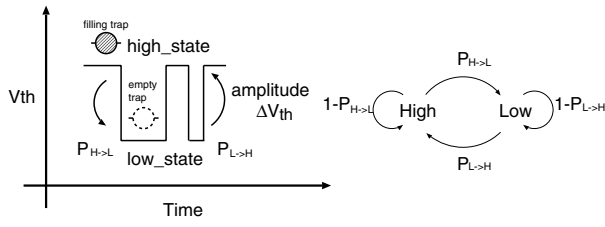
A. Pseudo RTN based on Markov Process

We consider the random behavior of RTN as a Markov process under the assumption that the process of capture/emission does not depend on the history. The algorithm of the pseudo RTN based on a Markov process is shown in Fig. 4. The transition probability P_{LH} (from the emission state (low V_{th}) to the capture state (high V_{th})), P_{HL} (from the capture state to the emission state) and RTN-induced ΔV_{th} are characteristic parameters depending on devices, and the probabilities are calculated from Eqs. (1), (2) with τ_e and τ_c . $T_{duration}$ in Eqs. (1), (2) is the duration considered in the simulation.

$$P_{LH} = 1 - \exp\left(-\frac{T_{duration}}{\tau_c}\right) \quad (1)$$

$$P_{HL} = 1 - \exp\left(-\frac{T_{duration}}{\tau_e}\right) \quad (2)$$

Fig. 5 shows an example of V_{th} fluctuation based on this algorithm. The power spectrum density (PSD) of this fluctuation is shown in Fig. 6. Considering RTN has $1/f^2$ -shaped (Lorentz) PSD in the log-log scale [4], this figure suggests the pseudo-RTN based on a Markov process reconstructs the RTN-behavior. The cutoff angular frequency F_{cutoff} for the PSD of RTN can be calculated from the following equation.



```

double RTN (current_state, P_L→H, P_H→L, high_state, low_state){
  if (current_state==high_state){
    if (Prand(0,1) < P_H→L )
      return low_state;
    else
      return high_state;
  }
  else if (current_state==low_state){
    if (Prand(0,1) < P_L→H )
      return high_state;
    else
      return low_state;
  }
}

```

Figure 4. The algorithm of the Pseudo RTN on the Markov process. P_{LH} , P_{HL} and ΔV_{th} are characteristic parameters depending on devices. Using this algorithm, we simulate RTN-induced fluctuation of V_{th} every one $T_{duration}$.

$$F_{cutoff} = \frac{1}{2\pi} \frac{\tau_e \tau_c}{\tau_e + \tau_c} \quad (3)$$

B. Bias dependence of RTN-induced ΔV_{th} and τ_e, τ_c

As shown in Fig. 2, RTN-induced ΔV_{th} becomes larger as V_{gs} increases. Fig. 7 shows the V_{gs} -dependence of RTN-induced ΔV_{th} at 50% and 3 σ of CDF. To consider the V_{gs} -dependence of ΔV_{th} in the RTN-aware delay model, we have approximated the V_{gs} -dependence of ΔV_{th} as a quadratic function (Fig. 7). Then we have calculated the effective RTN-induced ΔV_{th} from transistor-level circuit simulation with voltage-controlled voltage source describing RTN-induced ΔV_{th} connected to the gate of a transistor.

Another important factor of RTN, τ_e and τ_c , has also the V_{gs} -dependence, and with increasing V_{gs} τ_e increases and τ_c decreases exponentially by the change of the carrier density and the Fermi energy-level (Fig. 8 (a)) [7, 10]. Reference [11] shows the PSD of RTN under circuit operation (AC bias) is decreased by the modulation of τ_e and τ_c due to the V_{gs} -dependence of these two time constants. To consider the modulation effect of τ_e and τ_c under AC bias in our RTN-aware delay model, we set the modulation coefficients $m_c = m_e = m = 10^s$ where the power s is between 0 and 2 randomly, and calculate the “bias-off” state time constants τ_{cOFF} and τ_{eOFF} from Eqs. (4) and (5) with the “bias-on” state time constants τ_{cON} and τ_{eON} (Fig. 8) [11]. Then, as shown in 9, the calculation of the total transition probabilities over the time $T_{durationON}$ and $T_{durationOFF}$ is split into the product of

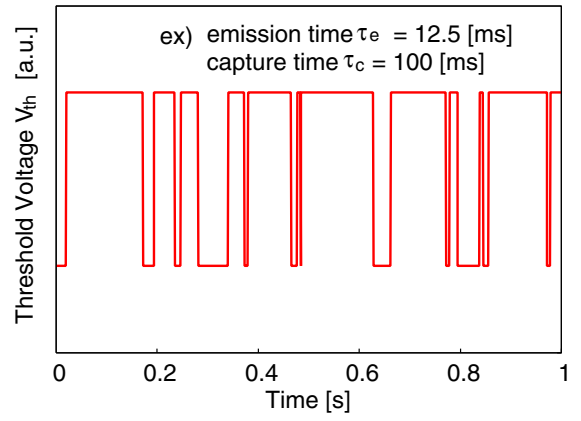


Figure 5. An example of V_{th} fluctuation based on the algorithm shown in Fig. 4.

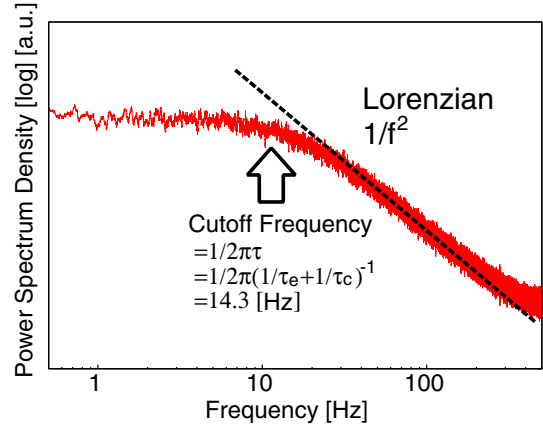


Figure 6. The power spectrum density (PSD) of V_{th} fluctuation shown in Fig. 5. $1/f^2$ -shaped (Lorentz) PSD in the log-log scale is an evidence of the reconstruction of the RTN-behavior.

the transition probabilities for the “bias-off” and “bias-on” periods separately [11].

$$\tau_{cOFF} = \tau_{cON} \times m \quad (4)$$

$$\tau_{eOFF} = \tau_{eON} / m \quad (5)$$

C. RTN-aware delay model

To simulate the impact of RTN on circuit performance using the pseudo RTN based on the Markov process, circuit delay variation is linearly approximated using variable parameters (ΔV_{th} and ΔL) and their sensitivity coefficients ($K_{V_{th}}$ and K_L) of each MOSFET in the following eq. (6). The sensitivity coefficient is calculated from transistor-level simulation. This equation represents the delay fluctuation of combinatorial circuit with temporal variability of ΔV_{th} due to RTN

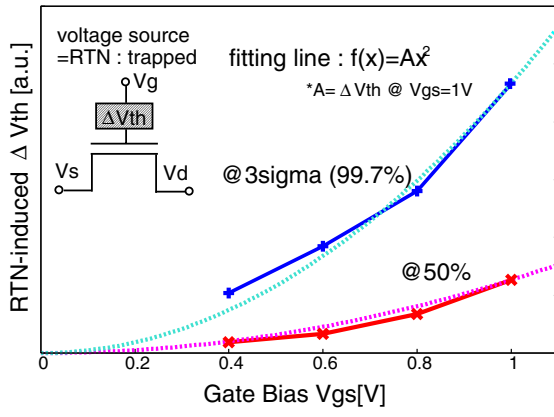


Figure 7. The V_{gs} -dependence of RTN-induced ΔV_{th} at 50% and 3 sigma of CDF. In this paper, we have approximated the V_{gs} -dependence of ΔV_{th} as a quadratic function, and evaluated the impact of ΔV_{th} considered V_{gs} -dependence from transistor-level simulation with voltage-controlled voltage source which has a quadratic control function.

as well as static variability of ΔV_{th} and ΔL due to within die variability.

$$\Delta T = \sum_i (K_{V_{th}i} \Delta V_{thi} + K_{L_i} \Delta L_i) \quad (6)$$

To use the RTN-aware delay model, we assume the following points.

1. The RTN-parameters (ΔV_{th} , τ_e and τ_c) depend on devices, and their distributions are determined device by device.
2. All MOSFETs have two-state RTN by a single trap. ΔV_{th} of nMOSFET has a Gumbel-distribution shown in Fig. 2 and ΔV_{th} of pMOSFET is three times as large as that of nMOSFET [8]. Distributions of the time constants (τ_{eON} and τ_{cON}) are logarithmic Gaussian shown in Fig. 3.
3. As explained in section 2-2-B, RTN-induced ΔV_{th} is weighted by a parameter calculated from transistor-level simulation in order to consider the V_{gs} -dependence of ΔV_{th} . And, we set $T_{durationON} = T_{durationOFF} =$ a half period of a target circuit, which is a 7-stage ring oscillator.
4. WID variation-induced ΔV_{th} and ΔL are Gaussian and extracted by the method discussed in [12].

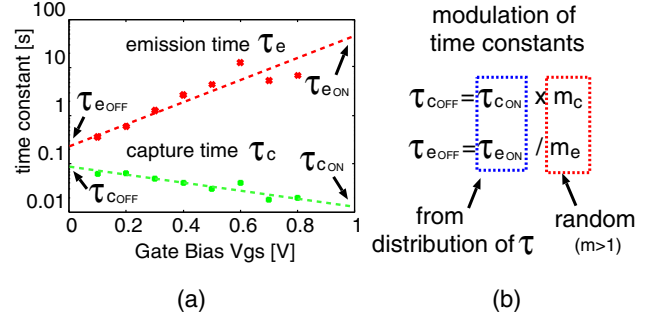


Figure 8. (a) The example of V_{gs} -dependence of τ_e and τ_c . With increasing V_{gs} τ_e increases and τ_c decreases exponentially. (b) Calculation of the “bias-off” state time constants τ_{cOFF} and τ_{eOFF} from the “bias-on” state time constants τ_{cON} and τ_{eON} . In this paper, we set the modulation coefficients $m_c = m_e$.

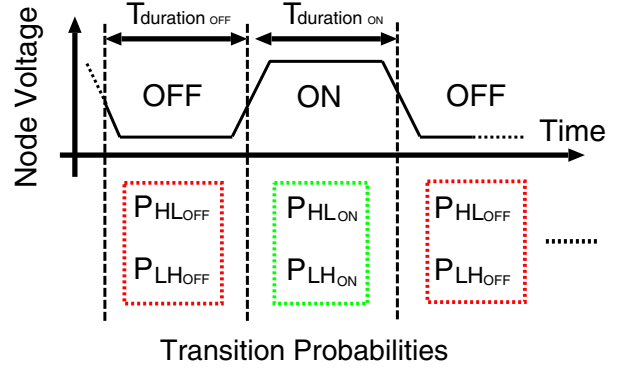


Figure 9. Transition probabilities on periodically cycled gate bias. P_{ON} (P_{HLON} , P_{LHON}) is calculated from Eqs. (1) and (2) with τ_{ON} (τ_{cON} , τ_{eON}).

3 Results and Discussion

3.1 Measurement of RTN-induced Delay Fluctuation

A. Test Circuit Structure

Fig. 10 shows the test structure fabricated in a 65nm CMOS technology for RTN induced delay fluctuation measurement. The circuit matrix array contains 20×15 identical sections and each section is constructed by 7-stage, 13-stage, 19-stage, 29-stage, and 59-stage ring oscillators. Ring oscillators are connected to dividers as shown in Fig. 11. In the test structure, we select 7-stage ring oscillators as a representative of combinatorial circuits. The frequency of RO is varied by changing power supply (VDD_{RO}), and the output of RO is connected to the clock of the D-FF through one inverter constructing a frequency divider as shown in Fig. 11. The power supply of the D-FF

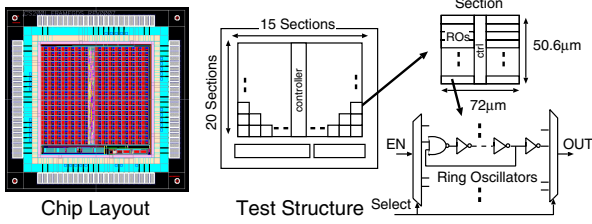


Figure 10. Test structure for process variation and RTN-induced delay fluctuation measurement in 65nm CMOS technology.

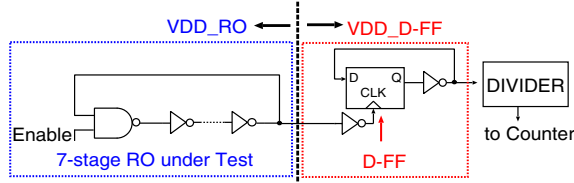


Figure 11. With test circuit consisted of Ring Oscillator (RO) and Divider (D-FF), the impact of process variation and RTN on digital circuits can be evaluated.

(VDD_{D-FF}) can also be varied. In this experiment, we measure the fluctuation of oscillation frequencies for 250 s by counting oscillation counts over 20 ms at room temperature. Supply voltages VDD_{RO} and VDD_{D-FF} are set to 1.0 V and 1.2 V.

B. Power Spectrum Density of Measured Frequency Fluctuation

Considering the source of $1/f$ noise is superposition of multiple RTN [10], the PSD of the frequency fluctuation of a 7-stage ring oscillator consisting of 18 MOSFETs is found to be well represented by $1/f^s$ where the power s is between 1 and 2.

Fig. 12 shows 2 examples of measured frequency fluctuation out of 300 samples. Since the PSD of measured frequency fluctuation is $1/f^2$ -shaped or $1/f$ -shaped, frequency fluctuations are believed to be caused by RTN. The increase of VDD_{D-FF} has no influence on frequency fluctuation. This confirms that the frequency fluctuation is caused by the phase-noise of the ring oscillator due to RTN.

3.2 Distributions of Simulated and Measured Frequency Fluctuations

We have measured the maximum frequency shift caused by RTN over measurement time of 250s. The maximum frequency shift has been also simulated by the proposed RTN-aware delay modeling. In this simulation, we considered V_{gs} -dependencies of RTN-induced ΔV_{th} and time constants τ_e and τ_c . Distributions of the maximum frequency

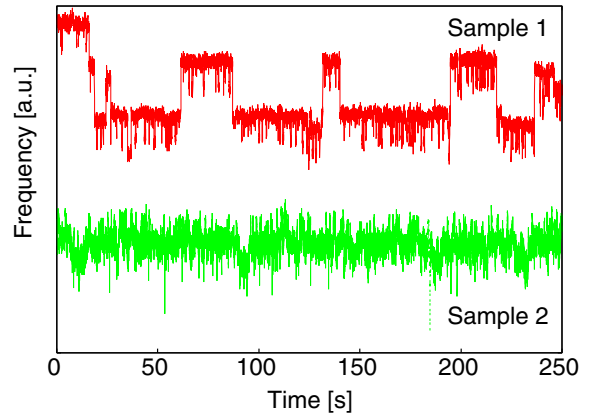


Figure 12. Two examples of measured RTN-induced frequency fluctuation.

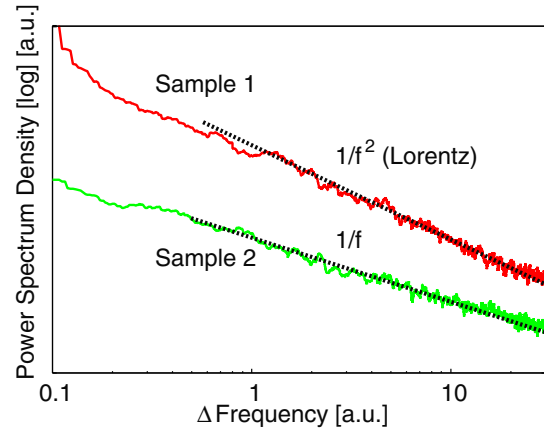


Figure 13. PSD of RTN-induced frequency fluctuations shown in Fig. 12. Frequency fluctuations are believed to be caused by RTN because these PSD of them show $1/f^2$ -shaped (Lorentz) and $1/f$ -shaped.

shifts obtained by measurements (300 samples) and simulations (10,000 samples) are shown in Fig. 14. The simulation overestimates frequency fluctuation more than two times. Possible reasons for this discrepancy include inaccuracy in the modeling and extraction of statistical properties of RTN-parameters. Further investigation is underway.

For reference, the maximum frequency shift has been simulated without any V_{gs} -dependencies of RTN-induced ΔV_{th} and time constants τ_e and τ_c , and also without the V_{gs} -dependencies of RTN-induced ΔV_{th} but with that of τ_e and τ_c . Distributions of those results are also shown in Fig. 14. Those results are about four times larger than the measured distribution. The V_{gs} -dependency of time constants τ_e and τ_c does not have large impact on the frequency shift, whereas the V_{gs} -dependency of RTN-induced ΔV_{th} does. In our simulation, the V_{gs} -dependency of RTN-induced ΔV_{th} attenuates the RTN impact on delay by half.

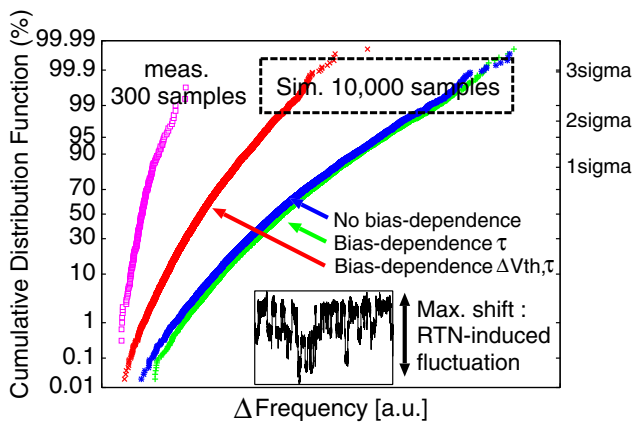


Figure 14. Distribution of measured RTN-induced frequency fluctuation and simulated one considered the bias-dependence of ΔV_{th} and τ_e, τ_c .

4. Conclusion

A new delay model for the statistical analysis of the impact of RTN on circuit delay using Pseudo RTN based on a Markov process with RTN statistical property has been proposed. We have also measured RTN-induced delay fluctuations using a circuit matrix array fabricated in a 65nm process. From measured and simulated delay fluctuation data, we indicate the V_{gs} -dependence of RTN-induced ΔV_{th} has considerable effects on the large attenuation of RTN under circuit operation.

5. Acknowledgment

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References

- [1] S. Borkar. Designing reliable systems from unreliable components: the challenges of transistor variability and degradation. *Micro, IEEE*, Vol. 25, No. 6, pp. 10 – 16, nov. 2005.
- [2] S. Mahapatra and M.A. Alam. Defect generation in p-mosfets under negative-bias stress: An experimental perspective. *Device and Materials Reliability, IEEE Transactions on*, Vol. 8, No. 1, pp. 35 –46, mar. 2008.
- [3] H. Onodera. Variability modeling and impact on design. *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pp. 1 –4, dec. 2008.
- [4] N. Tega, H. Miki, T. Osabe, A. Kotabe, K. Otsuga, H. Kurata, S. Kamohara, K. Tokami, Y. Ikeda, and R. Yamada. Anomalously large threshold voltage fluctuation by complex random telegraph signal in floating gate flash memory. In *Electron Devices Meeting, 2006. IEDM '06. International*, pp. 1 –4, 11-13 2006.
- [5] Jun-Myung Woo, Hong-Hyun Park, Hong Shick Min, Young June Park, Sung-Min Hong, and Chan Hyeong Park. Statistical analysis of random telegraph noise in cmos image sensors. In *Simulation of Semiconductor Processes and Devices, 2008. SISPAD 2008. International Conference on*, pp. 77 –80, 9-11 2008.
- [6] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya. Random telegraph signal in flash memory: Its impact on scaling of multilevel flash memory beyond the 90-nm node. *Solid-State Circuits, IEEE Journal of*, Vol. 42, No. 6, pp. 1362–1369, jun. 2007.
- [7] M. Tanizawa, S. Ohbayashi, T. Okagaki, K. Sonoda, K. Eikyu, Y. Hirano, K. Ishikawa, O. Tsuchiya, and Y. Inoue. Application of a statistical compact model for random telegraph noise to scaled-sram vmin analysis. In *VLSI Technology, 2010 Symposium on*, pp. 95 –96, 16-18 2010.
- [8] N. Tega, H. Miki, M. Yamaoka, H. Kume, Toshiyuki Mine, T. Ishida, Yuki Mori, R. Yamada, and Kazuyoshi Torii. Impact of threshold voltage fluctuation due to random telegraph noise on scaled-down sram. In *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, pp. 541 –546, apr. 2008.
- [9] N. Tega, H. Miki, F. Pagette, D.J. Frank, A. Ray, M.J. Rooks, W. Haensch, and K. Torii. Increasing threshold voltage variation due to random telegraph noise in fets as gate lengths scale to 20 nm. In *VLSI Technology, 2009 Symposium on*, pp. 50 –51, 16-18 2009.
- [10] M. J. Kirton and M. J. Uren. Noise in solid-state microstructures: a new perspective on individual defects, interface states, and low-frequency noise. *Advances in Physics*, Vol. 38, No. 4, pp. 367–468, jul. 1989.
- [11] A.P. van der Wel, E.A.M. Klumperink, L.K.J. Vandamme, and B. Nauta. Modeling random telegraph noise under switched bias conditions using cyclostationary rts noise. *Electron Devices, IEEE Transactions on*, Vol. 50, No. 5, pp. 1378 – 1384, may. 2003.
- [12] S. Nishizawa and H. Onodera. Variability characterization using an ro-array test structure and its impact on design. *DFM&Y Workshop*, jun. 2010.