Effect of Regularity-Enhanced Layout on Printability and Circuit Performance of Standard Cells

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Abstract— As the minimum feature size shrinks down far below sub-wavelength, Restricted Design Rule(RDR) or layout regularity plays an important role for maintaining pattern fidelity in photo lithography. However, it also incurs overheads in layout area and circuit performances. Therefore it is important to find an appropriate level of regularity that gives the best trade-off among manufacturability, cost, and performance for each process technology. This paper discusses the effect of layout regularity on printability and circuit performance in 90–45nm processes by lithography simulation and real chip measurement. It is shown that we can focus more on circuit performance with less on layout regularity in a 90nm process while adequate amount of regularity is imperative for ensuring proper amount of lithographic process windows in a 45nm process. We demonstrate the quantitative evaluation of the trade-off between printability and circuit performance of regularity-enhanced standard cells.

Keywords— DFM, Standard Cell, Layout Regularity, Variability, Performance

I. Introduction

Technology scaling of LSI has been a basic principle for speed improvement, power reduction and die-size shrink. However in sub-100nm era, a number of difficulties arise in performance variability and manufacturability. In the past, there was a clear separation between manufacturing side and design side with a set of design rules as an interface. The manufacturing side has been making an effort to suppress variability and improve yield. However in sub-100nm era, the design side also has to take manufacturability into consideration. The effort from the designer side, called Design For Manufacturability(DFM), is becoming more important [1–3]. One of the techniques to enhance manufacturability by improving printability in a lithographic process is to employ regularity into physical layout [4,5]. Regularity-enhanced design is friendly to photolithography. However, design restriction associated with regularity reduces design flexibility and requires extra features such as dummy patterns. From a viewpoint of the circuit performance, regularity-enhanced design has negative impact since extra features require extra area and dummy patterns increase parasitic capacitance. Therefore designers should consider the trade-off between the advantage in printability and the disadvantage in circuit performance.

In this paper, we discuss the trade-off between printability and circuit performance. There are several techniques to improve layout regularity in standard cells. We design standard cells with different levels of regularity. To observe the effect of technology scaling, we evaluate the printability and the circuit performance in 90nm, 65nm and 45nm processes. The printability is evaluated by a photolithography simulation, and the circuit performance is evaluated be a transistor level circuit simulator. Also in a 90nm process, we have fabricated test structures that consist of an array of ring oscillators with different layout regularities. A regularity-enhanced standard cell with dummy poly insertion does reduce performance variability. However, the amount of the improvement is moderate, and, more importantly, noticeable amount of performance overhead is observed, which means that this level of regularity does not pay off in the 90nm process. In a 65nm process, layout regularity also helps to suppress performance variability while it incurs performance penalty of 4% speed loss in a ring oscillator circuit estimated by lithography and circuit simulations. In a 45nm process, on the other hand, certain level of regularity is indispensable for ensuring printability under adequate amount of lithographic process windows. From those experimental results, as the technology scaling progresses, the required level of regularity becomes ramping up steeply. It is important to evaluate the minimum amount of layout regularity that is necessary for securing required level of printability. The contribution of this paper is to illustrate the trade-off between printability and circuit performance quantitatively.

Section II introduces fundamentals of regularity-aware design. The latter part shows experimental results. First, Section III illustrates the measurement results in a 90nm process. Section IV and Section V show simulation results in a 65nm process and a 45nm process, respectively. Section VI concludes the discussion.

II. Issues in Deep Sub-Wavelength Lithography and Layout Regularity Enhancement

In this section, we explain Optical Proximity Correction(OPC) for deep sub-wavelength lithography, and the effect of layout regularity on printability.

A. Optical Proximity Correction

It is difficult in principle to print a feature smaller than the photolithographic wavelength. Edge placement errors because of interference and diffraction, etc, that is called OPE(Optical Proximity Effect), are becoming more seri-

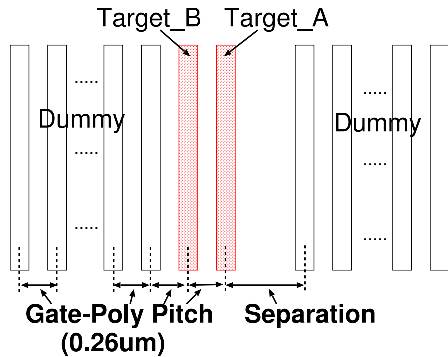

Fig. 1. Test pattern to evaluate the effect of gate poly pitch.

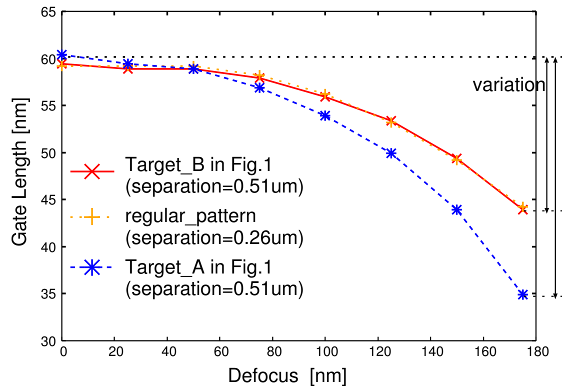

Fig. 2. Simulation results of the effect of pitch irregularity.

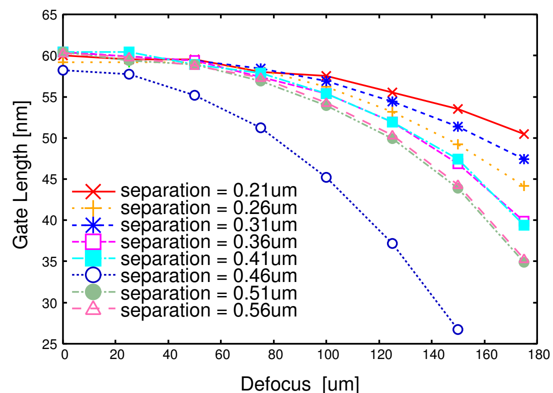

Fig. 3. Simulated gate width of the pattern that faces the separation under different separation length.

ous. The method of mask preparation for correcting OPE is called OPC(Optical Proximity Correction). In sub-100nm era, OPC is indispensable. The complexity of OPC processing and the amount of mask data after OPC increase explosively as technology goes into deep sub-wavelength region. Also, the ability of pattern collection becomes decrease. It is expected that the reduction of layout complexity by introducing regularity is one of essential methods for ensuring printability while maximally exploiting OPC.

B. Regularity-Enhanced Layout

Introduction of layout regularity can be an effective method for improving printability. In this paper, we focus on the layout regularity of polysilicon patterns that has the primal effect on transistor performance. For the enhancement of polysilicon patterns, we consider arranging them in a single pitch and removing jogs. Those effects are discussed in the following paragraphs.

Effect of Gate Pitch

Single gate pitch is favorable in many manufacturing stages. We show that the pitch of gate forming polysilicon has a direct effect on gate length variation.

Using a test structure shown in Fig. 1, we examine the effect of irregular pitch by lithography simulation in a 65nm process [6]. There are two groups of arrayed polysilicon patterns with the contacted pitch of 0.26μm. First, setting the separation of two groups to the contacted pitch, we evaluate the gate length of the single pitch pattern as a function of defocus by lithography simulations. We then set the separation to 0.51μm and evaluate the effect of the pitch-break. The gate length of Target_A and Target_B are simulated as functions of defocus. Fig. 2 shows the result. As the amount of defocus increases, the gate length gradually decreases. Thanks to the OPC, the gate length of the uniform pattern and that of Target_B are almost identical. However, the gate length of Target_A at the edge of the group exhibits larger fluctuation which indicates degradation in susceptibility to defocus. Next, we evaluate the effect of separation length on the gate length of Pattern_A. Fig. 3 shows the gate length of Pattern_A as a function of defocus with several values of the separation. When the separation is less than 0.36μm, the gate length variation is smaller than the case of the single pitch (separation = 0.26μm). However, when the separation is greater than 0.36μm, the gate length variation increases rapidly with the defocus. It can be seen that pattern pitch has a direct effect on printability and regular pitch is effective for enhancing manufacuturability.

Effect of Poly Jog

The width of printed polysilicon patterns, especially at jogs and line ends, is susceptible to variation. If these patterns exist on or near diffusion area, the variability of the poly-pattern directly leads to gate length variation. It is therefore effective to remove jogs and spots where pattern width changes and to keep these spots as far away from diffusion.

III. Measurement in a 90nm Process

In this section, we show measurement results in a 90nm process. Three types of standard cells with different levels of regularity are designed. These cells are embedded in an array of ring oscillators. From measured oscillation frequencies and their variances, we can evaluate the effect of regularity on the performance and its variance of the circuit.

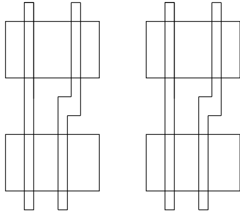

Fig. 4. Layout of NAND2-jog

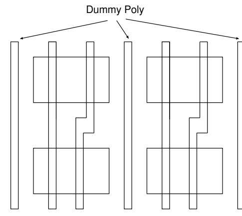

Fig. 5. Layout of NAND2-jogdum

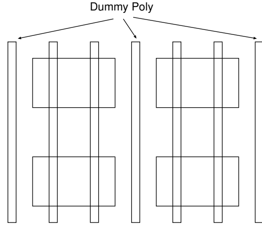

Fig. 6. Layout of NAND2-regular

A. NAND2 with Different Layout Regularity

We introduce three layouts of a two-input NAND gate. To evaluate the effect of regularity, each layout is configured as follows.

NAND2-jog(Fig. 4)

In this cell, no design restriction for regularity is employed. Gate pitch is irregular and jogs are allowed with minimized diffusion area.

NAND2-jogdum(Fig. 5)

In this cell, dummy polysilicons are inserted so that poly gates of PMOS transistors have a single pitch. Dummy polysilicons are expected to improve printability, although they increase parasitic capacitance.

NAND2-regular(Fig. 6)

In this cell, all the pitches of polysilicon patterns are designed to be identical. Dummy polysilicons are used and the jog of the polysilicon is prohibited.

B. Chip Fabrication

We have designed a test structure for variability characterization in a 90nm process. Figs. 7 shows the layout structure of the test chip. The chip contains two arrays of 15 by 15 tiles, occupying a 1.3 × 1.2 mm^2 area. Each tile includes 22 ring oscillators including three 19-stage NAND2 oscillators with different levels of regularity shown in Figs. 4 – 6. Therefore, 450 identical ring oscillators are placed regularly on a chip. In this paper, we write RO-jog, RO-jogdum and RO-regular as the ring oscillator made by NAND2-jog, NAND2-jogdum and NAND2-regular, respectively.

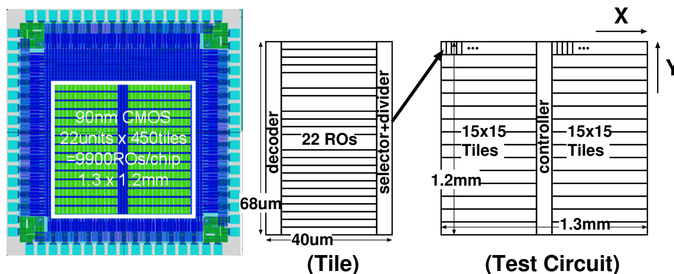

Fig. 7. Layout Screenshot of a Chip and Conceptual Layout of a Chip

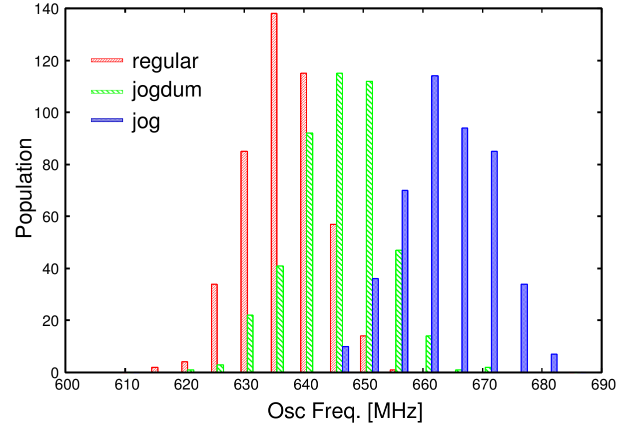

Fig. 8. Distribution of oscillation frequency

TABLE I
WID and D2D Variations of Oscillation Frequencies (Chip#1)

RO-type	jog	jogdum	regular
WID-μ[MHz]	660.1	642.6	633.7
WID-σ[MHz]	7.5	7.5	6.3
D2D-μ[MHz]	653.4	637.9	622.6
D2D-σ[MHz]	20.2	19.4	19.1

C. Experimental Results

We have measured 37 chips taken from a wafer. From the distribution of 450 oscillation frequencies for a chip, we can evaluate within-die(WID) variability. From the distribution of 37 mean oscillation frequencies for each chip, we can obtain die-to-die(D2D) variability.

Fig. 8 shows an example of the distribution of WID oscillation frequencies for RO-jog, RO-jogdum and RO-regular circuits. Table I compares the amount of within-die(WID) variation and die-to-die(D2D) variation for the three circuits. The standard deviation (σ) of RO-regular is 16% smaller than that of RO-jog. However, the mean frequency (μ) of RO-regular is 4.0% smaller than that of RO-jog. RO-jogdum does not improve the standard deviation, whereas degrades the oscillation frequency by 2.7%. As shown in Fig. 8, the strong regularity of single pitch enforcement with dummy insertion has negative effect on the performance while reducing the variability moderately. It means that, in 90nm process, the strong level of regularity is not necessary.

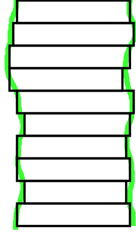

Fig. 9. approximate model of gate

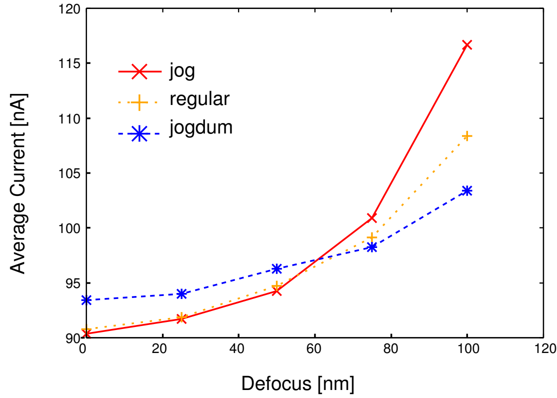

Fig. 10. Leakage of PMOS of two-input NAND

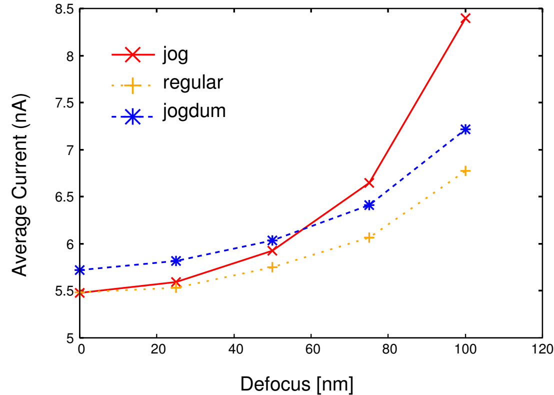

Fig. 11. Leakage of NMOS of two-input NAND

IV. Evaluation in a 65nm process

From Section III, the performance overhead of regularity-enhanced cells are noticeable and the regularity is less effective in the 90nm process. In this section, we evaluate regularity-enhanced cells in a 65nm process by lithography and circuit simulation.

A. Evaluation by Lithography Simulation

To discuss the effect of layout regularity, we evaluate the printability by a lithography simulation.

Simulation Setup

It is not favorable to do lithography simulation only one cell separately, because exposed cells could be affected by the neighboring pattern. In the lithography simulation, we make an array of cells in a 3×3 matrix, and evaluate the center cell after exposure. We use the average leakage current of each P/N transistors of NAND2 as evaluation measures. Leakage current is appropriate to evaluate gate length variation since it increase exponentially according to the inverse of gate length.

Generally, an edge of a printed pattern fluctuates according to its own and surrounding layouts, and therefore gate length varies inside a transistor. In leakage current calculation, we approximate the transistor under evaluation as a collection of small transistors as shown in Fig. 9 [7]. We estimate the amount of leakage current as a function of defocus. When the fluctuation of gate length reaches to ±15%, we assume that hotspots (pattern degradations) have arisen, and it is impossible to fabricate correct patterns.

Results of Lithography Simulation

Figs. 10 and 11 show the leakage current of PMOS and NMOS transistors respectively. NAND2-jogdum have hotspots above the defocus of 75 nm. Hotspots of NAND2-jog and NAND2-regular arise at the defocus of 100 nm. Leakage current increases in accordance with the defocus because the gate length decreases as indicated in Figs. 2 and 3. The increased leakage currents of NAND2-regular and NAND2-jogdum are less than that of NAND2-jog. For example, at the defocus of 100 nm, PMOS leakage current of NAND2-regular is about 20% smaller than that of NAND2-jog. That of NAND2-jogdum is almost the same as that of NAND2-regular, because the gate poly is very close to the nearby polys. However the pattern of NAND2-jogdum has a difficulty in printability even with strong OPC. From these results, we verify that regularity improves printability and robustness to defocus in the 65nm process, although the effect is not remarkable.

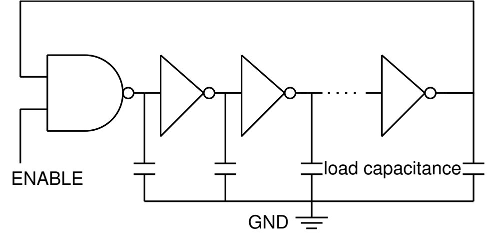

Fig. 12. Concept of ring oscillator circuit considering load capacitance

B. Effect on Circuit Performance

Delay of regularity-enhanced cells may increase due to the parasitic capacitance. Circuit performance degradation negates the merit of technology scaling down. Dummy poly insertion introduces two types of parasitic capacitance; between dummy and nearby poly, between dummy and ground. We estimate how these capacitances influence circuit performance.

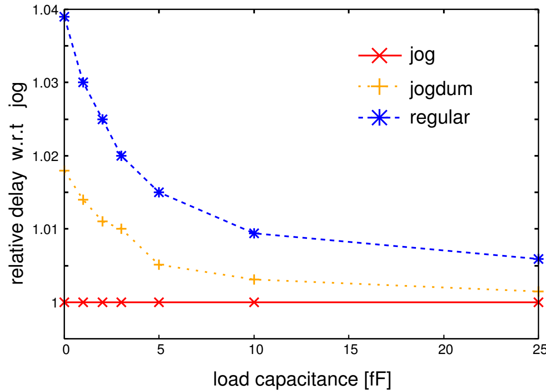

Fig. 13. RO simulation considering parasitic capacitance

Simulation Setup

We obtain the circuit delay from a 19-stage Ring-Oscillator(RO) simulation using NAND2 in Sec.III-A. We extract a netlist with parasitics from the Ring-Oscillator(RO) array layout. Moreover, a load capacitance is added to each stage in the RO (Fig. 12)that represents an output loading appears in an actual circuit. We simulate the delay of each circuit as a function of load capacitance. The delay is normalized to that of NAND2-jog which is the fastest circuit with the least parasitics.

Results of Circuit Simulation

Fig. 13 shows the simulated delay as a function of load capacitance. The performance of NAND2-jogdum RO degrades 2% in maximum and that of NAND2-regular RO degrades 4% in maximum when no load capacitance is added. In other words, inserting dummy increases delay by 2% and diffusion area expansion increases delay by 2%. In a real circuit other than ROs, each gate would drive more than a single gate. In this process, for example, fan-out of four corresponds to 5 fF. In that case, performance overhead of NAND2-jogdum and NAND2-regular decreases to 1.5% and 0.5%, respectively.

From the discussion above, the regularity is effective to improve printability. Thus the regularity-enhanced cell is a design option in this 65nm process.

V. Regularity-Enhanced Design in a 45nm Process and Beyond

From the discussion in the previous section, the regularity-enhanced cells are effective to improve printability in the 65nm process. This section focuses on more advanced process. We evaluate the relationship between printability and circuit performance in a 45nm process.

A. D-Flip-Flop (D-FF) with Different Layout Regularity

The layout under investigation is a D-Flip-Flop (D-FF), because, in general, the total size and power consumption of D-FFs in a chip account for more than 30% of the whole circuit in our experience. Also, it has a complex layout and therefore it is adequate to use as a test vehicle for evaluating the effect of layout regularity.

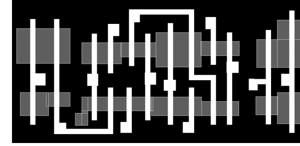
Fig. 14. Layout of DFF-standard

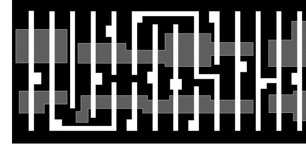
Fig. 15. Layout of DFF-regular

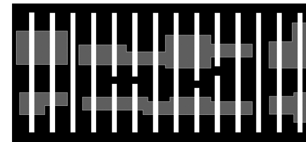
Fig. 16. Layout of DFF-ultra-reg

We have designed three DFF layouts with different levels of regularity. These three layouts are designed under design rules of a 90nm process with a few exception for the third layout, and converted to a 45 nm process by shrinking all geometry to half. Then OPC/Lithography simulation is conducted using an optical model for the 45nm process.

DFF-standard(Fig. 14)

It is a conventional design of D-FF for a 90nm process. It is designed to minimize area. Dense gate poly results in irregular pitches with less regularity.

DFF-regular(Fig. 15)

It contains single-pitched poly patterns only. Its layout has a moderate level of regularity. It has 8% larger area than DFF-standard and contains 8 vias in a cell. Minimum number of Metal 2 wires are used for completing within-cell routing.

DFF-ultra-reg (Fig. 16)

In this layout, polysilicon patterns has a single pitch and a single orientation, by eliminating jogs and also by removing contact-enclosures which could be achievable in a 45nm process. It has 8% larger area than DFF-standard and contains 16 vias in a cell. It maintain high level of regularity for polysilicon patterns but Metal 2 wires are widely used in a cell for completing within-cell routing.

B. Lithography Simulation

In this lithography simulation, we evaluate the effect of regularity by the gate- length variation. We calculate the average gate-length of 24 transistors in the cell, and obtain mean and standard deviation. At the same time we calculate standard deviation of gate-length within each transistor (σ-WIT). When the fluctuation of gate-length inside a

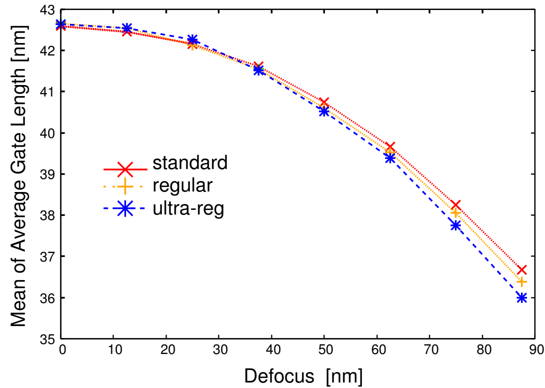

Fig. 17. Mean of average gate-length of each transistor

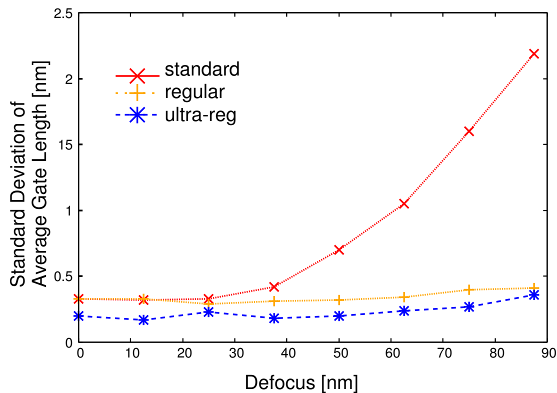

Fig. 18. Standard deviation of average gate-length of each transistor

transistor reaches to ±20%, we assume that a hotspot is generqated.

C. Simulation Results

Figs. 17 and 18 show the mean and the standard deviation of the average gate-length of each transistor, respectively. Fig. 19 shows the mean of the standard deviation of the gate-length inside each transistor. From Fig. 17, the average gate-length decreases with the increase in defocus. The three layouts show similar variability for the average gate-length. However, hotspots of D-FF-standard are generated at the defocus of 25nm. On the other hand, hotspots of D-FF-regular and D-FF-ultra-reg are generated at the defocus of 62.5nm and 87.5nm, respectively. Also, the standard deviation of the average gate-length(Fig. 18) as well as the gate-length fluctuation inside a transistor(Fig. 19) show rapid increase in variability as the amount of defocus grows. We can clearly see that layout regularity greatly enhances pattern fidelity. A complex layout which is popular in a 90nm process cannot have an enough process window in the 45nm process. We need a moderate regularity similar to DFF-regular for this technology node.

VI. Conclusion

In this paper, we evaluate the effect of regularity on printability and circuit performance by simulation and

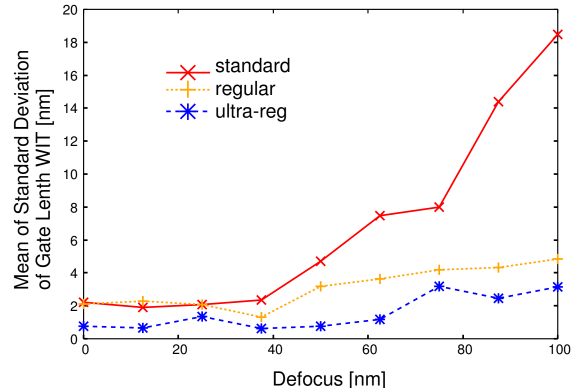

Fig. 19. Mean of standard deviation of gate-length within transistor (mean of σ-WIT)

test-chip measurements. In the case that the regularity-enhanced cells are used in a 90nm test chip, the frequency decreases by 4.0% in maximum, and the standard deviation improves about 16%. From this results, the merit of regularity is little at the 90nm technology nodes. However regularity-enhanced design is becoming more important around the 65nm process. In the 65nm process, a lithography simulation shows that leakage current of a regularity-enhanced two-input NAND decreases 20% in maximum under 100nm defocus condition. A circuit simulatioin, cosidering parasitics, also shows that its freqency decreases by 4% in maximum. In the 45nm process, there is a strong requirement for regularity-enhanced design and moderate level of regularity is required. From the results of a lithography simulation, regularity-enhanced design clearly improves pattern fidelity. At the same time, regularity enforcement may affect interconnect flexibility and increases in area. We must therefore derive the adequate level of regularity for each technology node considering overall manufacturability, cost, and performance overhead.

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