# Radiation Hardened Flip-Flops with low Area, Delay and Power Overheads in a 65 nm bulk process

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***Abstract*—We propose two types of radiation-hard flip-flops named PLTGFF and FBTIFF with low ADP (area, delay and power) overheads by increasing critical charge ($Q_{\rm crit}$) at weak nodes. They have additional transistors and wires. PLTGFF has the area, delay, and power overheads by 5%, 4%, and 10%, respectively. FBTIFF has the area, delay, and power overheads by 42%, 10%, and 22%, respectively. They were fabricated in a 65 nm bulk process. $\alpha$-particle irradiation tests revealed that $\alpha$-SERs of PLTGFF and FBTIFF were suppressed by 45% and by 90% than that of STDFF. By spallation neutron irradiation tests, neutron-SERs of PLTGFF and FBTIFF were suppressed by 18% and by 35% than that of STDFF. In the terrestrial environment, the proposed FFs have better trade-offs between reliability and performance than these of multiplexed FFs with large overheads.**

***Index Terms*—soft error, Single Event Upset (SEU), $\alpha$ particle, neutron, flip-flop**

## I. INTRODUCTION

Reliability issues such as radiation-induced soft errors become more serious with technology down scaling [1]. Soft errors are one of the temporal failures that upset stored values in storage elements such as flip-flops (FFs) or SRAMs caused by a radiation strike. To improve the soft error tolerance of storage elements, several redundant circuits such as triple modular redundancy (TMR) [2] and the dual interlocked storage cell (DICE) [3] [4] have been proposed. However the number of transistors of these FFs is significantly larger than that of a standard FF, and the performance overhead is large. These FFs may not be optimal for some applications. For example, due to higher radiation flux in outer space than in the terrestrial environment, storage-cell multiplication is an effective countermeasure in space. In the terrestrial environment, however, the possibility of soft errors is much lower than space. Thus multiplication is sometimes excessive. Therefore, it is necessary to take countermeasures to bring a balance between soft error tolerance and circuit performance.

In the terrestrial environment, $\alpha$-particles and neutrons induce soft errors. In this paper, we proposed two types of radiation-hardened FFs named PLTGFF and FBTIFF with low performance overheads by increasing the critical charge ($Q_{\rm crit}$). Area, delay, and power of PLTGFF and FBTIFF were higher than those of the standard FF (STDFF), respectively. However, these overheads are much smaller than DICEFF. TCAD simulations show that the threshold linear energy transfers (LET) increase at every node. We revealed that the proposed FFs have high soft error tolerance caused by $\alpha$-particles and high energy neutrons.

## II. RADIATION-HARDENED FLIP-FLOPS

### A. Proposed Radiation-hardened Flip-Flops

Fig. 1 shows the STDFF without any radiation hardness.

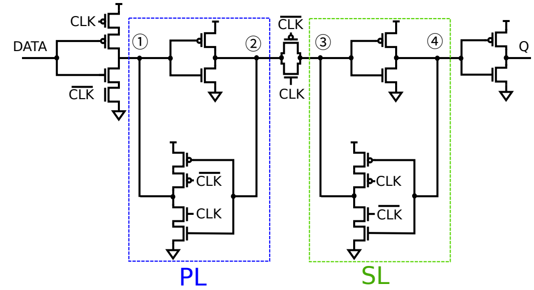


Fig. 1: STDFF (Standard FF)

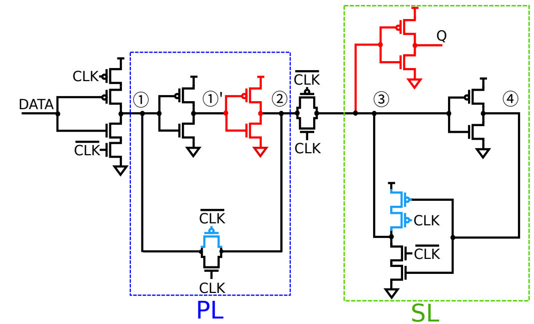


Fig. 2: PLTGFF (Primary Latch Transmission Gate FF). The gate width of the blue PMOS transistors are doubled.

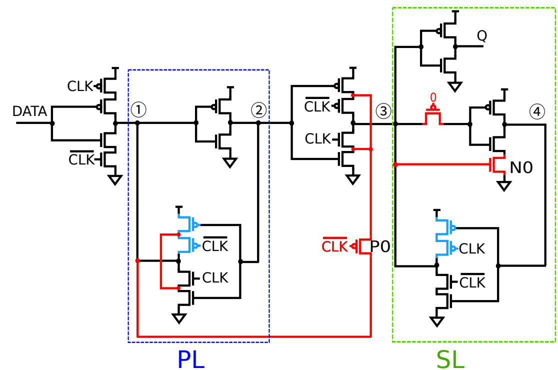


Fig. 3: FBTIFF (Feed-Back Tristate Inverter FF). The gate width of the blue PMOS transistors are doubled.

The proposed circuit structures, PLTGFF and FBTIFF, are shown in Figs. 2 and 3. We focus on $Q_{\rm crit}$ calculated by circuit simulations. Soft errors occur due to electrons in NMOS and

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TABLE I: Node numbers to evaluate Qcrit in all four (Q, CLK) states.

| (Q, CLK) | STDFF | PLTGFF | FBTIFF |
|---|---|---|---|
| (0, 1) | ① | ① ② | ① |
| (1, 1) | ② | ①' | ② |
| (1, 0) | ③ | ④ | ④ |
| (0, 0) | ④ | ③ | ③ |

TABLE II: $Q_{\mathrm{crit}}$ of nodes in the standard and proposed FFs

| Circuit structure | $Q_{\mathrm{crit}}$ [fC] | | | | |
|---|---|---|---|---|---|
| | ① | ①' | ② | ③ | ④ |
| STDFF | 3.7 | - | 11 | 3.0 | 8.5 |
| PLTGFF | 5.7(+2.0) | 8.9 | 14(+3.0) | 4.6(+1.6) | 8.7(+0.2) |
| FBTIFF | 8.9(+5.2) | - | 9.4(-1.8) | 20(+17) | 17(+8.5) |

holes in PMOS. Soft errors are likely to occur in NMOS because the mobility of electrons is larger than the that of holes [5].

Therefore, we considered countermeasures to increase the $Q_{\mathrm{crit}}$ on NMOS. The current source used for the simulation is the single exponential model in Eq. (1) [5]. $T$ in Eq. (1) refers to the time constant determined by a process node. $T$ is set to 20 ps, corresponding to a 65 nm process [6].

$$I(t) = Q\frac{2}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(-\frac{t}{T}\right). \quad (1)$$

Table I shows node numbers to evaluate $Q_{\mathrm{crit}}$ in all four (Q, CLK) states. Table II shows $Q_{\mathrm{crit}}$ of NMOS transistors in the standard and proposed FFs. In STDFF, the node 1 and 3 are weaker to soft errors than the other nodes because the output current of tri-state inverter is low. The proposed FFs increase $Q_{\mathrm{crit}}$ at the vulnerable nodes to improve soft-error tolerance.

In PLTGFF, revising the circuit topology increases stray capacitance at the node 3 to increase $Q_{\mathrm{crit}}$. The number of logic gates through which the signal passes from the transmission gate to the output is reduced and then the increment of C-Q delay is suppressed. In the primary latch (PL), the clocked inverter is split into an inverter and a transmission gate and the inverter is moved between the input and output nodes in order to keep the number of transistors in the latch. This change results in the same circuit operation as STDFF without increasing the number of transistors. The gate width of the PMOS transistors that constitute the feedback gate is doubled. The size doubling increases the number of holes that capture the electrons collected in the diffusion region [7].

FBTIFF is implemented to increase $Q_{\mathrm{crit}}$ as in PLTGFF. As shown in Fig. 4, the SET pulse generated at the node 3 can be suppressed by inserting the PMOS pass transistor [8].

TABLE III: Difference in static power with or without NMOS (Normalized to STDFF)

| Circuit structure | Static power |
|---|---|
| STDFF | 1.00 |
| FBTIFF | 1.55 |
| FBTIFF (without N0) | 212 |

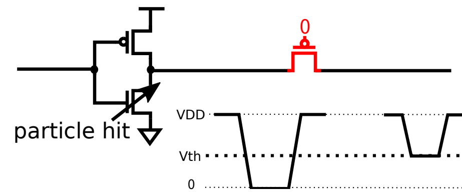
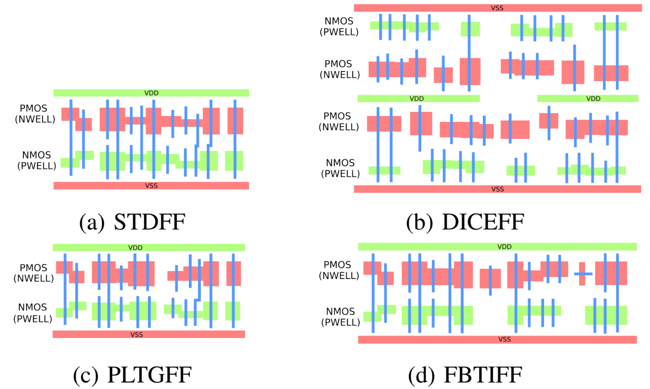



Fig. 4: SET suppression mechanism using PMOS pass transistor



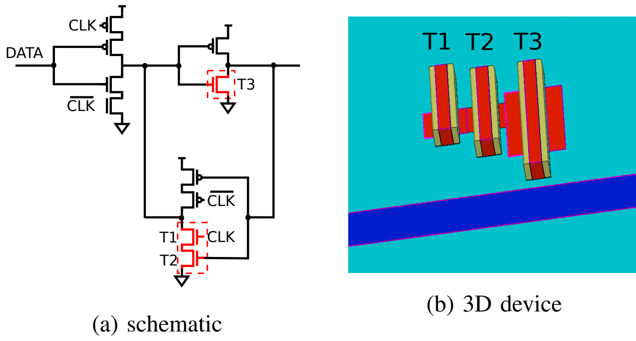

(a) STDFF (b) DICEFF (c) PLTGFF (d) FBTIFF

Fig. 5: Simplified layout patterns of STDFF, DICEFF and the proposed FFs. They are designed in 9 pitches. DICEFF is designed in the double height.

However, it significantly increases static power because of the drain node of the ON-state PMOS pass-transistor. Therefore, the cascaded NMOS (N0) is added to the inverter in the secondary latch (SL) to reduce static power. Table III shows static power with or without the NMOS. These results show that static power can be significantly reduced by the cascaded NMOS. Both of the clocked inverters in PL and between PL and SL are split into the inverter and the transmission gate [7]. The pass transistor (P0) is added between the tristate inverter between PL and SL and the node 1. The gate width of the PMOS is also doubled as PLTGFF. These revisions increase the amount of current flowing into the node 1. Fig. 5 shows layout patterns of the fabricated FFs with 9 pitches.

### *B. TCAD Simulations*

We estimate soft error tolerance by device simulations using Synopsys Sentaurus. NMOS transistors in PL and SL are modeled in the device level, while the other transistors are modeled in the circuit level. An example of the 3D device structures is shown in Fig. 6. We constructed a 3D transistor model to fit static characteristics of a SPICE simulation model distributed from a fabrication company. In this paper, we estimate soft error tolerance by threshold LET (Linear Energy Transfer). LET is the energy given to a material by a charged particle as it passes through a unit length. LET value is proportional to the amount of charge generated when a particle hits the transistor. The threshold LET is the minimum LET value that upsets stored values. Fig. 7 shows threshold LET. In this study, threshold LET values are obtained by irradiating heavy ions vertically at the center of the diffusion region of NMOS in node 1 and 3 of the circuit under evaluation at 0.01 $\mathrm{MeV{\cdot}cm^2/mg}$ resolutions. Table IV shows threshold




(a) schematic

(b) 3D device

Fig. 6: Schematic and 3D device structure on TCAD

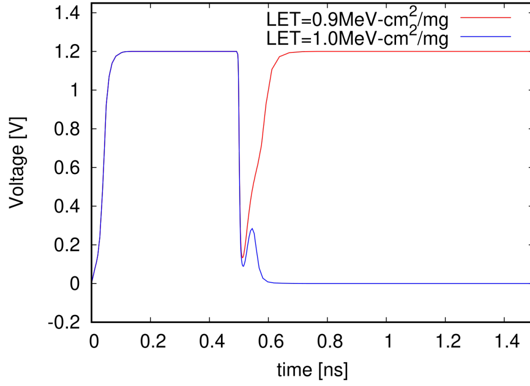



Fig. 7: Threshold LET. No flip occurs when the LET of irradiated heavy ions is $0.9\ \mathrm{MeV{\cdot}cm^2/mg}$, while a flip occurs when the LET becomes $1.0\ \mathrm{MeV{\cdot}cm^2/mg}$.

LET values to cause a soft error at each node calculated by TCAD simulations. The threshold LET values at each node increase as $Q_{\mathrm{crit}}$ increase. Therefore, the proposed FFs are expected to improve soft error tolerance. The threshold LET values of all nodes increase by 30% in PLTGFF compared to STDFF. In FBTIFF, threshold LET values at all nodes are significantly increase than STDFF. In particular, the threshold LET value at the node 3 increases by more than 400% compared to STDFF, indicating high soft-error tolerance.

### C. Circuit Performance

We calculate area, D-Q delay time, power consumption of those FFs using circuit simulations at the standard supply voltage ($V_{\mathrm{dd}}$) of 1.2 V. These performances of STDFF, proposed FFs, and DICEFF are shown in Table V. PLTGFF has the area, delay, and power overheads by 5%, 4%, and 10%, respectively. FBTIFF has the area, delay, and power overheads by 42%, 10%, and 22%, respectively. These FFs are able to suppress D-Q delay by changing the circuit topology of SL. In FBTIFF, the area increase significantly by 42% compared to STDFF due to the pass transistor. The proposed circuits have smaller number of transistors than conventional radiation-hard FFs and much lower performance overheads. Table VI shows C-Q delay, setup and hold time of the conventional and proposed FFs.

TABLE IV: TCAD simulation results of threshold LET at vulnerable nodes.

| Circuit structure | threshold LET [$\mathrm{MeV{\cdot}cm^2/mg}$] | |
|---|---|---|
| | node1 | node3 |
| STDFF | 0.45 | 0.35 |
| PLTGFF | 0.60 (1.33) | 0.46 (1.31) |
| FBTIFF | 1.20 (2.66) | 1.90 (5.43) |

TABLE V: Simulation results of area, D-Q delay, and power of the conventional and proposed FFs at $V_{\mathrm{DD}}$ = 1.2 V. (Normalized to STDFF). The number of transistors includes clock buffersA.

| Circuit structure | Area | Delay | Power | # of Tr. |
|---|---|---|---|---|
| STDFF | 1.00 | 1.00 | 1.00 | 24 |
| PLTGFF | 1.05 | 1.04 | 1.10 | 24 |
| FBTIFF | 1.42 | 1.10 | 1.22 | 29 |
| DICEFF | 2.95 | 3.03 | 2.94 | 50 |

## III. Experimental Results

The test chips were fabricated in a 65 nm bulk process. All FFs were implemented in a shift register. We evaluated soft-error tolerance by $\alpha$ particle and neutron irradiation tests. The irradiation tests were conducted as follows.

1) Initialize serially-connected FFs by all 0 or all 1.
2) Stabilize CLK to 0 or 1.
3) Expose $\alpha$-particles or neutrons to FFs.
4) Read out stored data of FFs.
5) Count the number of upsets.
6) Repeat 1 - 5 for four (Q, CLK) conditions.

### A. $\alpha$ Particle Irradiation

$\alpha$ particle irradiation tests were carried out using a $3\,\mathrm{MBq}$ $^{241}\mathrm{Am}$ source. We exposed $\alpha$-particles to FFs for 30 seconds. Fig. 8 shows $\alpha$-SER of the proposed FFs with error bars of 95% confidence at $V_{\mathrm{dd}}$ = 1.2 V. The $\alpha$-SER of DICEFF is almost zero. The proposed FFs have improved soft error tolerance compared to STDFF. However, PLTGFF was weak at (Q, CLK) = (0, 0). As show in Table I, the node 3 in PLTGFF is weak at (Q, CLK) = (0, 0). However, the $\alpha$-SER of PLTGFF is 40% less than that of STDFF at (Q, CLK) = (1, 0) where the node 3 in STDFF is weak. Compared to the result of STDFF at (Q, CLK) = (1, 0) where the node 3 is also weak, the $\alpha$-SER of PLTGFF is 40% smaller than STDFF. Therefore, the proposed FFs have improved soft-error tolerance at all nodes. The overall error rate is 45% lower for PLTGFF and 90% lower for FBTIFF than STDFF.

### B. Spallation Neutron Irradiation

Spallation neutron tests were conducted at the research center for nuclear physics (RCNP), Osaka University, Japan [9]. Fig. 9 shows the normalized neutron beam spectrum with the terrestrial neutron spectrum defined in JESD 89B

TABLE VI: Simulation results of C-Q delay, setup time and hold time of the conventional and proposed FFs. (Normalized to STDFF)

| Circuit structure | C-Q delay | Setup time | Hold time |
|---|---|---|---|
| STDFF | 1.00 | 1.00 | 1.00 |
| PLTGFF | 0.94 | 3.18 | 0.94 |
| FBTIFF | 0.98 | 3.80 | 0.96 |
| DICEFF | 1.92 | 8.69 | 0.67 |

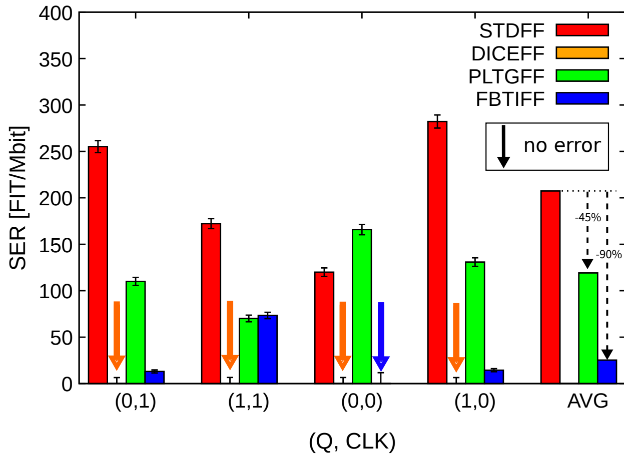



Fig. 8: $\alpha$-SER under four (Q, CLK) states and average $\alpha$-SER. Error bars are within 95% confidence. These results assume the use of the super ultra low alpha (SULA) package ($0.001\ \mathrm{cph/cm^2}$). Note that DICEFF has no error at all conditions.

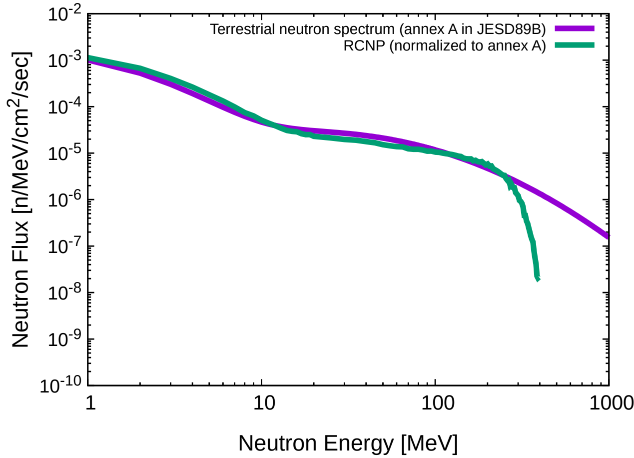



Fig. 9: Terrestrial neutron spectrum and that from spallation neutron source at RCNP.

($12.96\ \mathrm{n/cm^2{\cdot}h}$) [10]. The average acceleration factor (AF) is $1.0 \times 10^8$ in average. We exposed neutrons to FFs for 1800 seconds. In order to increase the number of errors in the limited measurement time, 32 test chips are measured simultaneously as shown in Fig 10. Fig. 11 shows n-SER (neutron-SER) of the proposed FFs with error bars of 95% confidence at $V_{dd}$ = 1.2 V (standard voltage). The n-SER of DICEFF is almost zero, indicating that it is sufficiently resistant to terrestrial neutron strikes. Compared to STDFF, the soft error tolerance of FBTIFF is improved at (Q, CLK) = (0, 1), (0, 0), and (1, 0) while FBTIFF was weak at (Q, CLK) = (1, 1) due to insufficient $Q_{\rm crit}$. The soft error tolerance of PLTGFF is improved at (Q, CLK) = (0, 1) and (1, 0). However, PLTGFF was weak at (Q, CLK) = (0, 0) and (1, 1). The overall error rate is 18% lower for PLTGFF and 35% lower for FBTIFF than STDFF.

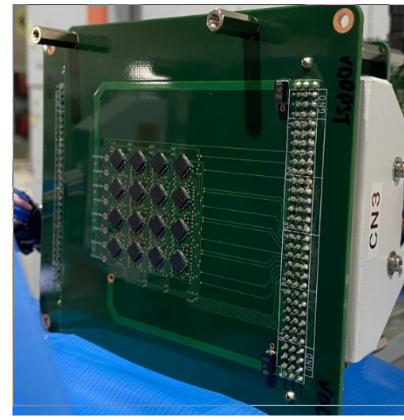


Fig. 10: Simultaneous measurement of 32 test chips at the neutron irradiation test. 16 chips are mounted on the DUT board, and two DUT boards are simultaneously irradiated.

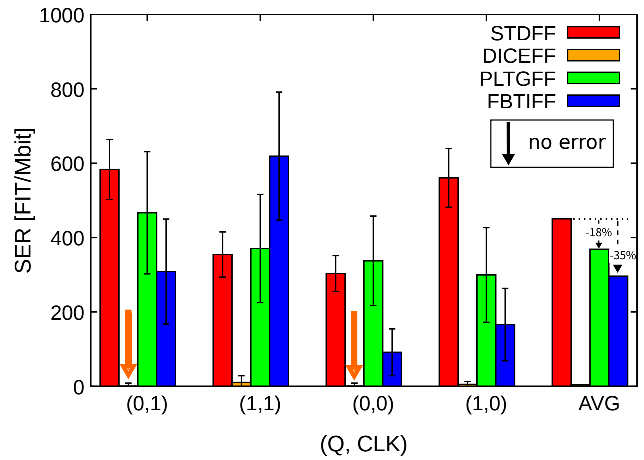



Fig. 11: N-SER under four (Q, CLK) states and average $\alpha$-SER. Error bars are within 95% confidence.

## C. Discussions

Fig. 12 shows sum of $\alpha$- and n- SER of STDFF, DICEFF, and the proposed FFs. Both $\alpha$-SER and n-SER of DICEFF are almost zero, ensuring sufficient soft error tolerance. The proposed FFs are not as soft error tolerant as DICEFF. However, the SER in the terrestrial environment is reduced by 25% for PLTGFF and 50% for FBTIFF compared to STDFF.

Fig. 13 shows the 2-dimensional charts plotting performance overheads and soft error tolerance of those FFs. The value of SER is the sum of $\alpha$-SER and n-SER. The SER and performances are normalized by the STDFF value. The numerical values in the graph indicate the distance from the origin. The smaller this value is, the better tha balance between performances and reliability. The figure shows that DICEFF has highest soft-error tolerance with relatively large performance overhead. Therefore, there seems to be an imbalance between performance and reliability in the terrestrial environment. In the terrestrial environment, the proposed FFs have better trade-offs between reliability and performance compared to DICEFF and STDFF.

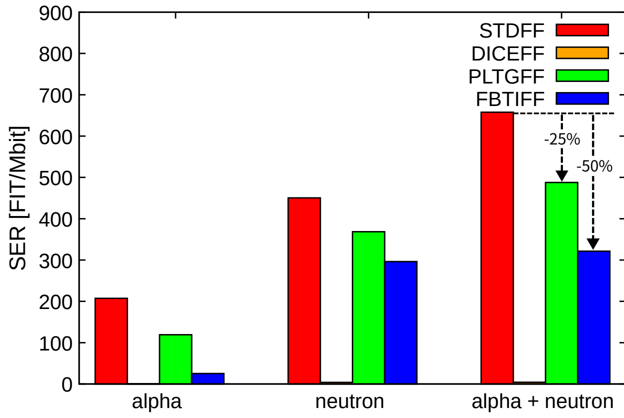
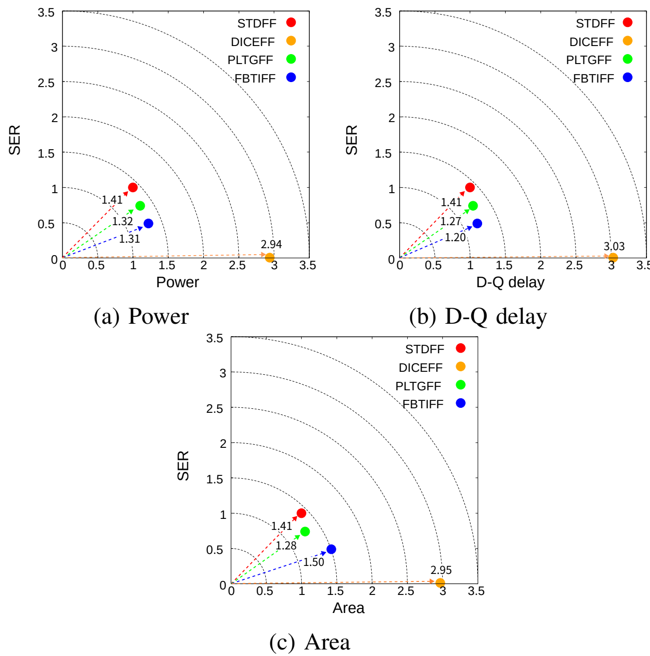



Fig. 12: Sum of $\alpha$- and n- SER. Each SER is the average of all four (Q, CLK) conditions.




(a) Power

(b) D-Q delay

(c) Area

Fig. 13: 2 dimensional charts of soft error tolerance and each performance (Area, DQ-delay, Power). SER is the sum of $\alpha$-SER and n-SER. SER and each performance are normalized by th STDFF value.

## IV. Conclusion

We proposed two types of FFs to improve soft error tolerance. $Q_{\mathrm{crit}}$ at the vulnerable nodes are increased by changing circuit topologies with additional transistors and wires. These proposed circuit structures without any multiplication of storage elements suppress the circuit performance overheads, especially D-Q delay. Compared to DICEFF, the performance overheads of the proposed FFs are very small. We fabricated proposed FFs in a 65 nm bulk process and evaluated soft error tolerance by $\alpha$ and neutron irradiation tests. $\alpha$ irradiation reveals that the $\alpha$-SERs of PLTGFF and FBTIFF are 45% and 90% lower than STDFF. By neutron irradiation, the n-SERs of PLTGFF and FBTIFF are 18% and 35% lower than STDFF. Although the proposed FFs are weaker to soft errors than multiplexed FFs, they still have higher soft error tolerance than the standard FF to $\alpha$-particles and neutrons with small performance overheads. These countermeasures are expected to be applicable to advanced process nodes below 65 nm. These are also effective in the FDSOI process because carrier collection efficiency is less than bulk.

## Acknowledgment

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