A 13-bit Radiation-Hardened SAR-ADC with Error Correction by Adaptive Topology Transformation

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***Abstract*— A 13-bit radiation-hardened-by-design (RHBD) successive approximation register ADC (SAR-ADC) has been proposed with almost no area overhead. The RHBD SAR-ADC has a differential topology with a couple of radiation detectors, and these radiation detectors are assigned, one for each of the differential data paths. The ADC transforms the topology adaptively from differential to single based on the result of radiation detection for error correction or reduction. Thanks to the error correction or reduction by the Adaptive Topology Transformation (ATT), measurement results show an order of magnitude improvement in cross-section and more than 10 dB SNDR enhancement under over 10^6 count/cm^2 irradiation condition.**

Keywords- SAR-ADC, Radiation-Hard, Radiation Detector, Single and Differential Topologies, Topology Transformation

I. INTRODUCTION

For the last decade, resilience enhancement to radiation effects has been required for Integrated Circuits (ICs) in various applications, e.g. space, nuclear and medical industries. In these applications, ICs have to work properly under an environment of high dose rate radiation. In such environment, a high-energy particle hits a node in ICs and the circuit's node voltages get affected to provoke the non-destructive single-event effect (SEE). It causes a flipping of data state in digital circuits, which is known as a single-event upset (SEU) [1-3]. As for analog circuits, a single-event transient (SET) fluctuates the amplitude and degrades the linearity of an analog signal [4-5].

To enhance the resilience for radiation effects, the most direct way is to use specific fabrication process which is particularly designed to achieve radiation-hardness (Radiation Hardening-By-Process, RHBP). However, the rad-hard process has fewer variations and higher costs than the standard process. Recently, new space companies of private capital have entered the space industry, and cost-consciousness of space products including ICs has been required. Under these circumstances, Radiation-Hardness-By-Design (RHBD) techniques have been reported to improve radiation resilience through design using standard commercial processes [6-7].

An Analog-to-digital converter (ADC) is essential component of Integrated Circuits (ICs), and successive approximation register ADC (SAR-ADC) is very suitable for cost-conscious products, thanks to its small area and low power consumption. Therefore, RHBD SAR-ADCs have been reported [8-10] to enhance resilience for SET, which generates carriers (electron and hole) in a substrate to potentially change the amount of electric charges stored in capacitors of Capacitive D/A Converter (C-DAC) in SAR-ADCs. To avoid wrong code generation by SET, guard rings [8], extra ADCs & operation cycles [9] and redundant C-DAC [10] were adopted. However [8] could not correct error of wrong codes and [9,10] required overheads of area and conversion-time due to the redundant components.

This paper proposes simple error collection or reduction scheme for differential SAR-ADC using the radiation detector without any additional ADC/C-DAC nor operation cycle.

II. CIRCUIT CONCEPT OF RADIATION HARDNESS

Fig. 1 shows block diagram of the proposed SAR-ADC. The SAR-ADC has 13-bit resolution and complementary input signals (V_{INP}, V_{INN}) for differential topology. The differential signals (V_{INP}, V_{INN}) are fed to a couple of capacitive D/A converters (C-DACs). Each C-DAC possess binary-waited capacitors to support the 13-bit resolution, and the capacitors have common nodes (V_{DACP}, V_{DACN}) for sequential comparison by a comparator. The differential input signals (V_{INP}, V_{INN}) are sampled onto the comparison nodes (V_{DACP}, V_{DACN}) by sampling switches and the sampled voltages are continuously compared 13 times by the comparator to generate A/D conversion codes.

The SAR-ADC features a comparator with a multiplexer. The multiplexer changes comparison nodes from C-DAC node (V_{DACP}, V_{DACN}) to external common-mode voltage (V_{CM}) of the differential input signals (V_{INP}, V_{INN}). If either V_{DACP} or V_{DACN} switches to V_{CM} in the multiplexer, the switched side C-DAC is excluded from the comparison in the comparator and a sequential comparison is executed between the non-switched side C-DAC and V_{CM}. Namely, the SAR-ADC changes conversion topology from differential to single when the multiplexer switches the input of the comparator from C-DAC node (V_{DACP}, V_{DACN}) to the common-mode voltage (V_{CM}). The decision for switching between the C-DAC node (V_{DACP}, V_{DACN}) and the common-mode voltage (V_{CM}) at the multiplexer is made by a couple of radiation detectors.

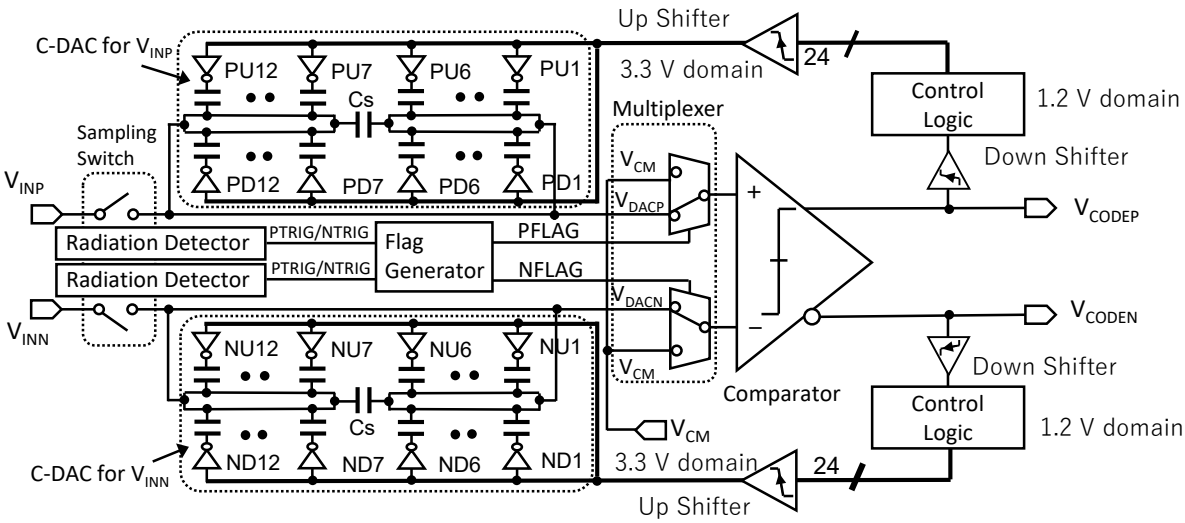


Figure 1. *Circuit Diagram of the proposed SAR-ADC*

The radiation detectors are placed near the sampling switches of differential signal inputs (V_{INP}, V_{INN}) respectively. The radiation detector launches flag signals (PFLAG, NFLAG) when detects carrier generation of hole and electron by SET. The carrier generation may cause wrong digital code of A/D conversion in normal SAR-ADCs. Because the A/D conversion of SAR-ADCs assumes that the total amount of charge in the capacitors of the C-DAC is conserved during whole time of a conversion period. Therefore, if extra charge is injected into the capacitors, SAR-ADCs will produce the wrong digital codes.

A basic idea to suppress wrong code generation of the SAR-ADC is as follows. The charge injection is occurred through the sampling switches, because the capacitors in C-DAC have MIM (Metal-Insulator-Metal) structure and the comparison nodes (V_{DACP}, V_{DACN}) of C-DAC have diffusion areas **only** at the sampling switches. Therefore, a couple of radiation detectors are allocated very close to the sampling switches to correct the carriers generated by SEE. When charged particles hit to one of the sampling switches of the differential inputs (V_{INP}, V_{INN}) and generate extra carriers (hole and electron) at the sampling switch, surplus electric charge may enter capacitors of the C-DAC corresponding to the sampling switch. In this situation, the radiation detector which is placed near the irradiated sampling switch asserts the flag signal (PFLAG or NFLAG) to disconnect the charge-injected C-DAC from the comparison of the comparator. The comparator compares the comparison node (V_{DACP}, V_{DACN}) of another C-DAC with the common-mode voltage (V_{CM}). Since the SAR-ADC disconnects the C-DAC with the possible surplus charge from the successive approximation, the generation of the wrong digital code will be suppressed.

It means that the differential type SAR-ADC transforms into a single type for the error correction or reduction of wrong code adaptively according to the result of radiation detection. The essence of this Adaptive Topology Transformation (ATT) is to correct or reduce the error of wrong codes by disconnecting the comparison voltage (V_{DACP} or V_{DACN}) from the C-DAC of the irradiated side and switching to the common-mode voltage (V_{CM}) prior to the comparison at the comparator.

More specifically, in the SAR-ADC, successive approximation is sequentially performed by the comparator, then the comparison voltages (V_{DACP}, V_{DACN}) of the C-DACs change according to the comparison result for the next comparison. Namely, each successive approximation is usually a comparison of the complementary signals (V_{DACP}, V_{DACN}) of the C-DACs. However, when irradiated, the C-DAC on the irradiated side is disconnected and the comparison node (V_{DACP} or V_{DACN}) is switched to the common-mode voltage (V_{CM}) prior to the comparison by the comparator. Hence the comparison result of the comparator does not refer to the comparison voltage (V_{DACP} or V_{DACN}) of the C-DAC on the irradiated side. In other words, the proposed SAR-ADC basically outputs the same digital code as a single SAR-ADC without irradiation.

III. CIRCUIT DETAILS

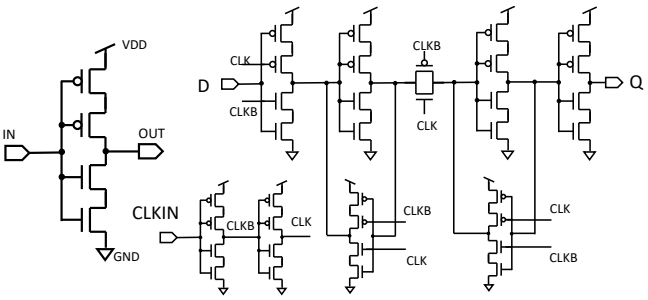
This chapter describes characteristic circuits in the proposed SAR-ADC. All analog circuits described below were designed with bulk CMOS transistors for 3.3V operation. Therefore, the analog circuits may malfunction by SET under irradiation condition. As for digital circuit, SOI transistors were used to avoid malfunction due to radiation emission. The SOI structure inherently resistant to SEU and SET because of bulk substrate isolation from source and drain nodes by an insulator of SiO2. This research focuses on the RHBD implementation of analog circuits, and utilizes the RHBP approach for digital circuits.

A. Capacitive D/A Converter (C-DAC)

As shown in Fig.1, C-DAC has binary-waited MIM capacitors, and the capacitance of minimum capacitor is about 40 fF. In the C-DAC, the lower bit capacitor group (1~6) and the upper bit capacitor group (7~12) are identical, and these groups are connected by a coupling capacitor (Cs) at a common terminal (V_{DACP}, V_{DACN}) of the capacitors. This configuration dedicates an area reduction of C-DAC layout. The other terminals of these capacitors are connected to VDD33 (3.3 V) or GND by control signals from the control logic in Fig.1.

B. Digital Circuits

The control logic is pure digital circuit, and the digital circuit is designed using CMOS transistors of the SOI structure as stated above. The SOI transistors are operable at 1.2 V. Furthermore, as shown in Fig.2, the digital circuits adopt stacked structure of PMOS and NMOS transistors to enhance a tolerance to radiation emission by a dispersion of the generated carriers [12, 13]. This hybrid approach of RHBP and RHBD in the digital circuits helps focus research activity on analog circuits using bulk CMOS transistors.



(a) *Inverter* **(b)** *Flip-Flop*

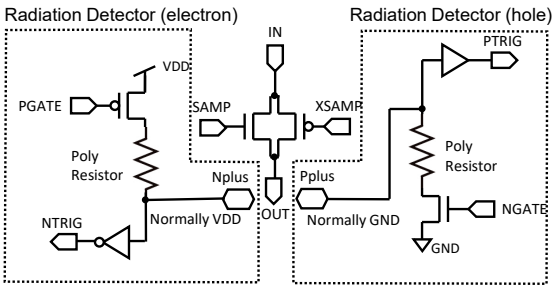
Figure 2. *Examples of Circuit Schematics for the Digital Circuit*

C. Samling Switch and Radiation Detector

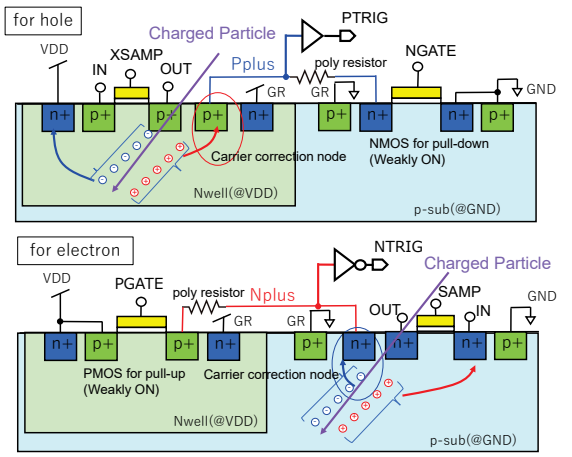
Fig. 3 (a) shows circuit schematics of the sampling switch and the radiation detector. The sampling switch consists of PMOS and NMOS transistors. The radiation detector has pull-up resister with PMOS and pull-down resistor with NMOS for electron and hole collection at diffusion nodes of Nplus and Pplus respectively. The resistances of the pull-up and pull-down can be controlled by gate voltages of PGATE and NGATE. To produce proper voltage pulse for PTRIG and NTRIG generation, the resistances of the PMOS and NMOS are very important. The resistance adjustment should be done at an actual experiment with an irradiation condition.

Fig. 3 (b) illustrates physical cross section of the sampling switch and the radiation detector. When charged particle strikes the vicinity of the sampling switch and generates electron-hole pairs in the p-type substrate or Nwell, the hole and electron are collected at Pplus and Nplus nodes respectively, because Pplus and Nplus nodes are set to lower and higher voltages respectively through the pull-down and pull-up structures. At the same time, the generated electron in Nwell and hole in p-substrate are similarly corrected to VDD and GND through n+ and p+ diffusion. These carrier corrections cause a momentary current flow from VDD to GND through poly-resistor, then the resistor produces a voltage pulse and launches a pulse signal of PTRIG or NTRIG. The radiation detector asserts detection of radiation exposure at the sampling switch by low to high voltage transition of PTRIG or NTRIG signal.

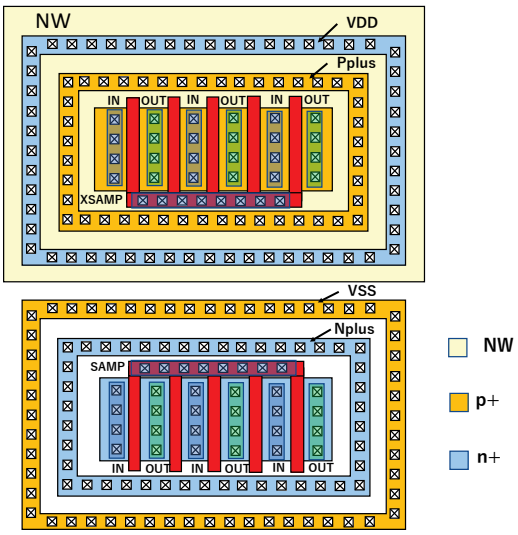
Fig. 3 (c) depicts a concept of frontend layout for the sampling switch and the radiation detector. As shown in the figure, p+ (Pplus) node is surround PMOS of the sampling switch and connected to GND through poly resistor and NMOS (not shown) of Fig.3(a) and (b). In same manner, n+ (Nplus) encircles NMOS of the sampling switch and tied to VDD through poly resistor and PMOS (not shown).



(a) *Circuit Schematics*



(b) *Physical Cross Section*



(c) *Layout Concept*

Figure 3. *Sampling Switch and Radiation Detector*

Fig.4 illustrates circuit schematic of Flag Generator for the post-processing of the output signal from the radiation detector. The output signals (PTRIG, NTRIG) from Radiation Detectors for differential inputs (V_{INP}, V_{INN}) are ORed to tell hole or electron generation at the sampling switches of V_{INP} or V_{INN}. The ORed signals are fed to Set inputs of a couple of SR latches. Both SR latches accept SCLK at their Reset inputs and output flag signals of PFLAG and NFLAG. The SCLK is system clock that represents one cycle of A/D conversion. Therefore, once the flag signal of PFLAG or NFLAG is asserted, the assertion is held until the A/D conversion is finished. In other words, once carrier generation by radiation emission is detected, the SAR-ADC operates in single mode topology during the conversion cycle.

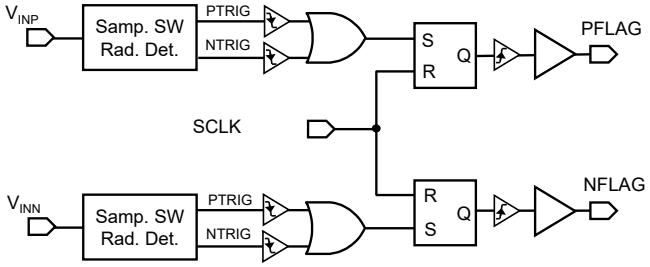


Figure 4. *Circuit Schematic of Flag Generator*

D. Comparator with Multiplexer Capability

Fig.5 depicts circuit schematic of the comparator. As shown in the figure, the comparator is double-tail dynamic latch type. The comparator compares output voltages (V_{DACP}, V_{DACN}) of C-DACs for V_{INP} and V_{INN} at rising edge of operation clock (CLK), and feed the comparison result (V_{CODEP}, V_{CODEN}) to the control logic for successive approximation.

The comparator has a capability of the multiplexer by gating the CLK (CK_P, CK_N) using the flag signals (PFLAG, NFLAG). The comparator changes comparison signal by PFLAG or NFLAG assertion from the comparison node (V_{DACP} or V_{DACN}) to the common-mode voltage (V_{CM}) which is intermediate voltage of differential input signals (V_{INP}, V_{INN}). A cascode connection of NMOS of CK_P and CK_N contribute to reduce kickback noise of the operating clock (CLK).

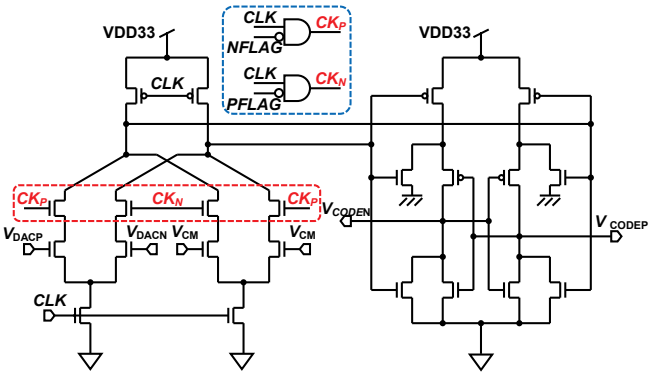
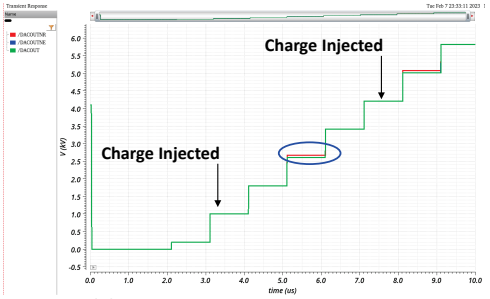


Figure 5. *Double-tail comparator with input multiplexing capability*

IV. Simulations

This chapter shows simulation results of the proposed SAR-ADC. A differential ramp signal from -3.3 V to 3.3 V was applied onto V_{INP} and V_{INN}, then A/D conversion results, i.e. digitized 13-bit codes were observed via converting to a decimal voltage value. Fig.6 shows the decimal value in voltage on time-domain.



(a) *Digital Codes of Ramp signal Input*

(b) *Digital Codes with and w/o Error Correction*

Figure 6. *Simulation Waveforms of the SAR-ADC*

The ramp signal is properly converted to a stepped decimal digital code as shown in Fig.6(a). In this simulation, three conditions were set in the matrix of charge injection and error code collection. As for the charge injection, current model for heavy ion strike of Kr was used [14], and the charge was injected into p+ diffusion of sampling switch of V_{INN}. Due to the charge injection, three different codes were generated. The different codes (blue circle) are shown enlarged in Fig.6(b).

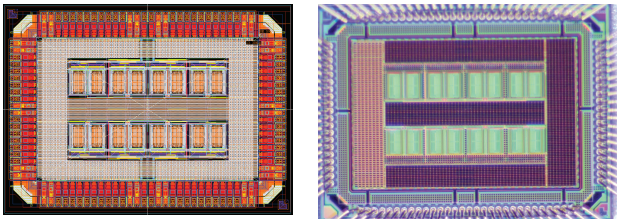
As shown in Fig. 6(b), the correct digital code is 2604 (blue) without charge injection. When charge injection occurs, the digital code becomes 2667 (red), which significantly deviates from the correct code. However, when the proposed RAD-hardened design is enabled, the digital code becomes 2604 (green), which exactly same as the correct value of 2604. The simulation results prove that the proposed error correction can effectively correct the error caused by SET occurring at the sensitive V_{INN} node.

V. Test-Chip Measurement

A test-chip of the SAR-ADC was fabricated by Renesas 65 nm thin-BOX FDSOI process. As stated above, analog blocks including C-DAC were designed by bulk CMOS 3.3 V I/O transistors. SOI transistors were used only in digital blocks. This is to remove the stability concern in SAR logic circuits under irradiation condition. Measurements with heavy ion irradiation were carried out at CYRIC, Tohoku University, Japan.

A. Testchip Configuration

Fig.7 shows layout and micrograph of the test-chip. The test-chip has 8 types of SAR-ADCs, which have variations in the control logic, radiation detector and comparator.



(a) *Chip Layout* **(b)** *Chip Micrograph*

Figure 7. *Test-chip Layout and Micrograph*

The control logic was designed by the 1.2 V SOI or 3.3 V I/O Bulk transistors. The design by Bulk transistors is for comparison with SOI design. As for the radiation detector, we have prepared two types of transistor sizes for inputting PGATE and NGATE signals in Fig.3(a): a predetermined size and twice that size. Regarding the comparator, there is a variation that allow external control of whether the input signal is the comparison voltage (V_{DACP}, V_{DACN}) from the C-DAC or the common-mode voltage (V_{CM}).

These variations are summarized in Table 1.

Table 1. *SAR-ADC Variations*

ADC#	#1	#2	#3	#4	#5-8
Transistor of Ctrl Logic	1.2 V SOI				3.3 V Bulk
Tr. size of P/NGATE	N.A	×1	×2	×1	Same Comb. as #1~4
Function of Comparator	Normal (no VCM)	Same as Fig.5	→	Ext. Controll able	↓
Description	Non RH	RHBD	→	Test Purpose	↓

The ADC#5~8 are same combinations as ADC#1~4 except for the control logic configuration.

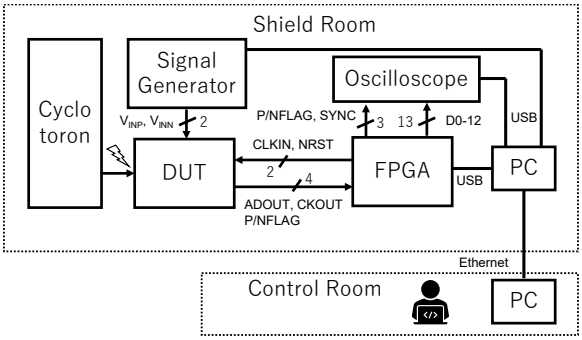
Regarding to ADC#5~8 in Table 1, the control logic of 3.3 V bulk transistors did not work properly by SET in the actual measurement at irradiation condition. Therefore, we excluded ADC#5~8 from the measurements, and block diagrams of ADC#5~8 are not illustrated in this paper.

As shown in the Table 1, one of the eight types of SAR-ADCs (ADC#1) is a conventional SAR-ADC (non-RHBD SAR-ADC) with a normal comparator and no radiation detector.

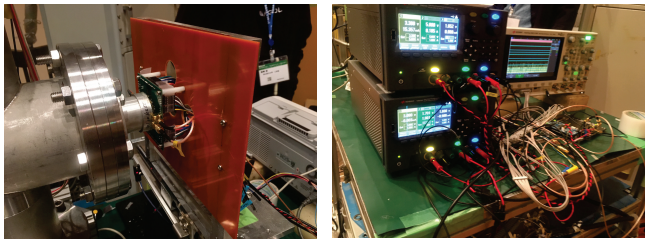
Differential inputs (V_{INP}, V_{INN}) and sampling clock are common for 8 SAR-ADCs. The 13-bit digital code, i.e. the result of A/D conversion is sequentially output as a 1-bit digital signal of ADOUT. To specify a boundary for the sequential output of ADOUT, a boundary clock is output as CKOUT. The ADOUT and CKOUT are also common for 8 SAR-ADCs and these outputs are multiplexed by a combination of external digital input signals.

B. Measurement System and Conditions

Fig.8 shows measurement system in CYRIC. Device Under Test (DUT) is irradiated by Cyclotron, and handled by FPGA board. The FPGA supplies sampling clock (CLKIN) to DUT, and performs a serial-to-parallel conversion of ADOUT in order to feed 13-bit digital code to an oscilloscope. The FPGA also pass-throughs flag signals (PFLAG, NFLAG) and the boundary clock (CKOUT) to the oscilloscope. The differential input of V_{INP} and V_{INN} is fed by a signal generator. The FPGA board, the oscilloscope and the signal generator are controlled by PC via USB in the shield room.



(a) *Block Diagram*



***(b)** Irradiation Port and DUT* ***(c)** Measuring Instruments*

Figure 8. *Measurement System in CYRIC*

The PC in the shield room is controlled by another PC in the control room through an internal network of CYRIC. As shown in Fig.8(b) and (c), the experiments are carried out in atmospheric radiation emission, and supply voltages to DUT are set by DC power supply.

C. Measurement Results

The proposed and conventional type SAR-ADCs were measured using above mentioned conditions. The irradiation condition is listed in Table 2.

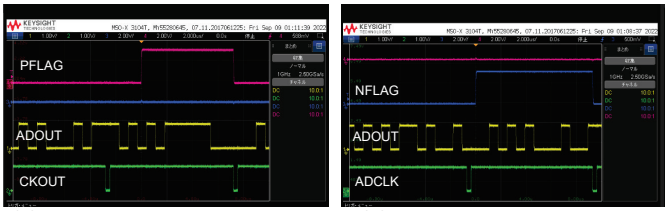
Table 2. *Characteristics of Heavy Ion in the measurement*

Ion Spacies	Energy (MeV)	LET (MeV·cm^2/mg)	Range in Si (μm)	Flux (N_{flux}) (#/cm^2/sec)
$^{84}Kr^{17+}$	180	41	25.8	8.5×10^4

To adjust the resistance of PMOS and NMOS in Fig.3(a), PGATE and NGATE voltage have been changed gradually with observing PFLAG and NFLAG assertion in actual measurement under the irradiation condition using ADC#2 in Table 1.

Fig. 9 shows analog output signals from the proposed ADC#2 under Kr irradiated condition. The signals are the sequential output of digital code (ADOUT), the boundary clock (CKOUT) and the flag signals (PFLAG, NFLAG). As shown in the figure, both flag signals (PFLAG, NFLAG) remains asserted until the end of the A/D conversion cycle as depicted in Fig.4. At this situation, PGATE and NGATE were set to 1.3 V and 0.5 V respectively, therefore we adopted these voltage conditions of PGATE and NGATE in the actual measurement. As for ADC#3, due to time constraints, we have not yet found the optimal voltages for PGATE and NGATE.

Hence, we focused to ADC#1 and 2 in the actual measurement.

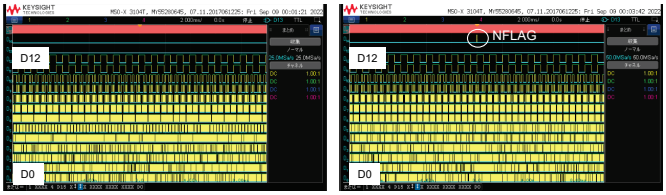


(a) *PFLAG assertion at Kr irradiation* **(b)** *NFLAG assertion at Kr irradiation*

Figure 9. *Measured Digital Code (D0-12) at DC input and Analog Output*

(1) AC input under irradiated condition

A sinusoidal signal of 1 kHz with 1 V amplitude was fed to the differential input (V_{INP}, V_{INN}) of the proposed SAR-ADC, and the SAR-ADC operated in 100 kHz sampling frequency. The 13-bit digital code (D0~D12) and the flag signals are shown in Fig.10(a) and (b). As shown in these figures, any flag signal is not asserted without irradiation and the flag signal of NFLAG has been asserted under Kr irradiated condition. Similarly, PFLAG was also asserted (not shown).



(a) *Before Irradiation* **(b)** *Kr Irradiated*

Figure 10. *Measured Digital Code (D0-12) at DC input and Analog Output*

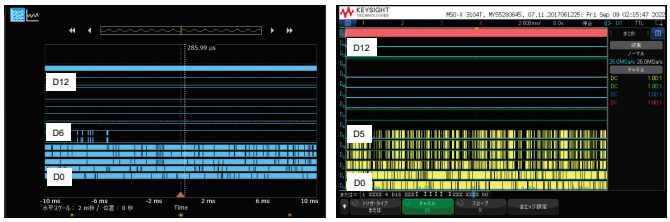
(2) DC input under irradiated condition

In this measurement, input signals were DC voltages with differential amplitude of 100 mV and specified V_{CM} voltages (1.25V, 1.45V and 1.65V). The reason for measuring with the DC input is that it is not possible to identify the error trigger with an AC input. If the expected values of all output codes could be stored in memory and compared sequentially, it would be possible to measure with the AC inputs, but it is very difficult to achieve. In the measurements, triggers of the oscilloscope were set according to DC noise situation before irradiation as stated later.

i) Case of V_{CM}=1.25 V

The irradiation condition was basically the same as in Table 2, but flux was 1.2×10^4 count/cm2/sec for the conventional SAR-ADC (ADC#1). The sampling frequency was 100 kHz.

Fig.11 shows the 13-bit digital code (D0~D12) of the proposed SAR-ADC (ADC#2) and conventional SAR-ADC (ADC#1) before irradiation at V_{CM}=1.25 V. Fig.11(a) has a different appearance from others because of miss-operation at screen saving in the oscilloscope. As shown in the figure, DC noise covers D0 to D6 in the proposed SAR-ADC (ADC#2), therefore triggers of the oscilloscope were set to D7~D12 in actual measurement at V_{CM}=1.25 V.



***(a)** Proposed SAR-ADC (ADC#2)* ***(b)** Conventional SAR-ADC (ADC#1)*

Figure 11. *Measurement on DC input at V_{CM}=1.25 V before Irradiation*

A summary of the measurement results in the condition of V_{CM}=1.25 V is listed in Table 3. As a supplement, the measurement result for the flux of 1.2×10^4 count/cm2/sec in the proposed SAR-ADC (ADC#2) is added.

As described in the Table 3, no error has been detected for 10 minutes under low flux condition of 1.2×10^4 count/cm2/sec in the proposed SAR-ADC.

The SNDR (Signal-to-Noise and Distortion Ratio) is the ratio of the very low-frequency signal power to the total signal power up to the Nyquist frequency.

Table 3. *Summary of Measurement for DC input at V_{CM}=1.25 V*

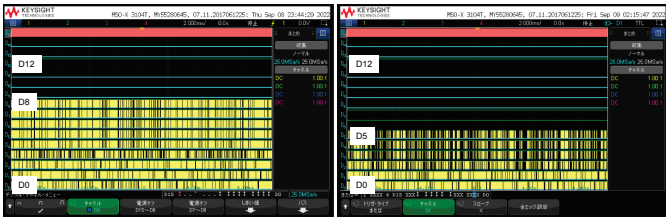
V_{CM}	1.25 V		
ADC Type	Conventional (ADC#1)	Proposed (ADC#2)	
Trigger	D7 ~ D12		
Flux (#/cm2/sec)	1.2×10^4	1.2×10^4	8.5×10^4
Time until 1st Error	39 sec	> 10 min	77 sec
Total Flux (#/cm2)	4.7×10^5	$>7.2\times10^6$	6.5×10^6
SNDR @Error	-57.8 dB	No Error	-58.8dB

ii) Case of V_{CM}=1.45 V and 1.65 V

Fig.12 and 13 show the 13-bit digital code (D0~D12) of proposed SAR-ADC (ADC#2) and conventional SAR-ADC (ADC#1) before irradiation at V_{CM}=1.45 V and 1.65 V respectively.

***(a)** Proposed SAR-ADC (ADC#2)* ***(b)** Conventional SAR-ADC (ADC#1)*

Figure 12. *Measurement on DC input at V_{CM}=1.45 V before Irradiation*



***(a)** Proposed SAR-ADC (ADC#2)* ***(b)** Conventional SAR-ADC (ADC#1)*

Figure 13. *Measurement on DC input at V_{CM}=1.65 V before Irradiation*

As shown in the figures, DC noise covers D0 to D8 in the proposed SAR-ADC(ADC#2), therefore triggers of the oscilloscope were set to D9~D12 in actual measurement at both of V_{CM}=1.45 V and 1.65 V.

The measurement results of V_{CM}=1.45 V and 1.65 V are summarized in Table 4.

Table 4. *Summary of Measurement for DC input at V_{CM}=1.45 V and 1.65 V*

V_{CM}	1.45 V		1.65 V	
ADC Type	Conv. (ADC#1)	Proposed (ADC#2)	Conv. (ADC#1)	Proposed (ADC#2)
Trigger	D9 ~D12			
Flux (#/cm2/sec)	8.5×10^4			
Time until 1st Error	35 sec	527 sec	35 sec	45 sec
Total Flux (#/cm2)	3.0×10^6	4.5×10^7	3.0×10^6	3.8×10^6
SNDR @Error	-34.4 dB	-38.8 dB	-38.8 dB	-38.3 dB

Moreover, there is a difference in noise floor between the proposed and the conventional SAR-ADC. The proposed ADC has a higher noise floor as shown in Fig.10 to Fig.12. This is common to all V_{CM} conditions. This comes from the configuration of the comparator. The conventional SAR-ADC has normal double-tail latch type comparator without V_{CM} input. This is discussed later in discussion session.

iii) Cross Section and SNDR

Fig.13 depicts measured cross-section of the conventional and proposed SAR-ADC at irradiation condition of Table 2. Referring to [15], a cross-section (CS) is expressed as the reciprocal of the time-integrated value of the flux (N_{flux}) until any error detected at the given trigger settings (T_{err}). The CS can be calculated by equation (1).

$$CS^{-1} = \int_0^{T_{err}} N_{flux} dt \qquad (1)$$

Comparing the CS of conventional and proposed SAR-ADC, Fig. 14 shows almost an order of magnitude improvement at V_{CM} of 1.25 V and 1.45 V conditions.

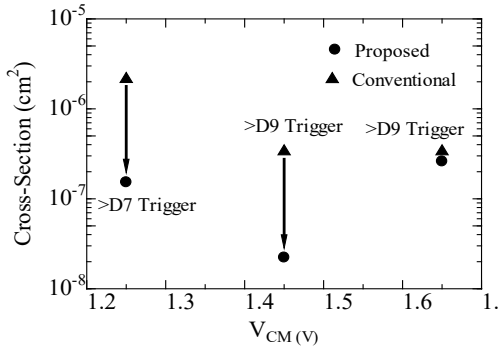


Figure 14. *Measured Cross-Section (DC input)*

Fig. 15 illustrates the SNDR of various fluxes for specified V_{CM} voltages with 100 mV DC differential input. Under the condition of flux above 10^6 count/cm^2, the proposed SAR-ADC shows an improvement of more than 10dB compared to the conventional one.

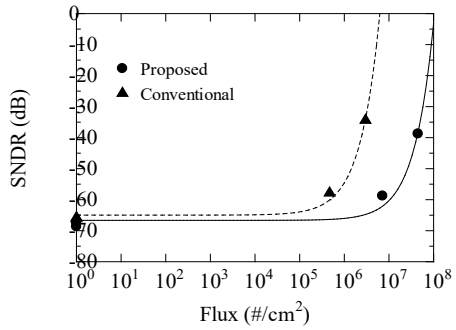


Figure 15. *Measured SNDR v.s Flux (DC input)*

Table 5 summarizes the comparison between the proposed and other RHBD SAR-ADCs. As shown in the Table, the proposed SAR-ADC has significant advantages for overheads of area and conversion time. As stated in the measurement section, the proposed ADC certainly promises improved performance under irradiation conditions compared to the conventional one (non-RHBD). However, others RHBD SAR-ADCs may have higher error correction capabilities than the proposed SAR-ADC because of their very large overhead. This trade-off should be discussed in system design and cost estimation.

Table 5. *Summary of Comparisons in RHBD SAR-ADCs*

		Proposed	[9]	[10]
RHBD Architecture		ATT	TMR	Red. C-DAC*1
Process Technology		0.35 µm/65 nm	65 nm	0.18 µm
Resolution		13 bits	14 bits	12 bits
Meas. w/ Radiation		Yes	Yes	No
Exposure		$^{84}Kr^{17+}$	proton beam	None
Area		0.068 mm^2	0.342 mm^2	N.A.
Overhead	Area	< +2 % by Detector	> +100 % by TMR	+70 %*2 by C-DAC
	Conv. Time*3	0 %	> +20 %	None

*1 Redundant C-DAC , *2 Estimation, *3 Conversion-Time

VI. Discussion

In the measurements, the input signals were set to DC to catch the moment by a trigger of the oscilloscope when an error occurs. As shown in Fig.11 to 13, the trigger criteria have to be changed according to the V_{CM} voltage because the amount of comparator noise varies depending on the V_{CM}, i.e. the higher the V_{CM}, the more amount of noise. Therefore, cross-section improvement was very small in case of V_{CM} = 1.65 V. This symptom comes from cascode design of the comparator. As shown in Fig.5, three NMOS are connected vertically to configure cascode topology. This configuration enhances the comparator's gain, and the gain will be boosted by bias current increase according to higher V_{CM} condition. Furthermore, V_{CM} is fed from an external pin and has a certain amount of noise. The V_{CM} noise reduction and the improvement of the comparator topology are subject to engineering change in next design.

Furthermore, the proposed SAR-ADC has a theoretical disadvantage. Due to Adaptive Topology Transformation, the Signal-to-Noise Ratio (SNR) will degrade by 6 dB. Because a differential amplitude of the input signals from V_{INP} and V_{INN} becomes half after topology transformation from the differential to the single type. This is very important for system design and signal level diagram determination.

VII. Conclusion

The proposed SAR-ADC presented a simple error correction or reduction scheme of ATT, and it does not require any additional ADC or C-DAC. Furthermore, any extra operation cycle is not needed for the error correction. This area-efficient RHBD SAR-ADC showed significant improvement over non-RHBD SAR-ADC in the CS and SNDR by the error correction of ATT under heavy ion ($^{84}Kr^{17+}$) exposure conditions in actual measurements.

The proposed SAR-ADC cannot always correct the error induced by SET perfectly, but can reduce the error, i.e. generate the code more 'close' to the correct data. It means the code is still erroneous, but better than without the ATT mechanism (SET detection circuit and switching from differential to single mode).

The proposed SAR-ADC can generate less-erroneous digital code but cannot fully correct errors completely, and degrades the SNR by transformation to single mode. Although the proposed SAR-ADC has these drawbacks, it can provide an option for system designs of future space electronics thanks to the almost no overhead. Therefore, the proposed SAR-ADC is expected to offer some sort of solutions in the recent space industry, which is becoming more cost-conscious.

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