

An Aging Degradation Suppression Scheme at Constant Performance by Controlling Supply Voltage and Body Bias in a 65 nm Fully-Depleted Silicon-On-Insulator Process

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Abstract—We propose an aging degradation suppression scheme at constant performance by controlling supply voltage and body bias for an FDSOI device. Reducing supply voltage while increasing body bias can maintain performance and suppress dynamic power and aging degradation caused by BTI. From measurement results of ring oscillators in a 65 nm FDSOI, NBTI- and PBTI-induced degradations can be reduced by 29% and 10% at 1.5 V supply voltage and 0.15 V forward body bias paying the penalty of 2x leak power increase.

Index Terms—bias temperature instability (BTI), forward body bias (FBB), ring oscillator (RO)

I. INTRODUCTION

Shrinking device sizes of semiconductor chips has brought a lot of advantages. However, reliability problems such as bias temperature instability (BTI) has become a significant concern with the miniaturization of the device size [1]. BTI-induced degradation occurs when defects trap carriers. However there is no established theory to explain the origin of BTI. Thus it is important to measure and analyze BTI-induced degradation to clarify the origin of BTI.

BTI-induced degradation is accelerated by increasing supply voltage and ambient temperature. Lowering supply voltage greatly suppresses the degradation but circuit performance is degraded. It is possible to keep circuit performance by controlling body bias.

In this paper, we propose an aging degradation suppression scheme by controlling supply voltage and body bias while keeping circuit performance.

II. RING OSCILLATORS SENSITIVE TO NBTI OR PBTI

Fig. 1 depicts NAND-PBTI and NOR-NBTI ROs which suffer from only PBTI or NBTI stress when they stop oscillation. Fig. 2 shows transistor-level schematics of NAND and NOR gates in those ROs [2]. When EN is low or ENB is high, all outputs are fixed to 0 or 1 and the ROs suffer from BTI. PBTI becomes dominant in the NAND-PBTI RO and NBTI becomes dominant in the NOR-NBTI RO. When the ROs stop oscillation, V_{GS} of the colored MOSFETs are in the stress condition. Thus only PBTI or NBTI-induced degradation occurs in the NAND-PBTI and NOR-NBTI ROs respectively. The back gate terminals of PMOSFETs and NMOSFETs are connected to VBP and VBN to control body biases.

III. BTI SUPPRESSION SCHEME AT CONSTANT PERFORMANCE

We investigate the bias conditions of supply voltage (VDD) and body bias (VBB) at which the oscillation frequency of ROs is constant by circuit simulations. Fig. 3 shows various bias conditions of VDD and VBB when RO's oscillation frequency is constant. Note that VDD is swept around the nominal voltage of 0.75 V, and the temperature is 27°C.

By controlling VDD and VBB, leakage current and dynamic power consumption are also varied. Fig. 4 shows the simulation results of leakage current and dynamic power

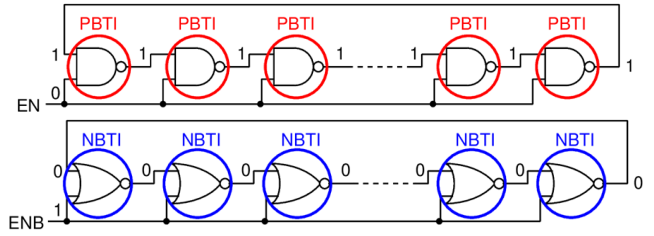


Fig. 1: RO composed NAND or NOR NBTI gates called NAND-PBTI RO and NOR-NBTI RO.

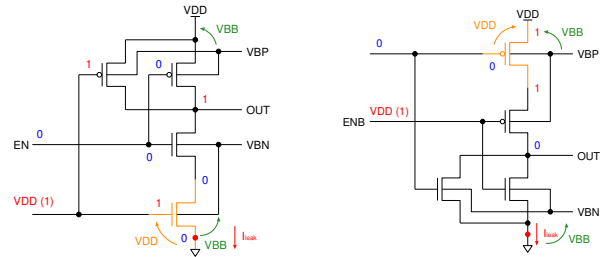


Fig. 2: Bias conditions of NAND gate (left) and NOR gate (right) when ROs stop oscillation.

consumption. Leakage current increases exponentially and dynamic power consumption decreases linearly.

IV. TEST CHIP IN A 65 NM FDSOI AND MEASUREMENT PROCEDURE

The NAND-PBTI and NOR-NBTI ROs are implemented in a 65 nm thin BOX FDSOI process that can control body bias through a thin BOX layer [3]. Each RO has 11 stages and a chip contains 490 of each RO. It has an embedded 16 bit counter to store the number of oscillations. Fig. 5 shows the measurement flow. When the ROs are exposed to stress, VDD is increased to accelerate BTI-induced degradation and

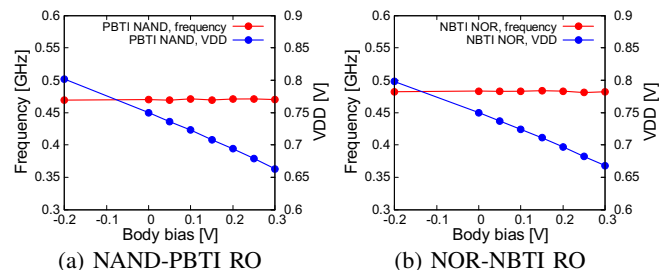


Fig. 3: Supply voltage and body bias when the oscillation frequency of ROs is constant.

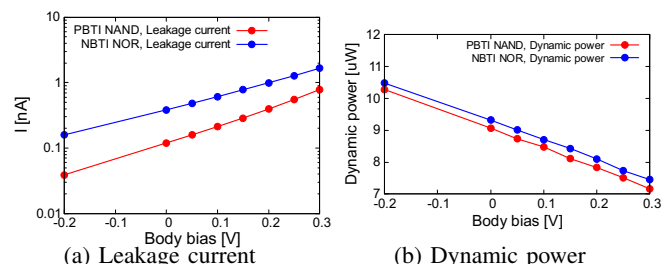


Fig. 4: Simulation results.

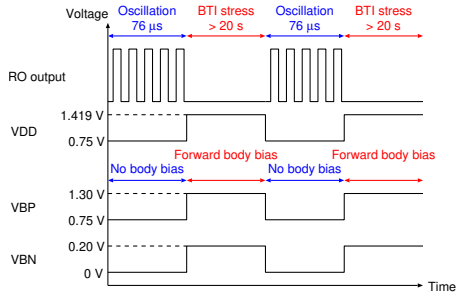
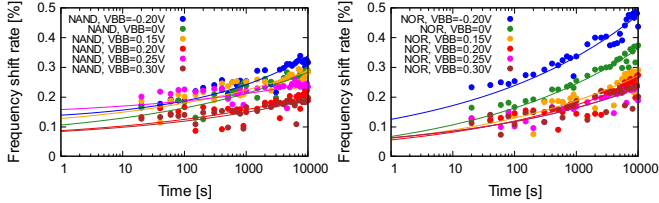


Fig. 5: Measurement flow when VDD = 1.419 V.



(a) NAND-PBTI ROs

(b) NOR-NBTI ROs

Fig. 6: Measurement results of aging degradation at the bias condition in Table I.

VBB (= VBN on NMOS and = VDD-VBP on PMOS) is varied to equalize oscillation frequency. In order to accelerate degradation due to BTI, VDD is swept around 1.5 V and the temperature is set to 120 °C. When the ROs oscillate, VDD, VBP and VBN are set to the standard voltages (VDD = VBP = 0.75 V, VBN = 0 V) to compare degradation at the same operating condition.

The ROs oscillate for 76 μs at few hundreds of megahertz at 0.75 V. They stop oscillation for over 20 s to expose BTI stress. In this measurement scheme, BTI-induced degradation becomes more dominant than the hot carrier injection (HCI) because the ROs only oscillate during a short period. Frequency shift rate is calculated as $(f_0 - f(t))/f_0$, where f_0 is the initial frequency at $t = 0$ and $f(t)$ is the measured frequency at time t .

V. MEASUREMENT RESULTS

Fig. 6 shows measured BTI-induced degradations of the PBTI-NAND and NBTI-NOR ROs. BTI-induced degradation is suppressed by lowering VDD and applying the forward body bias (FBB, VBB > 0), and accelerated by increasing VDD and applying the reverse body bias (RBB, VBB < 0). The measured data are fitted by an power-law function described as $A t^n + B$, where t is the stress time, A and B are fitting parameters. Here we fix the time exponent n to 0.16 [4].

When VBB = 0.15 V, 0.20 V, NBTI-induced degradations at 10,000 s are suppressed by 22%. When VBB = 0 V, 0.15 V, PBTI-induced degradations at 10,000 s are almost equivalent. But when VBB = 0.20 V, it is suppressed by 14%.

Table I shows the ratios of frequency shift of the PBTI-NAND RO to the NBTI-NOR RO at 10,000 s. At VBB = 0.15 V, the degradation at 10,000 s due to NBTI and PBTI becomes almost equivalent (NBTI/PBTI = 1.02).

Table II compares BTI degradation (A), leakage current (I), and dynamic power consumption (P) at each body bias. The BTI degradation is compared with the parameter A . If A is larger, more BTI degradation is observed. When VBB = 0.15 V, A , I and P of the PBTI-NAND RO becomes 0.90x, 2.40x and 0.89x of those at VBB = 0 V. In the NBTI-NOR RO, (A , I , P) becomes (0.71x, 2.03x, 0.89x). At VBB = 0.15 V, the NBTI-NOR RO can suppress NBTI by 29%, while the PBTI-NAND RO can suppress PBTI by 10%.

TABLE I: Ratio of frequency shift (NBTI-NOR RO/PBTI-NAND RO) at 10,000 s.

VDD [V]	1.582	1.500	1.441	1.419	1.397	1.375
VBB [V]	-0.20	0	0.15	0.20	0.25	0.30
PBTI [%]	0.316	0.287	0.286	0.188	0.234	0.198
NBTI [%]	0.437	0.374	0.290	0.273	0.189	0.202
NBTI/PBTI	1.38	1.30	1.02	1.45	0.81	1.02

TABLE II: Fitting parameter A , leakage current I , and dynamic power P normalized to those at VBB = 0 V.

NAND-PBTI	Body bias [V]					
	-0.20	0	0.15	0.20	0.25	0.30
A	1.25	1.00	0.90	0.66	0.51	0.60
I	0.32	1.00	2.40	3.29	4.60	6.54
P	1.13	1.00	0.89	0.86	0.83	0.79

NOR-NBTI	Body bias [V]					
	-0.20	0	0.15	0.20	0.25	0.30
A	1.19	1.00	0.71	0.66	0.57	0.57
I	0.41	1.00	2.03	2.59	3.32	4.33
P	1.13	1.00	0.89	0.86	0.83	0.79

TABLE III: Frequency shift at 10^5 s and 10 years later.

VDD [V]	0.750	0.708	0.694	0.678	0.662
VBB [V]	0	0.15	0.20	0.25	0.30
NBTI (at 10^5 s) [%]	0.095	0.068	0.062	0.059	0.058
NBTI (10 years later) [%]	0.188	0.124	0.109	0.094	0.091

VDD [V]	1.200	1.148	1.128	1.109	1.089
VBB [V]	0	0.15	0.20	0.25	0.30
NBTI (at 10^5 s) [%]	0.267	0.179	0.158	0.139	0.134
NBTI (10 years later) [%]	0.798	0.474	0.397	0.297	0.283

Table III estimates NBTI degradation at 10^5 s and 10 years later. The NBTI degradations at VDD = 0.75 V (the standard voltage on the 65 nm FDSOI process), 1.2 V (nominal voltage in a 65 nm bulk process) scaled from measurement results at VDD = 1.5 V and the equation $C \times \exp(VDD) \times t^D \times \exp(E/T)$, where C , D and E are fitting parameters and T is absolute temperature [5]. At $t = 10^5$, the NBTI degradation at VBB = 0.15 V becomes 0.72x at VDD = 0.75 V and 0.67x at VDD = 1.2 V smaller than that at VBB = 0 V. After 10 years, the NBTI degradation at VBB = 0.15 V becomes 0.66x at VDD = 0.75 V and 0.59x at VDD = 1.2 V smaller than that at VBB = 0 V.

VI. CONCLUSIONS

The aging degradation suppression scheme at constant performance by controlling supply voltage and body bias is proposed. Measurement results in the 65 nm FDSOI process clearly shows the aging degradation due to NBTI and PBTI are suppressed by 0.71x and 0.90x and the dynamic power consumption becomes 0.89x when the body bias (VBB) is 0.15 V although the leakage current increases by around 2x. At VBB = 0.15 V and VDD = 1.441 V, NBTI and PBTI degradation becomes almost equivalent at 10,000 s. At 0.75 V and 1.2 V, NBTI degradations at 0.15 V forward body bias can be suppressed to 0.66x and 0.59x of those at 0 V body bias, respectively.

REFERENCES

- [1] T. Grasser, et. al, *IEEE Trans. on Elec. Dev.*, vol. 58, pp. 3652-3666, 2011, [2] R. Kishida, et. al, *IEEE Trans. on Semi. Man.*, vol. 33, no. 2, pp. 174-179, 2020, [3] Y. Morita, et. al, *VLSI Tech. Symp.*, pp. 166-167, 2008, [4] S. Mahapatra, et. al, IRPS, 3B.1, 2014, [5] M. M. Gourary, et. al, EWDTs, pp. 1-4, 2019