

Bias Temperature Instability Depending on Body Bias through Buried Oxide (BOX) Layer in a 65 nm Fully-Depleted Silicon-On-Insulator Process

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Abstract— Bias temperature instability (BTI) depending on body bias through the buried oxide (BOX) layer was measured using ring oscillators at nominal gate-source voltage. BTI through the BOX layer becomes dominant on OFF-state transistors by applying reverse body bias (RBB) even at nominal gate-source voltage. BTI-induced degradation is accelerated by RBB, which is opposite to previous results at which only ON-state transistors were measured. The degradation rate at 1.0 V RBB is more than 5x larger than that in zero body bias.

Index Terms—bias temperature instability (BTI), reverse body bias (RBB), ring oscillator (RO)

I. INTRODUCTION

Shrinking device sizes of semiconductor chips has brought a lot of advantages. For example, low power consumption and high performance electric gadgets are developed and most of people are using those gadgets. Device structure development such as the fully-depleted silicon-on-insulator (FDSOI) and FinFET process technologies also contributes useful electric devices [1]. Particularly, the body bias control on a thin-buried-oxide (BOX) FDSOI process is useful for high performance with low power [2]. Forward body bias decreases threshold voltage (V_{th}) and transistors operate at higher speed. On the other hand, V_{th} is increased and leakage current is decreased when reverse body bias (RBB) is applied. The RBB is useful for stand-by mode.

Reliability problems such as bias temperature instability (BTI) has become a significant concern with the miniaturization of the device size [3]. Transistor performance is degrading with time due to BTI, which results in decreasing timing margins of implemented circuits. V_{th} increases with time due to BTI and decreases oscillation frequency in ring oscillator (RO) [4], [5]. BTI depends on measurement conditions and circuit

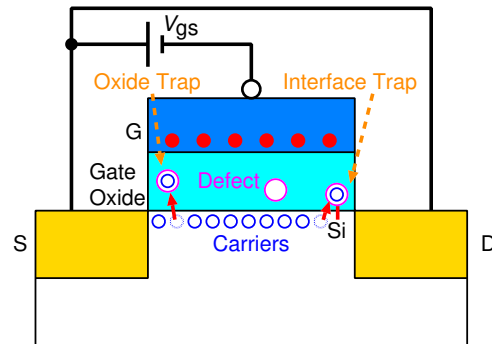


Fig. 1. Atomistic trap-based BTI (ATB) model. BTI occurs when defects trap carriers.

topologies. It is important to measure and analyze BTI-induced degradation to clarify the mechanism of BTI.

Previous researches evaluated BTI-induced degradation depending on body bias [6]–[11]. A lot of BTI-induced degradation caused by body bias are measured and valuable data. However, those measurements focused on the degradation in the gate oxide. BTI occurs through the gate oxide by gate bias and also through the thin-BOX layer by body bias in thin-BOX FDSOI process technologies. In this paper, BTI-induced degradations by body bias through the thin-BOX layer are evaluated using ring oscillators (ROs) fabricated in the 65 nm thin-BOX FDSOI including ON- and OFF-state transistors at nominal gate-source voltage (V_{gs}).

II. BTI AND BODY BIAS

BTI is one of the aging degradations [12]. BTI-induced degradation occurs when defects trap carriers as shown in Fig. 1. This degradation can be explained by the atomistic trap-based BTI (ATB) model [13]. There are

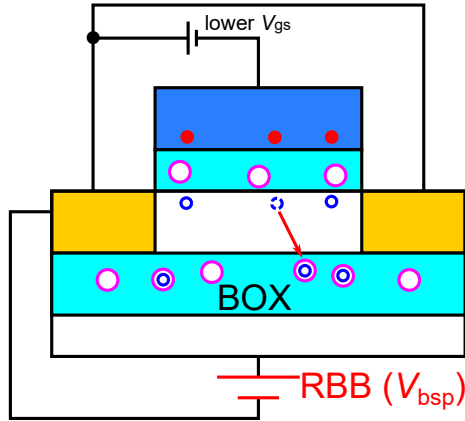


Fig. 2. BTI by RBB. Carriers are trapped in the gate oxide and also in the BOX layer by RBB.

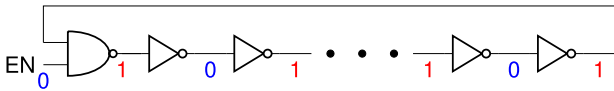


Fig. 3. RO composed inverter gates.

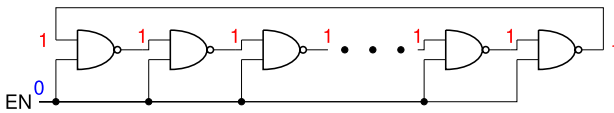


Fig. 4. RO composed NAND gates. All outputs and gate voltage are fixed to VDD (= 1) when RO stops.

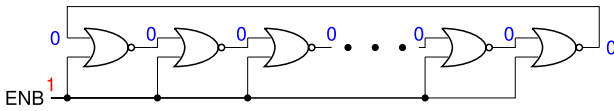


Fig. 5. RO composed NOR gates. All outputs and gate voltage are fixed to GND (= 0) when RO stops.

oxygen vacancy defects in the gate oxide and dangling bonds in the interface between the gate oxide and silicon substrate. When these defects trap carriers, the electric field in the gate oxide decreases and drain-source current decreases. Each defect has an individual time constant to trap a carrier. Those time constants are distributed from 10^{-9} s to 10^9 s [14]. Particularly, defects with large time constants affect aging degradations induced by BTI. BTI-induced degradation is recovered when carrier emission is promoted as V_{gs} is reduced because trapped carriers in the gate oxide are easily emitted to channel. Previous researches measured BTI depending on body bias. RBB accelerates BTI-induced degradation at constant operating speed in a discrete transistor since V_{gs} must be increased to keep operating speed when RBB

is increased [7]. A lot of carriers are trapped to the gate oxide at higher V_{gs} . On the other hand, RBB suppressed the degradation at constant V_{gs} in ROs because carriers in channel decreases by RBB and probability to be trapped in the gate oxide is decreased [8]. Other researches showed no correlation between BTI-induced degradation and body bias [9], [10]. However, these previous researches focused on BTI through the gate oxide. There is the thin-BOX layer to trap carriers under the drain/source in the thin-BOX FDSOI process as shown in Fig. 2. Since the electric field inside the thin-BOX layer depends on body bias, BTI-induced degradation also depends on the body bias.

III. MEASUREMENT SETUP

Fig. 3 shows an inverter-based RO. It oscillates when EN is high and stops oscillation when EN is low. BTI occurs when the RO stops because constant gate-source voltage (V_{gs}) is applied.

Figs. 4 and 5 show NAND RO and NOR RO, respectively. When EN is low and ENB is high, all outputs are fixed to 0 or 1, respectively and the ROs suffer from BTI. These ROs oscillate during frequency measurement. The oscillation frequency is decreased when the V_{th} of those transistors is degraded.

Figs. 6-8 show these ROs in the transistor level. In the inverter-based RO (Fig. 6), the PMOS transistor is alternately in ON- and OFF-state during stress. In NAND RO (Fig. 7), the left PMOS transistor is in OFF-state during stress. In NOR RO (Fig. 8), the bottom PMOS transistor is in OFF-state during stress.

BTI depending on body bias is measured by changing body bias of PMOS (V_{bsp}) or NMOS (V_{bsn}). When BTI depending on V_{bsp} is measured, V_{bsn} is fixed to ground (GND). Likewise, V_{bsp} is fixed to supply voltage (VDD) during measurements of V_{bsn} dependence.

Fig. 9 shows a test chip fabricated in the 65 nm thin-BOX FDSOI process. Note that the thickness of the BOX layer is about 15 nm that is thin enough to apply body bias. The 3×2 mm² chip has 126×4 11-stage ROs. The number of oscillations are stored in the 16-bit counters and average oscillation frequencies are obtained by dividing oscillation time (28 μ s).

Our measurement system is shown in Fig. 10. The test chip (device under test, DUT) is measured by an LSI tester (Griffin, HILEVEL Technology, Inc.). An external power supply (N6700B, Keysight Technologies) and a peltier module (CTS-01A, ATE Service Corporation) are used to control bias and temperature stress, respectively.

Fig. 11 shows a flow to measure BTI-induced degradations. ROs oscillate for only 28 μ s in the order of few hundreds of megahertz at 0.85 V. They stop oscillation for over 20 s for BTI stress after measuring frequencies. BTI is the most dominant degradation compared with hot carrier injection (HCI) because ROs stop most of the

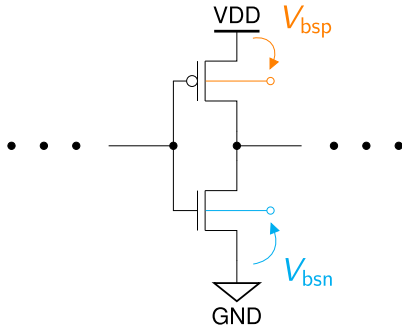


Fig. 6. Inverter-based RO in transistor level. BTI-induced degradation is measured with changing body bias of PMOS (V_{bsp}) or that of NMOS (V_{bsn}).

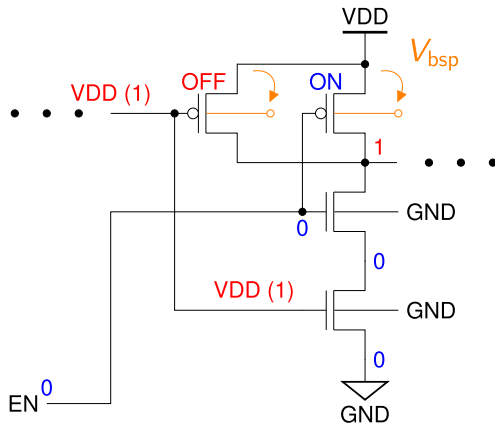


Fig. 7. NAND RO in transistor level during stress when BTI depending on V_{bsp} is measured (V_{bsn} is GND).

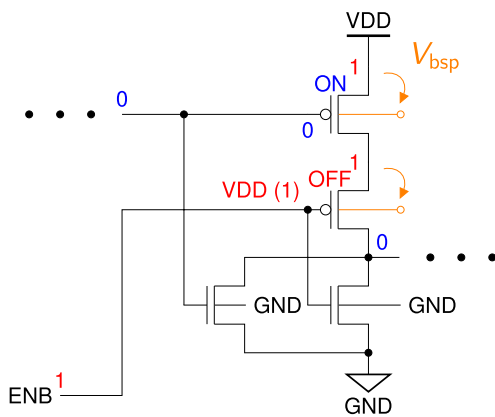


Fig. 8. NOR RO in transistor level during stress.

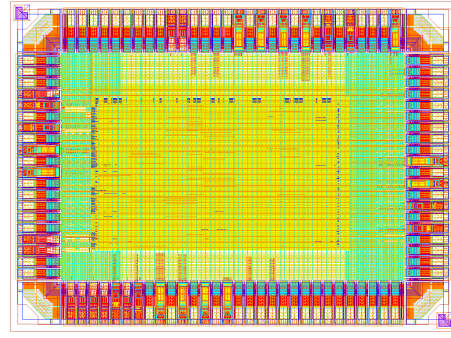


Fig. 9. Test chip fabricated by the 65 nm thin-BOX FDSOI process. The number of oscillations is counted by embedded 16-bit counters.

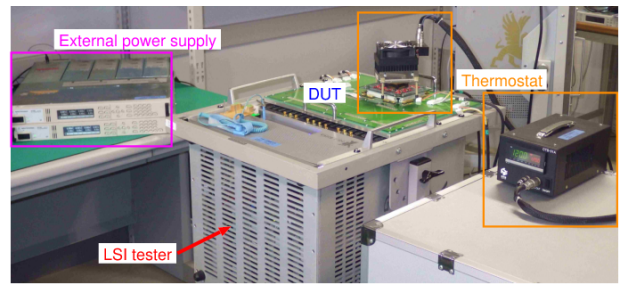


Fig. 10. Measurement system. Test chip (Device Under Test, DUT) is measured by LSI tester. Voltage is supplied by external power supply and temperature is fixed by peltier module with temperature controller.

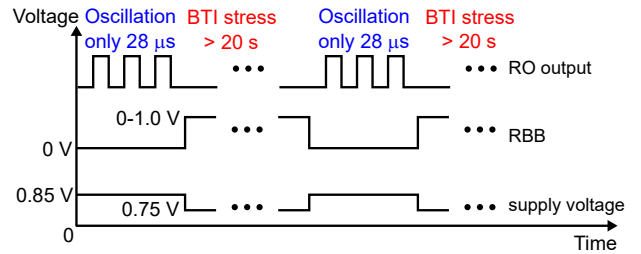


Fig. 11. Measurement flow. Supply voltage (V_{gs}) is nominal to measure BTI through BOX layer.

measurement time. The oscillation and BTI stress are repeated. The measurements are performed at 120 °C to accelerate BTI-induced degradation. Supply voltage is kept at nominal voltage of 0.75 V to suppress BTI-induced degradation caused by gate bias. Frequency shift rate (R_{freq}) is calculated as

$$R_{freq} = \frac{F_0 - F(t)}{F_0}, \quad (1)$$

where F_0 is the initial frequency at $t = 0$ and $F(t)$ is the measured frequency at time t .

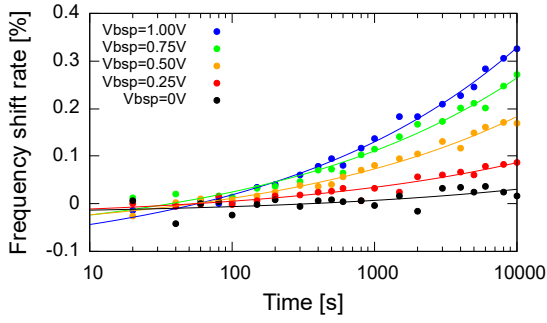


Fig. 12. Measurement results of inverter ROs.

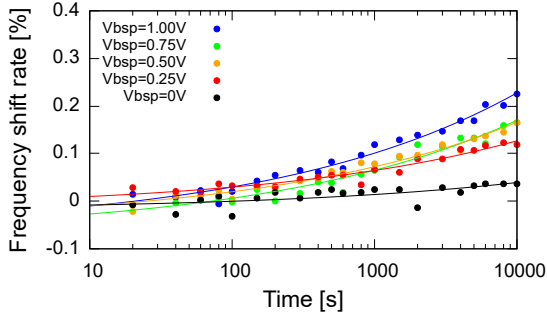


Fig. 13. Measurement results of NAND ROs.

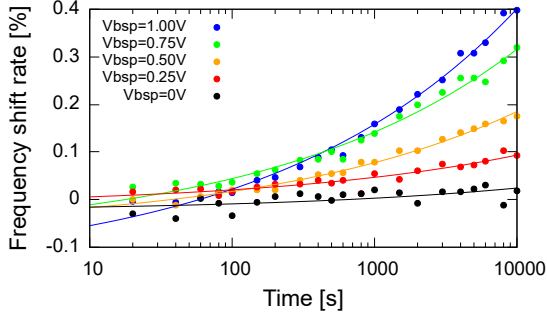


Fig. 14. Measurement results of NOR ROs.

IV. MEASUREMENT RESULTS AND DISCUSSIONS

Fig. 12 shows the measured BTI-induced degradations of inverter-based ROs. The X-axis and the Y-axis show the BTI stress time and R_{freq} , respectively. R_{freq} is averaged in 126 ROs. Measured data are fitted by Eq. (2):

$$f(t) = At^n + B, \quad (2)$$

where t is the stress time, A and B are fitting parameters, and n is a time exponent.

BTI-induced degradation is larger as RBB is higher. R_{freq} at 10 ks is 10x larger on 1.0 V RBB compared with on zero RBB condition.

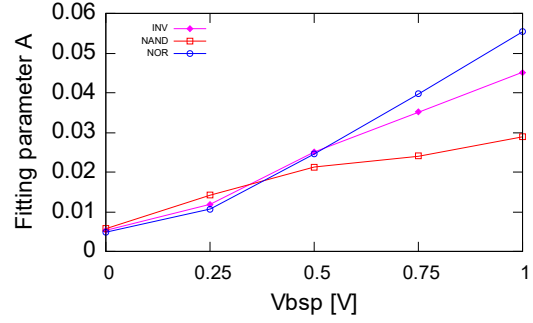


Fig. 15. Fitting parameter A and V_{bsp} . A indicating the degradation increases as RBB increases.

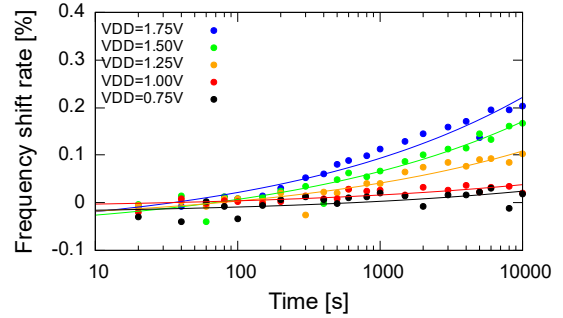


Fig. 16. Measurement results of **supply voltage dependence** in NOR ROs. BTI caused by VDD is less than that by RBB.

Figs. 13 and 14 show measured BTI-induced degradations of the NAND and NOR ROs, respectively. RBB accelerates the degradation in both results similar to the result of the inverter-based RO.

Fig. 15 shows the fitting parameter A and V_{bsp} in all ROs. Since A represents the factor of BTI-induced degradation, 1.0 V RBB accelerates BTI-induced degradation by more than 5x from zero RBB.

Previous researches in [9], [10] suggest that RBB does not promote BTI. However, they only focused on BTI by RBB in ON-state PMOS transistors. In our measurements, BTI on OFF-state PMOS transistors by RBB is measured with lower V_{gs} . In the NOR RO, the left PMOS transistor which is in OFF-state during stress. It means that OFF-state PMOS transistor suffers from BTI by RBB. The degradation becomes the largest in the NOR RO since the drain voltage of the OFF-state bottom PMOS transistor is 0, while that of the OFF-state left PMOS transistor is VDD in the NAND RO. The degradation of the inverter-based RO is between those of the NOR and NAND ROs since the PMOS transistor is alternately in ON- and OFF-state during stress. We assume that RBB promotes carrier traps in the BOX layer in OFF-state transistors.

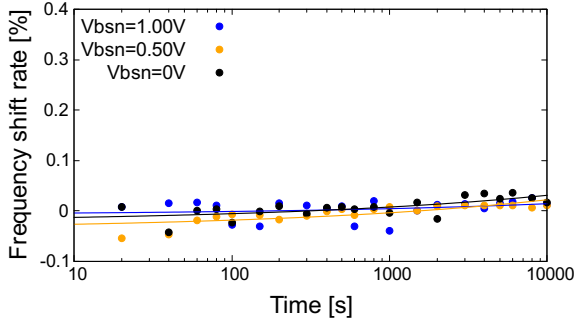


Fig. 17. Measurement results of V_{bsn} dependence in inverter ROs.

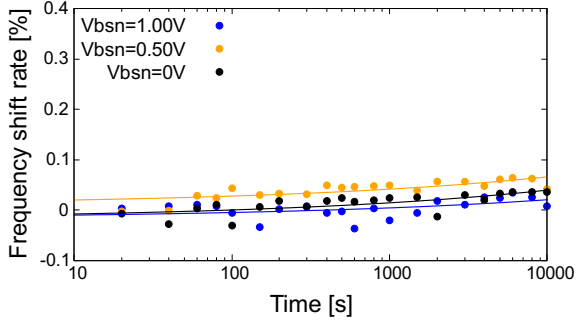


Fig. 18. Measurement results of V_{bsn} dependence in NAND ROs.

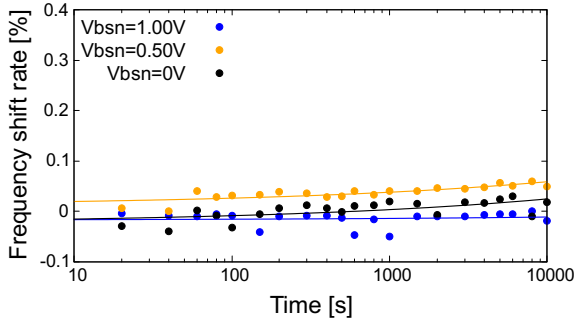


Fig. 19. Measurement results of V_{bsn} dependence in NOR ROs.

Fig. 16 shows supply voltage dependence in the NOR ROs. The degradation is half of body bias dependence in Fig. 14. BTI by body bias is more dominant than that by supply voltage.

Figs. 17-19 show measured BTI-induced degradations depending on NMOS reverse body bias (V_{bsn}) of the inverter-based, NAND and NOR ROs, respectively. Because R_{freq} is less than 0.1% at 10 ks in any V_{bsn} , there is no correlation between the degradation and V_{bsn} in all results. Fig. 20 shows the fitting parameter A and V_{bsn} in all ROs. BTI in NMOS through the BOX layer is not dominant similar to BTI through the gate oxide.

Figs. 21 and 22 show measurement results of forward

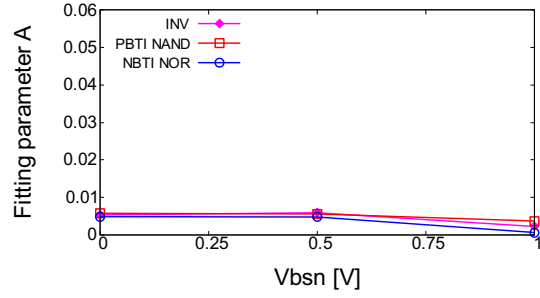


Fig. 20. Fitting parameter A and V_{bsn} . BTI-induced degradation is not accelerated by NMOS reverse body bias.

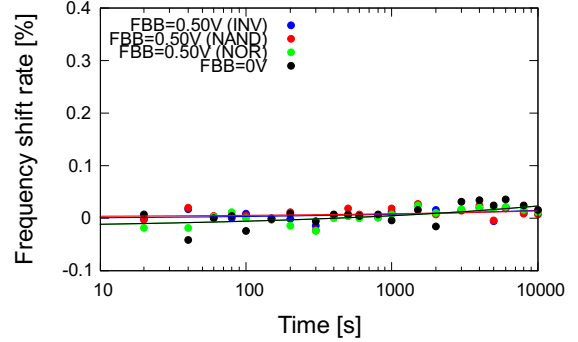


Fig. 21. Measurement results of forward body bias (FBB) in PMOS.

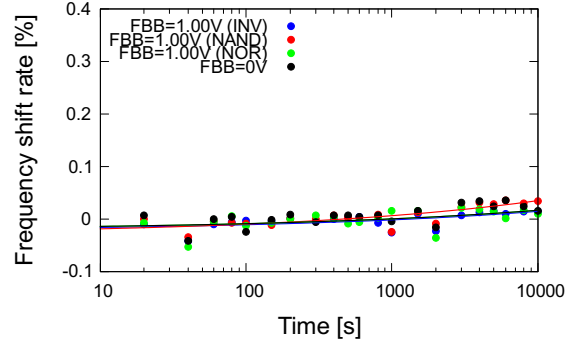


Fig. 22. Measurement results of forward body bias (FBB) in NMOS.

body bias (FBB) in PMOS and NMOS, respectively. The degradation by FBB is small enough similar to the result of NMOS reverse body bias. BTI-induced degradation through the BOX layer should be considered in the thin-BOX FDSOI process when RBB is applied.

V. CONCLUSIONS

BTI-induced degradation by reverse body bias is measured in the 65 nm FDSOI process. Reverse body bias (RBB) accelerates BTI-induced degradations in OFF-state PMOS transistors. The degradation at 1.0 V RBB is more than 5x larger than that at zero body bias. Although leak current is decreased by RBB, BTI-induced

degradation is accelerated through the BOX layer at OFF-state condition. RBB in NMOS and FBB do not affect to the degradation. PMOS BTI by RBB becomes dominant even in OFF-states.

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REFERENCES

- [1] K. J. Kuhn, "CMOS Scaling for the 22nm Node and Beyond: Device Physics and Technology," *Symposium on VLSI Technology*, pp. 1–2, April 2011.
- [2] R. Tsuchiya, M. Horiuchi, S. Kimura, M. Yamaoka, T. Kawahara, S. Maegawa, T. Ipposhi, Y. Ohji, and H. Matsuoka, "Silicon on Thin BOX: A New Paradigm of The CMOSFET for Low-Power High-Performance Application Featuring Wide-Range Back-Bias Control," *IEEE International Electron Devices Meeting (IEDM)*, pp. 631–634, Dec. 2004.
- [3] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P.-J. Wagner, F. Schanovsky, J. Franco, M. T. Luque, and M. Nelhiebel, "The Paradigm Shift in Understanding the Bias Temperature Instability: From Reaction-Diffusion to Switching Oxide Traps," *IEEE Transactions on Electron Devices*, vol. 58, pp. 3652–3666, Nov. 2011.
- [4] R. Kishida, A. Oshima, and K. Kobayashi, "Negative Bias Temperature Instability Caused by Plasma Induced Damage in 65 nm Bulk and Silicon on Thin BOX (SOTB) Processes," *IEEE International Reliability Physics Symposium (IRPS)*, pp. CA.2.1–CA.2.5, April 2015.
- [5] W. H. Choi, S. Satapathy, J. Keane, and C. H. Kim, "A Test Circuit Based on a Ring Oscillator Array for Statistical Characterization of Plasma-Induced Damage," *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2014. p.14-3.
- [6] J. Franco, B. Kaczer, M. Toledano-Luque, P. J. Roussel, G. Groeseneken, B. Schwarz, M. Bina, M. Waltl, P. J. Wagner, and T. Grasser, "Reduction of the BTI Time-Dependent Variability in Nanoscaled MOSFETs by Body Bias," *IEEE International Reliability Physics Symposium (IRPS)*, pp. 2D.3.1–2D.3.6, April 2013.
- [7] J. Franco, B. Kaczer, G. Eneman, P. J. Roussel, T. Grasser, J. Mitard, L. A. Ragnarsson, M. Cho, L. Witters, T. Chiarella, M. Togo, W. E. Wang, A. Hikavy, R. Loo, N. Horiguchi, and G. Groeseneken, "Superior NBTI Reliability of SiGe Channel pMOSFETs: Replacement Gate, FinFETs, and Impact of Body Bias," *IEEE International Electron Devices Meeting (IEDM)*, pp. 18.5.1–18.5.4, Dec. 2011.
- [8] R. Kishida and K. Kobayashi, "Degradation Caused by Negative Bias Temperature Instability Depending on Body Bias on NMOS or PMOS in 65 nm Bulk and Thin-BOX FDSOI Processes," *IEEE Electron Devices Technology and Manufacturing Conference (EDTM)*, pp. 122–123, March 2017.
- [9] P. Mora, X. Federspiel, F. Cacho, V. Huard, and W. Arfaoui, "28nm UTBB FDSOI product reliability/performance trade-off optimization through body bias operation," *IEEE International Reliability Physics Symposium (IRPS)*, pp. 6B.1.1–6B.1.5, April 2015.
- [10] T. Ishigaki, R. Tsuchiya, Y. Morita, N. Sugii, and S. Kimura, "Effects of Device Structure and Back Biasing on HCI and NBTI in Silicon-on-Thin-BOX (SOTB) CMOSFET," *IEEE Transactions on Electron Devices*, vol. 58, pp. 1197–1204, April 2011.
- [11] R. Faraji and H. R. Naji, "Adaptive Technique for Overcoming Performance Degradation Due to Aging on 6T SRAM Cells," *IEEE Transactions on Device and Materials Reliability*, vol. 14, pp. 1031–1040, Dec. 2014.
- [12] R. Kishida, T. Asuke, J. Furuta, and K. Kobayashi, "Extracting Voltage Dependence of BTI-induced Degradation Without Temporal Factors by Using BTI-Sensitive and BTI-Insensitive Ring Oscillators," *IEEE Transactions on Semiconductor Manufacturing*, vol. 33, pp. 174–179, May 2020.
- [13] H. Kukner, S. Khan, P. Weckx, P. Raghavan, S. Hamdioui, B. Kaczer, F. Catthoor, L. V. der Perre, R. Lauwereins, and G. Groeseneken, "Comparison of Reaction-Diffusion and Atomistic Trap-Based BTI Models for Logic Gates," *IEEE Transactions on Device and Materials Reliability*, vol. 14, pp. 182–193, March 2014.
- [14] B. Kaczer, S. Mahato, V. V. de Almeida Camargo, M. Toledano-Luque, P. J. Roussel, T. Grasser, F. Catthoor, P. Dobrovolny, P. Zuber, G. Wirth, and G. Groeseneken, "Atomistic Approach to Variability of Bias-Temperature Instability in Circuit Simulations," *IEEE International Reliability Physics Symposium (IRPS)*, pp. XT.3.1–XT.3.5, April 2011.