An Accurate Device-Level Simulation Method to Estimate Cross Sections of Single Event Upsets by Silicon Thickness in Raised Layer

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***Abstract*— An accurate device-level simulation method to estimate cross sections (CS) of single event upsets for a standard latch is proposed. CS from the proposed method is compared with experimental results by heavy ions on a fabricated chip in a 65 nm FDSOI. Silicon thickness below silicide is parameterized to make CS coincident between simulation and measurement results. Silicon thickness is highly correlated to soft-error tolerance. By increasing silicon thickness, simulation results becomes closer to the measurement results. Device simulation results show that the cross section is proportional to the silicon thickness in the raised layer below silicide.**

***Index Terms*— single event effect, soft error, heavy ion irradiation, FDSOI, flip flop, device simulation, NMOS, PMOS.**

I. Introduction

Aggressive process scaling down to 7 nm launches high-performance devices including billions of transistors working at low power. The radiation-induced soft error becomes a serious reliability issue in those high performance devices for mission critical applications. Storage elements such as flip flops (FFs) or latches must be protected from soft errors on reliable applications for terrestrial region and outer space.

For a device-level radiation-hardened technology, fully-depleted silicon on insulator (FDSOI) is strong against soft errors with relatively lower cost than FinFET [1], [2]. A buried oxide (BOX) layer is formed between substrate and transistor regions. The BOX layer prevents charge collection that is generated by drift and funneling from the substrate. Charge collection is dominant mechanism causing soft error in bulk devices, while in FDSOI the parasitic bipolar effect (PBE) is dominant [3]. Figure 1 shows how holes are generated in the diffusion region and collected to the channel region. PBE turns on the parasitic bipolar transistor under the channel to cause a flip of a memory storage cell such as an SRAM cell or a latch.

Drain and source surface on MOSFETs is covered by silicide to reduce resistance. First silicon layer then silicide are formed by deposition. They are called the raised drain and source region. In this paper, we refer to the raised drain and source regions as the raised layer. Figure 2 shows the structure of the raised layer which consists of silicon and nickel silicide. Those thicknesses are defined as T_{S} and T_{N} respectively. In the FDSOI process, charge is collected only above the BOX layer. The structure of the raised layer severely affects the amount of charge generated by a particle strike [4].

In this paper, soft-error tolerance depending on the silicon thickness in the raised layer is evaluated by device simulations and heavy ion irradiation. This paper is organized as follows. Section II shows device simulation setup of cross sections in a 65 nm FDSOI process. In Section III, device simulation results are shown. In Section IV, shows experimental results and compare with simulation results. Finally, we describe the effectiveness of silicon thickness and the importance of radiation hardness in PMOS transistor.

II. Simulation Setup

A 3D model for TCAD simulations is constructed according to the device structure in a 65 nm FDSOI. In this paper, we use a commercial TCAD simulation tool, Synopsys Sentaurus.

Figure 3 shows cross-sectional views of an NMOS transistor and the schematic diagrams of a standard transmission-gate latch. The three NMOS transistors in the latch are implemented by 3D models and the other transistors are by circuit-level models to shorten simulation time. The 3D models are constructed to match the SPICE models which are calibrated with the fabricated devices from [5]. The capacitance-voltage (C_{gg}-V_{gs}) and current-voltage (I_{ds}-V_{gs}) of the transistor are shown in Fig. 4. Characteristics on

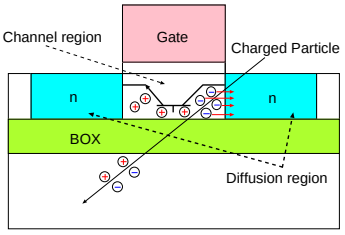


Fig. 1. Holes generated in the diffusion region are collected in the channel region and then drain-body-source parasitic bipolar transistor turns on.

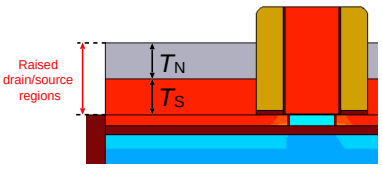


Fig. 2. Structure of the raised layer. Definition of thickness of silicon (T_{S}) and thickness of nickel silicide (T_{N}).

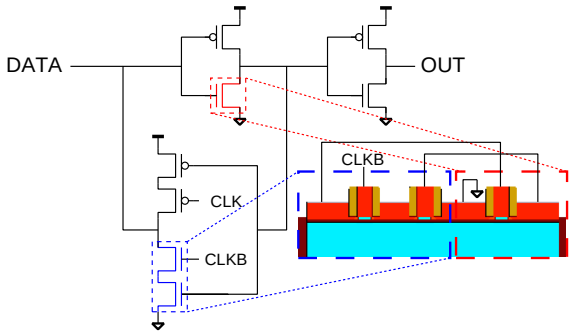
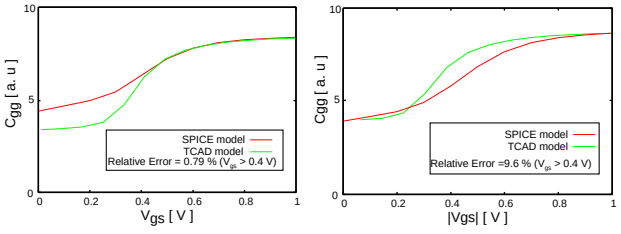
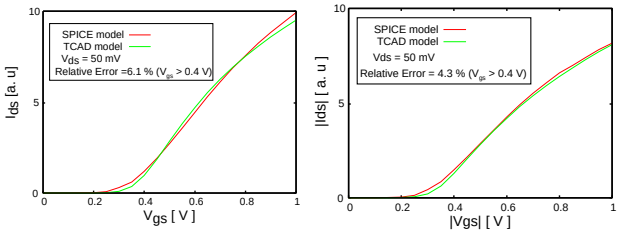


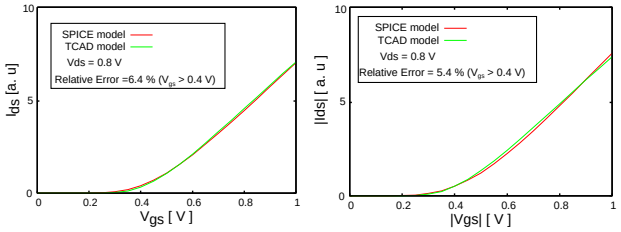
Fig. 3. Schematic diagram and the cross-sectional view of the 3D model used for device simulations.



(a) $C_{\rm gg}$-$V_{\rm gs}$



(b) $I_{\rm ds}$-$V_{\rm gs}$ at linear region ($V_{\rm ds}$ = 50 mV.)



(c) $I_{\rm ds}$-$V_{\rm gs}$ at saturation region ($V_{\rm ds}$ = 0.8 V)

Fig. 4. (a) Simulated $C_{\rm gg}$-$V_{\rm gs}$ characteristics at $V_{\rm ds}$ = 0 V. (b) Simulated $I_{\rm ds}$-$V_{\rm gs}$ characteristics at linear region. (c) Simulated $I_{\rm ds}$-$V_{\rm gs}$ characteristics at saturation region.

TCAD simulations are optimized to decrease the relative error between TCAD simulations and SPICE simulations to less than 9.6 % in the region of $|V_{\rm gs}| > 0.4$ V. We also constructed the latch with PMOS transistors in 3D device level and NMOS transistors in the circuit level.

Heavy ions with linear energy transfer (LET) of 15.7 or 40.3 MeV-cm^2/mg strikes vertically on the 3D-model transistor. Those LET values are from Ar and Kr ions which

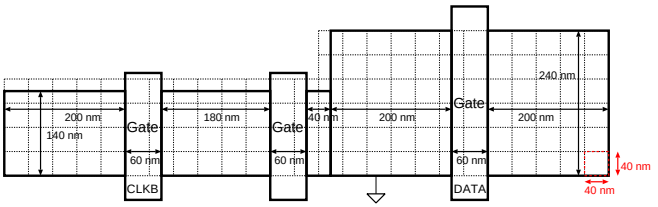
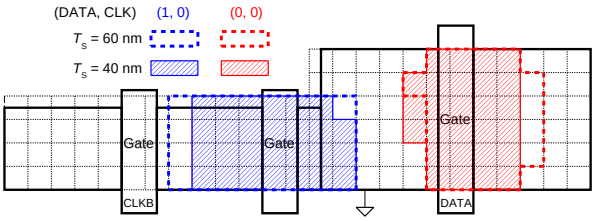
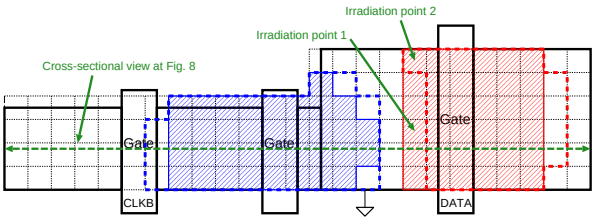


Fig. 5. Simulation setup to evaluate cross sections induced by a heavy ion with Ar and Kr. Radiation particles strike at the center of each grid.



(a) Ar irradiation



(b) Kr irradiation

Fig. 6. Cross section from device simulation results in NMOS.

TABLE I

CROSS SECTION OF NMOS FROM DEVICE SIMULATIONS.

Heavy Ion	Cross Section [cm^2/ion]			
	$T_{\rm S}$ = 40 nm		$T_{\rm S}$ = 60 nm	
	DATA = 0	DATA = 1	DATA = 0	DATA = 1
Ar	4.36×10^{-10}	4.36×10^{-10}	4.64×10^{-10}	5.12×10^{-10}
Kr	5.76×10^{-10}	5.60×10^{-10}	5.60×10^{-10}	6.56×10^{-10}

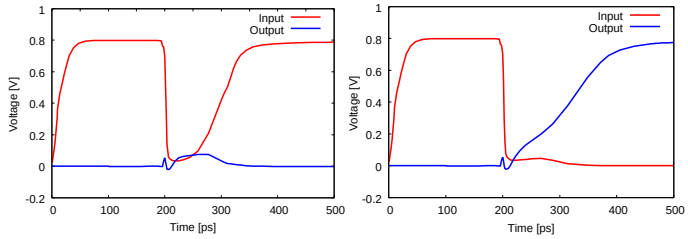
were used during experimental measurement. The track radius to generate electron-hole pairs is 50 nm. Even with heavy ion irradiation of 50 nm track radius, it is characteristic parameter. Electrons and holes generated by irradiation drift and diffuse. The drift and diffusion depends on the shape of the drain and source regions. Heavy ions are irradiated every 40 nm grid to calculate CS as shown in Fig. 5. (DATA, CLK) is fixed to (0, 0) or (1, 0) and $V_{\rm DD}$ is 0.8 V. CS from NMOS and PMOS transistors are summed up.

Simulations are performed by fixing $T_{\rm N}$ to 5 nm and changing $T_{\rm S}$ from 40 to 60 nm since we confirmed by device simulation that $T_{\rm N}$ does not change radiation hardness.

III. Simulation Results

Figure 6 and Table I show the device simulation results of NMOS transistors to evaluate CS by Ar (a) and Kr (b). CS increases as silicon thickness of the raised layer decreases.

The NMOS transistor covered by red rectangles becomes sensitive to a particle hit at DATA = 0 because it is off.



(a) Flip at T_S = 40 nm (b) Does not flip at T_S = 60 nm

Fig. 7. DATA and OUT voltage of the tristate inverter.

TABLE II

CROSS SECTION OF PMOS FROM DEVICE SIMULATIONS.

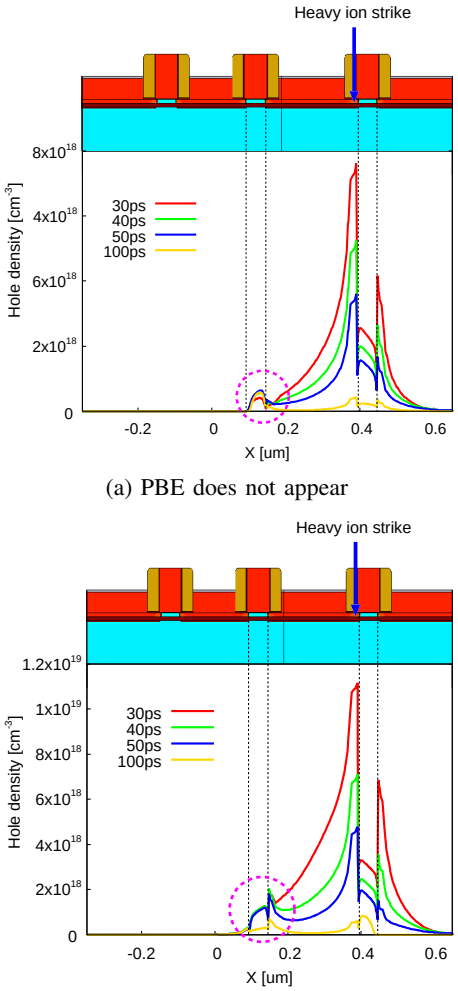
Heavy Ion	Cross Section [cm^2/ion]			
	T_S = 40 nm		T_S = 60 nm	
	DATA = 0	DATA = 1	DATA = 0	DATA = 1
Ar	0.00×10^{-10}	0.00×10^{-10}	0.00×10^{-10}	0.00×10^{-10}
Kr	0.96×10^{-10}	1.76×10^{-10}	1.76×10^{-10}	2.72×10^{-10}

The NMOS transistors covered by blue rectangles become sensitive at DATA = 1. By increasing silicon thickness of the raised layer, CS moves to right but the total area is almost same. Figure 7 shows the input and output voltage of the tristate inverter when a heavy ion strikes at the irradiation point 1 shown in Fig. 6 (b). The stored bit flips at T_S = 40 nm (a) but does not at T_S = 60 nm (b). In both cases, the input node goes down to the ground level. But the output node does not flip at T_S = 60 nm. It is because a heavy-ion strike brings PBE on both of the inverter and the tristate inverter.

PBE attenuates the pulse at the output node, which is called the pulse quenching effect [6]. Figure 8 shows temporal changes in hole density when heavy ions are irradiated to the two irradiation points shown in Fig. 6 (b) at T_S = 60 nm. Figure 8 (a) reveals holes are denser in the central channel region than in the adjacent drain and source regions. On the other hand, in (b), the hole density sharply decreases in the central channel region as compared with the adjacent drain and source region. PBE is generated when the hole density is greatly different between the drain and the channel region. It can be seen that when heavy ions are irradiated to the point 1, PBE also appears in the tristate inverters. Pulse quenching is stronger at the point 1 than at the point 2. Thus increase of generated charge does not always promote soft errors on NMOS.

Figure 9 and Table II show CS of PMOS transistors. Note that CS by Ar is 0. CS of PMOS transistor is much less than CS of NMOS mainly due to the difference of the mobility [7], [8]. Ar does not have enough LET to cause a bit flip in the latch. The total CS by Kr increases due to bit flips in the PMOS region. Table III shows the total CS from NMOS and PMOS. Except Ar irradiation at T_S = 40 nm, DATA = 1 is more vulnerable to soft errors than DATA = 0.

By changing the silicon thickness from 40 nm to 60 nm, the C_{gg}-V_{gs} and the I_{ds}-V_{gs} characteristics (static charac-



(a) PBE does not appear

(b) PBE appears

Fig. 8. Changes of hole density over time when heavy ions are irradiated to the two irradiation points at T_S = 60 nm. PBE does not appear (a) and appears (b).

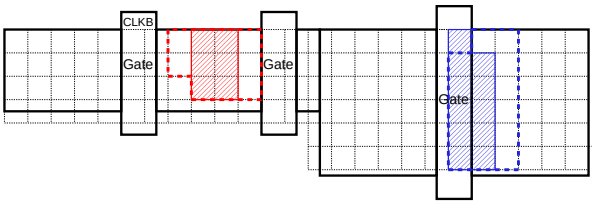
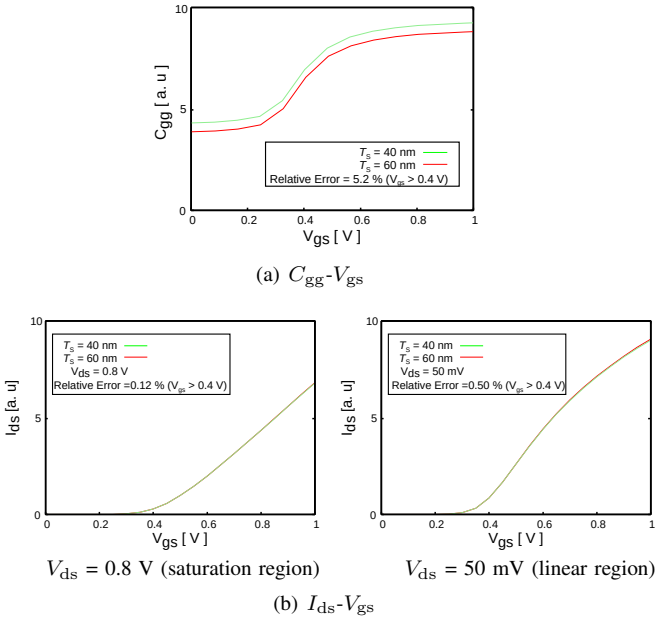


Fig. 9. Cross section by Kr from device simulation results in PMOS. CS by Ar is 0.

TABLE III

THE TOTAL VALUE OF CROSS SECTION OF NMOS AND PMOS FROM DEVICE SIMULATIONS.

Heavy Ion	Cross Section [cm^2/ion]			
	T_S = 40 nm		T_S = 60 nm	
	DATA = 0	DATA = 1	DATA = 0	DATA = 1
Ar	4.36×10^{-10}	4.36×10^{-10}	4.64×10^{-10}	5.12×10^{-10}
Kr	6.72×10^{-10}	7.36×10^{-10}	7.36×10^{-10}	9.28×10^{-10}



(a) C_{gg}-V_{gs}

V_{ds} = 0.8 V (saturation region) V_{ds} = 50 mV (linear region)

(b) I_{ds}-V_{gs}

Fig. 10. Dependence of silicon thickness to transistor characteristics

TABLE IV
CROSS SECTION FROM MEASUREMENT RESULTS.

Heavy Ion	Cross Section [cm^2/ion]	
	DATA = 0	DATA = 1
Ar	7.04×10^{-10}	7.51×10^{-10}
Kr	8.49×10^{-10}	1.28×10^{-9}

teristics) are changed as shown in Fig. 10. The C_{gg}-V_{gs} characteristic is changed by 5.2%. The I_{ds}-V_{gs} characteristic is changed by 0.12% at the saturation region and 0.5% at the linear region. CS when DATA = 1 by Kr increases by 26.1% at most. It can be seen that the impact of soft error tolerance is greater than the change in static characteristics.

IV. Experimental Results and Discussions

Heavy-ion irradiation was done at TIARA (Takasaki Ion Accelerators of Advanced Radiation Application, Japan). The standard latches were set to at (CLK, DATA) = (0, 0) or (1, 0) and supply voltage was fixed to 0.8 V. Ar and Kr ions were exposed to a fabricated chip in the 65 nm FDSOI from the normal angle. The experimental results are from [9]. Table IV show the experimental results. A comparison between simulation results (T_{S} = 60 nm) and actual measurement results is depicted in Fig. 11.

CS from the measurement is the sum of NMOS and PMOS CS. CS from the measurement and the simulation have the same tendency as clearly shown in Fig. 11. Regardless of the type of heavy ions, CS at (DATA, CLK) = (1, 0) is bigger than that at (0, 0). In the four conditions as shown in Fig. 11, CS from the device simulations are 65.9% to 86% of the experimental results. It can be concluded that in the experiments soft errors were also caused in the PMOS region by only Kr irradiation since the experimental and simulation results are highly correlated. Higher energy ions cause soft

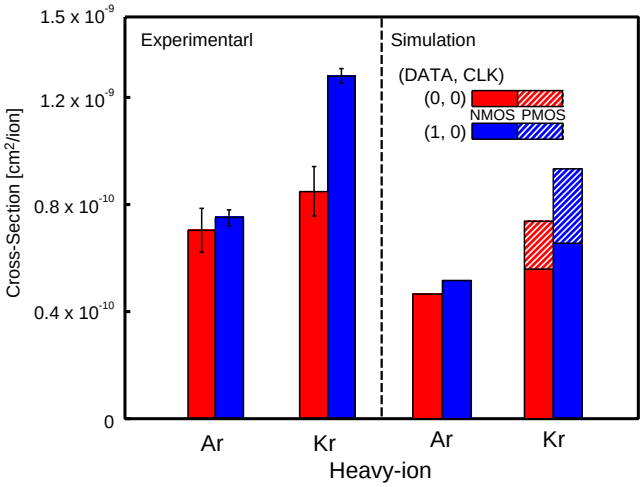


Fig. 11. Cross sections considering both of NMOS and PMOS contributions from simulations (T_{S} = 60 nm) and experiments.

errors in PMOS regions, which increases CS, while CS in NMOS regions is almost same due to the pulse quenching effect.

V. Conclusion

Silicon thickness is a key parameter to suppress soft errors in FDSOI. The thinner Silicon thickness is, the weaker soft error tolerance becomes. Adjusting thickness makes the simulation results closer to the measurement results. By increasing the silicon thickness from 40 nm to 60 nm, CS increase by 26.1% at most. On the other hand, static characteristics is changed by 5.2% at most. The impact of soft error tolerance is greater than the change in static characteristics. The silicon thickness of drain and source regions is a key parameter to fit the simulation results with the measurement results. From the simulation results an Ar hit on PMOS transistors does not cause a bit flip, while an Kr hit does. Considering contribution to soft-error CS from PMOS regions, the simulation results much closer to the measurement results. The pulse quenching effect suppresses a bit flip on NMOS regions by a heavy ion hit with higher LET. Soft errors from PMOS regions must be taken into account in the environments such as outer space.

ACKNOWLEDGMENT

This work was performed under the Shared Use Program of JAEA Facilities. This work is partly supported by JSPS KAKENHI Grant Number JP17K14667 and the Program on Open Innovation Platform with Enterprises, Research Institute and Academia (OPERA) from Japan Science and Technology Agency (JST). The VLSI chip in this study was fabricated under the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Renesas Electronics Corporation, Cadence Corporation, Synopsys Corporation, and Mentor Graphics Corporation.

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