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"Radiation Hardening by Design of Digital Circuits"

Single events by alpha particles and neutrons on the terrestrial region threaten safety, reliability and serviceability of semiconductor devices on which our daily life highly depends on. Radiation hardening by design must be taken into account for mission critical applications such as autonomous driving, aerospace and so on. This tutorial will provide an introduction of single events on digital circuits to cause a single event upset (SEU) on storage cells such as SRAMs, latches and flip-flops. Then several radiation-hardening-by-design (RHBD) techniques will be introduced to mitigate SEU including multimodular structures applicable to both of bulk and SOI and stacking structures effective to SOI.

Kazutoshi Kobayashi received his B.E., M.E. and Ph. D. in Electronic Engineering from Kyoto University, Japan in 1991, 1993, 1999, respectively. Starting as an Assistant Professor in 1993, he was promoted to associate professor in the Graduate School of Informatics, Kyoto University, and stayed in that position until 2009. For two years during this time, he acted as associate professor of VLSI Design and Education Center (VDEC) at the University of Tokyo. Since 2009, he has been a professor at Kyoto Institute of Technology. While in the past he focused on reconfigurable architectures utilizing device variations, his current research interest is in improving the reliability (Soft Errors, Bias Temperature Instability and Plasma Induced Damage) of current and future VLSIs. He started a research related to gate drivers for power transistors since 2013. He was the recipient of the IEICE best paper award in 2009 and the IRPS best poster award in 2013.