Impact of Combinational Logic Delay for Single Event Upset on Flip Flops in a 65 nm FDSOI Process

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***Abstract*— We measured single event upsets (SEUs) and single event transients (SETs) in a 65 nm FDSOI process by heavy-ion irradiation tests. SEU rates on a latch on a flip-flop depend on clock frequency and delay time of a combinational logic since SEU on slave latches cannot propagate through the combinational logic before clock signal turn to "1".**

SET cross section (CS) on an inverter is 1.14 x 10^{-11} cm^2/inv./ion which is 47x smaller than SEU CS in a standard FF. Maximum SET pulse width is 160 ps when Kr ions with linear energy transfer of 40 MeV-cm^2/mg were irradiated.

I. Introduction

Radiation-induced single event effects (SEEs) are significant issues for space application, aircraft and high performance computers. Occurrence probability of SEEs increases drastically in high performance computers since parallel arithmetic processors with low supply voltage are used for energy-efficient performance. However, radiation-hardened designs such as redundant structures have trade-off between radiation resilience and circuit delay.

SEEs are affected by circuit configuration and running application. Single event transients (SETs) are vanished by logical and timing-window masking effects during propagation through combinational logic circuits [1]. These effects also prevent single event upsets (SEUs) in flip-flops (FFs) from propagating to next FF. SEU rates on flip-flops can be reduced by large delay time of combinational stages since SEU may not propagate to next FF within a single clock cycle as shown in Fig. 1 [2]. SEU rates obtained from static condition tests are constantly overestimated.

We measured single event upsets (SEU) and single event transient (SET) in a 65 nm FDSOI process by heavy-ion irradiation tests. SEU rates were measured at clock frequencies of 500 kHz and 480 MHz to analyze the masking effect by delay time of combinational logic. SETs are measured by a time-to-digital converter to obtain SET pulse widths.

II. Measurement Circuits

A. Test Chip Overview

We fabricated two test chip in a 65 nm FDSOI process to measure SEU and SET rates as shown in Fig. 2. One has shift registers for SEU measurement while the other contains SET measurement circuits. The thicknesses of the buried oxide (BOX) layer and body layer are 15 nm and 12 nm, respectively. These two chips have the triple-well structure and well-contacts are inserted every 104 μm.

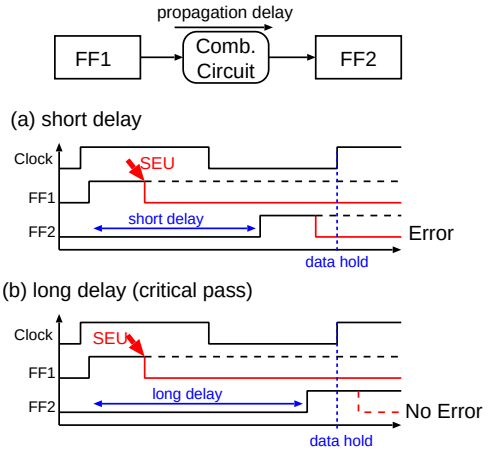

Fig. 1. Masking effect for SEU by the propagation delay of a combinational logics.

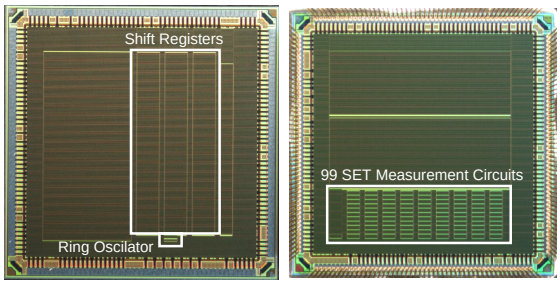

Fig. 2. Fabricated two test chips in a 65 nm FD-SOI process.

B. SEU Measurement Circuit

Figure 3 shows the implemented SEU measurement circuit. A ring oscillator is used for generating 480 MHz clock signal to measure SEU rates at dynamic condition. Multiplexers are inserted in the shift registers to keep stored values by switching shift registers from logical shift operation to circular shift operation [3]. 11-stage buffer chains are inserted as a combinational logic, which have 1.1 ns propagation delay time. In the shift register, a flipped value reaches next FF in 1.1 ns as shown in Fig. 5. SEU on the slave latch at CLK = 0 cannot reach next FF in the implemented shift register over the clock frequency of 480 MHz since it is less than 1.0 ns from the rising edge of the clock signal as shown in Fig. 5.

Three types of target FFs are implemented in the fabricated

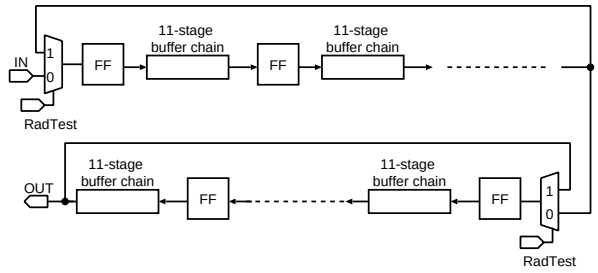

Fig. 3. Schematic diagrams of the SEU measurement circuit.

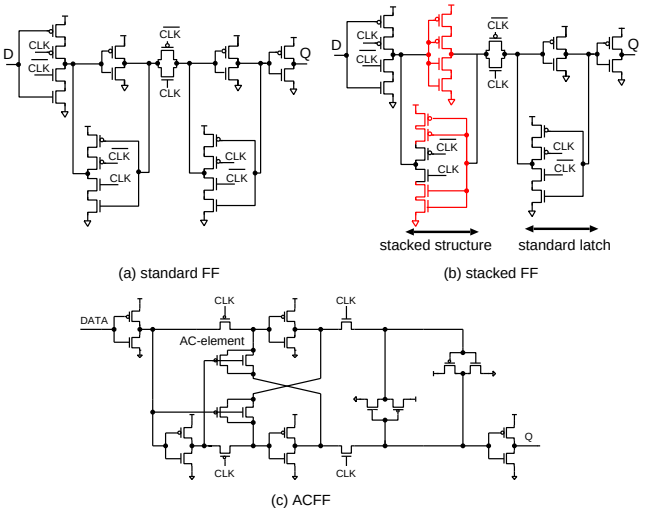

Fig. 4. Schematic diagrams of the implemented flip flops.

chip (Fig. 2 (a)): the standard FF, the stacked FF and ACFF (Adaptive Coupling FF) as shown in Fig. 4 (a) – (c), respectively [4], [5]. Stacked FF is based on the stacked inverter which consists of two series nMOS transistors and two series pMOS transistors. Neither parasitic bipolar action nor charge sharing happens simultaneously among these stacked transistors since FDSOI transistors are separated each other by the shallow trench isolator (STI) and the BOX layer. Therefore, the master latch in the stacked FF achieves higher soft error resilience in FDSOI. ACFF is a low-power FF which has no clock buffer for reversed clock signal. AC elements are inserted in the master latch to assist an input signal to overwrite a stored value in the master latch. The AC elements also reduce soft error rates since they attenuate SET in the master latch [6].

All implemented FFs have no SEU mitigation in the slave latches but the stacked FF and ACFF have SEU mitigation in the master latches. SEUs generated in the slave latch cannot propagated to next FF over 480 MHz clock frequency because combinational logic delay is larger than a half of clock period. We assume that the stacked FF and ACFF have smaller soft error rates than the standard FFs at 480 MHz.

C. SET Measurement Circuit

Figure 6 shows the measurement circuit for SET pulse widths. 16-parallel 50-stage inverter chains are implemented

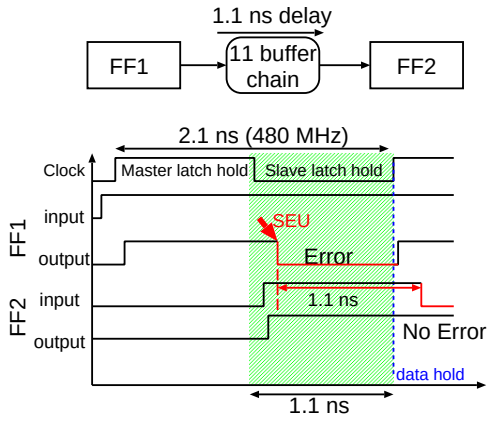

Fig. 5. Masking effect for SEU on slave latch by the propagation delay of the buffer chain.

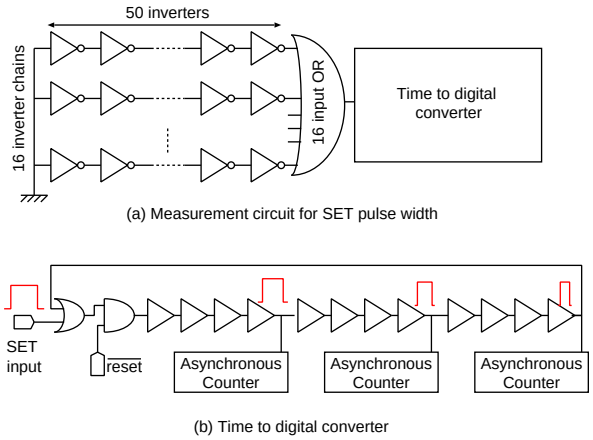

Fig. 6. Schematic diagrams of the SET measurement circuit.

as a target circuit connecting to a time-to-digital converter (TDC). Propagation-induced pulse shrinking (PiPS) effect is used to convert delay time to digital data by the TDC [7], [8], [9]. PiPS effect is caused by the difference between rise delay time D_r an fall delay time D_f in an unbalanced buffer. When D_r is larger than D_f, positive pulse width are linearly reduced by $D_r - D_f$ per buffer as shown in Fig. 7.

When a SET pulse is generated in the target circuit, it propagates through the inverter chain, the 16-input NOR logic cell and the buffer chain in the TDC. Then the SET pulse is shrunken during propagation through the buffer chain and finally vanished by the PiPS effect. SET pulse width can be obtained from the number of buffers through which the SET pulse propagates. Measurable maximum SET pulse width is equal to the total delay of the buffer chain. In this fabricated chip, measurable maximum SET pulse width is about 1.5 ns. Three asynchronous 10 bit counters measure the number of buffers through which the SET pulse propagates as shown in Fig. 6 (b). Note that transistor sizes of the inverter in Fig. 6 is 2x bigger than those of the buffer size in Fig. 3.

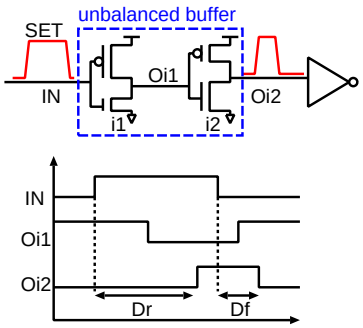

Fig. 7. Pulse shrinking mechanism by an unbalanced buffer.

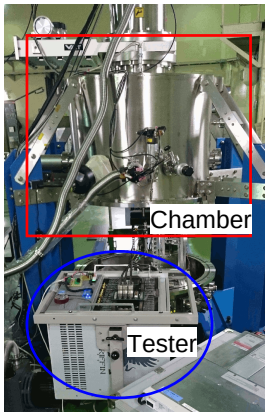

Fig. 8. Heavy ion irradiation test using vacuum chamber.

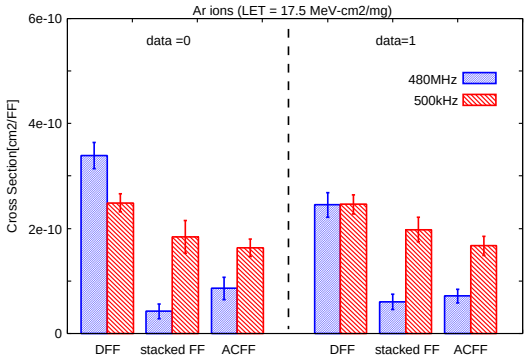

Fig. 9. Measurement results of Ar-ions-induced SEU cross sections at clock frequencies of 500 kHz and 480 MHz.

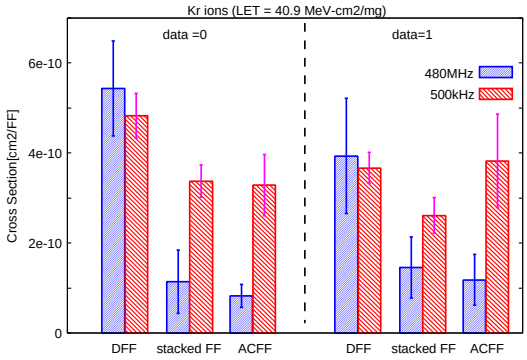

Fig. 10. Measurement results of Kr-ions-induced SEU cross sections at clock frequencies of 500 kHz and 480 MHz.

III. Heavy-ion Irradiation Tests

A. Test Setup

In order to investigate SEU and SET on a FDSOI process, neutron irradiation is not effective because of low error rates. Only a few SEUs were observed by one-day irradiation at RCNP (Research center for nuclear physics, Japan). Thus heavy-ion irradiation was performed at TIARA (Takasaki ion accelerators of advanced radiation application, Japan). The test chip was irradiated in a vacuum chamber shown in Fig. 8 to prevent decay of ion energy by the air. Irradiated ions are $^{40}Ar^{8+}$ and $^{84}Kr^{17+}$ whose linear energy transfer are 17.5 and 40 MeV-cm^2/mg, respectively.

During irradiation, 500 kHz or 480 MHz clock signals are applied to shift registers, which are generated by the external LSI tester or an implemented ring oscillator, respectively. All stored values in the three shift registers and the counters in the TDC are retrieved after irradiation.

B. SEU Measurement Results

Figures 9 and 10 show measurement results of SEU cross sections at clock frequencies of 500 kHz and 480 MHz. The number of observed SEUs and irradiated ion fluence are summarized in Table I. At 500 kHz, Kr-ions-induced SEU cross section in the DFF is 4 – 5 $\times 10^{-10}$ cm^2/FF, which is 8 – 10 times larger than that in a 28 nm FDSOI process [10]. One possible reason is that channel area in the 65 nm DFF is 5.4 times larger than that in the 28 nm DFF and body region depth also becomes thinner according to FDSOI process scaling down.

The SEU cross section of the standard FF does not depend on clock frequency. In contrast, SEU cross sections at 480 MHz of the stacked FF and ACFF are reduced to 25% – 55% of 500 kHz. It is because SEUs on slave latches of the stacked FF and ACFF become dominant. They cannot reach the SEU-hardened master latches by the propagation delay of 1.0 ns at 480 MHz.

We assume SEU in the stacked FF and AC FF at clock frequency of 480 MHz are induced by SET pulses. It is because SEU rates induced by SET pulses are increased according to increase of clock frequency. SET pulse width depends on the drive current of the logic gates through which a heavy ion passes. Therefore, SET pulses become wider in the slave latch composed of a small inverter and a tri-state inverter than those in logic gates. For better radiation hardness, SET-pulse mitigation on slave latches is more significant than SEU mitigation on slave latches.

C. SET Measurement Results

Figure 11 shows a pulse width distribution of Kr-ion-induced SET. Fluence and the number of SETs are also shown in Fig. 11. The counters in Fig. 6 is only active to SET pulses over 67 ps by circuit-level simulations. It means the SET measurement circuit cannot detect a SET

TABLE I

NUMBER OF SEUS AND IRRADIATED AR ION FLUENCE AT EACH CONDITION.

(a) Ar results

Clock Freq.	stored value	# of SEUs DFF	stacked FF	ACFF	Ar Fluence [ion/cm^2]
500kHz	ALL0	367	177	244	2.95×10^7
	ALL1	313	252	212	2.95×10^7
480MHz	ALL0	422	53	107	2.89×10^7
	ALL1	312	77	91	2.95×10^7

(b) Kr results

Clock Freq.	stored value	# of SEUs DFF	stacked FF	ACFF	Kr Fluence [ion/cm^2]
500kHz	ALL0	819	559	573	3.93×10^7
	ALL1	184	192	131	1.16×10^7
480MHz	ALL0	422	64	88	1.80×10^7
	ALL1	203	61	75	1.19×10^7

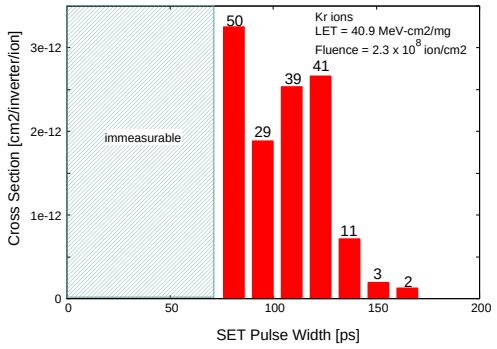

Fig. 11. Measurement result of SET pulse width distribution. The hatching region shows an immeasurable domain for implemented TDCs.

pulse less than 67 ps (the hatching region in Fig. 11). The maximum SET pulse width is 160 ps when Kr ions with linear energy transfer of 40 MeV-cm^2/mg were irradiated. Total SET cross section in a standard inverter is 1.14 x 10^{-11} cm^2/inverter/ion and it is 47x smaller than SEU cross section in the standard DFF. Compared with the SEU rates, SET rates on the inverter chain are negligibly small in the FDSOI process. SET pulse widths and SET rates can be increased by using multiple input NOR cells or logic cells with smaller transistor size which have smaller drive current. Therefore, soft errors induced by SET can not be ignored even in radiation hardened FFs.

IV. CONCLUSION

We measured single event upsets (SEUs) and single event transients (SETs) in a 65 nm FDSOI process by heavy-ion irradiation tests. SEU rates on the stacked FF and ACFF at 480 MHz are 2x – 4x smaller than those at 500 kHz. It is because SEU on the slave latch that holds a stored value when clock becomes 0 cannot propagate through the combinational logic connected to the slave latch. Radiation hardness of a slave latch is not mandatory when FFs connected to combinational logics with larger delay than a half clock cycle.

Distribution of SET pulses were also measured by the parallel inverter chains. SET cross section on an inverter is 1.14 x 10^{-11} cm^2/inv./ion. It is 47x smaller than SEU cross section in a standard FF. The maximum SET pulse width is 160 ps when Kr ions with linear energy transfer of 40 MeV-cm^2/mg were irradiated.

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