Sensitivity to Soft Errors of NMOS and PMOS Transistors Evaluated by Latches with Stacking Structures in a 65 nm FDSOI Process

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***Abstract*— Three different latch structures are fabricated in a 65 nm FDSOI process. We evaluate soft-error tolerance of latches by device simulations and α particle, neutron, heavy-ion irradiation tests in order to identify which transistor type is dominant to cause soft errors. The latch structure including an inverter with stacked NMOS and unstacked PMOS transistors has enough tolerance against soft errors by up to heavy ions with 40 MeV-cm^2/mg. It suggests that soft error rates are dominant on NMOS transistors not only in terrestrial regions but also in outer space.**

***Index Terms*— single event effect, soft error, α particle, neutron, heavy ion, FDSOI, stacked structure, PMOS, NMOS**

I. Introduction

Process scaling of technology results in high integration density and low power dissipation. Soft errors caused by radiation are one of the critical reliability issues. Redundant flip-flops and SRAM with error correct code (ECC)) have been employed for an effective method to suppress single event upset (SEU). However, they have larger area and power consumption overheads than conventional circuits. We need to minimize those overheads of radiation-hard circuits. We should identify which transistor type is weaker against SEU. It has been revealed that NMOS transistors are weaker against soft errors than PMOS transistors mainly due to the difference of the mobility [1][2]. While, recent investigations have demonstrated that the single event transient (SET) pulse widths for ion strikes on PMOS transistors (P-hits) is longer than those on NMOS transistors (N-hits) in a 65 nm bulk CMOS technology [3]. Fully depleted silicon on insulator (FDSOI) process has 50x - 110x higher tolerance for soft errors than bulk, because buried oxide (BOX) layers prevent charge from being collected from substrate [4]. Parasitic bipolar effect (PBE) is dominant to cause soft errors in FDSOI devices [4]. Generated carriers in body regions perturb the potential of body regions. Then, a parasitic bipolar transistor which is composed of the drain, body and source terminals turns on. Little is known about sensitive transistor of a latch in the FDSOI process. The purpose of this study is to compare the sensitivity to soft errors between N-hits and P-hits.

In this paper, we compare three different latch structures to identify a weak transistor type in a 65 nm FDSOI process. We evaluated the radiation hardness of these latches by TCAD simulations and α, neutron, heavy-ion irradiation tests.

II. SEU measurement Circuits

Figure 1 depicts three different latch schematics.

L0 : It is composed of two inverters and has no tolerance against soft errors.

L2 : It is composed of stacked inverters. They have two series-connected NMOS and PMOS transistors [5]. When a radiation particle hits on an NMOS or a PMOS transistor of the stacked inverter, its output node is not perturbed unless both of NMOS or PMOS transistors are influenced at the same time. Thus, the stacked inverter is strong against soft errors. We assume that soft errors rarely occur in this latch.

L1 : It is composed of stacked NMOS and unstacked PMOS transistors. This structure has high soft-error tolerance only when a radiation particle strikes on an NMOS transistor.

The measurement results of L0 show soft error rates (SER)

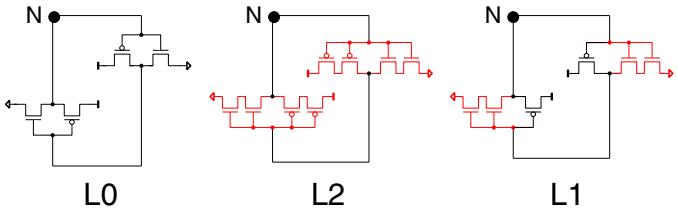


Fig. 1. Latch L0 is composed of two inverters. L1 is composed of stacked NMOS and unstacked PMOS transistors. L2 is composed of stacked inverters.

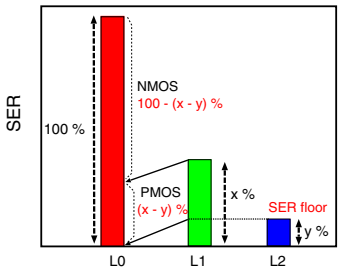
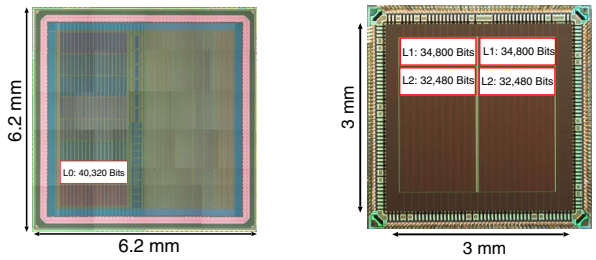


Fig. 2. Expected results that can compare radiation hardness of NMOS and PMOS transistors. We compare the results of L1 and L2 to remove SERs caused by stacked structures. It is possible to identify which of transistor types mainly cause soft errors by comparing the difference among the results of L1, L2 and L0. If $(x - y)\%$ is less than 50%, soft errors are dominant on NMOS transistors.



(a) [7] (b) [8]

Fig. 3. Fabricated chips in a 65 nm FDSOI process.

originated from NMOS and PMOS transistors. Those of L2 show the SER originated from NMOS transistors. Those of L1 show the SER originated from the stacked transistors. By comparing SERs of L0, L1 and L2, it is possible to investigate how PMOS transistors are contributed to soft errors as shown in Fig. 2.

We measured the SERs of L0, L1 and L2 using flip flops which contain these structures in the slave latches. Figures 3 (a) and (b) show the fabricated test chips in a 65 nm FDSOI process with thin BOX layers [6].

III. Simulation Results

Three-dimensional TCAD simulations are carried out using the Synopsys Sentaurus to evaluate radiation hardness of the latch constructed in the 65nm FDSOI process. We calculate soft-error tolerance of the latch consisting of cross-coupled inverters at supply voltage (V_{DD}) of 0.8 V. A heavy ion hits on an NMOS or a PMOS transistor as shown in Fig. 4.

We compared the threshold liner energy transfer (LET) value (the minimum LET at which the latch upsets). Higher threshold LET means higher radiation-hardness. Table I shows the threshold LET values. The threshold LET hitting on an NMOS transistor is 55% of that on a PMOS transistor. SET pulses originated from an NMOS transistor and a PMOS transistor in the latch were compared. Figure 5 shows SET pulses at V_{DD} = 0.8 V when an injected particle has

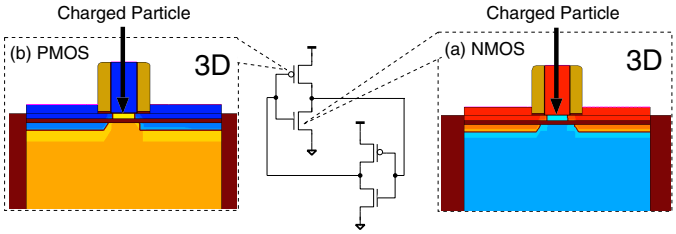


Fig. 4. Latch consisting of cross-coupled inverters on device simulations.

TABLE I
THRESHOLD LET VALUES OF LATCH.

Transistor	Threshold LET value (MeV-$\mathbf{cm^2}$/mg)
(a) NMOS	3.8
(b) PMOS	6.9

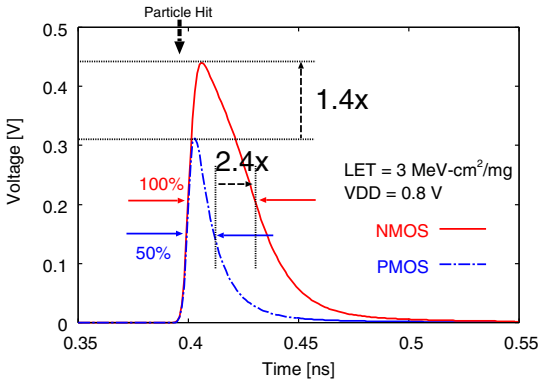


Fig. 5. SET pulses originated from particle hits on an NMOS transistor and a PMOS transistor in latch when the injected particle has LET of 3 MeV-$\mathbf{cm^2}$/mg at V_{DD} = 0.8 V. We compared values of heights at peaks and widths at 50% height.

LET of 3 MeV-$\mathbf{cm^2}$/mg. The SET pulse generated from an NMOS transistor is 1.4x higher and 2.4x wider than those from a PMOS transistor despite a particle with same LET. This simulation results reveal that NMOS transistors produce bigger SET pulses than PMOS transistors.

IV. Experimental Results

We measured the radiation hardness of three latches when the node N is 0 or 1 in Fig. 1.

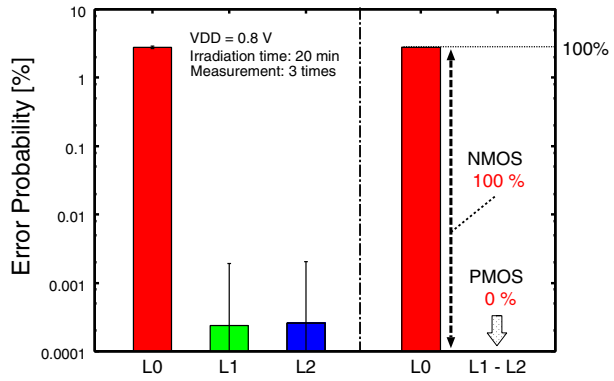
A. α Particle Irradiation

α particle irradiation tests were carried out using a 3 MBq $^{241}\mathrm{Am}$ source. All measurements were done by repeatedly initializing all latches: the α source was placed on the chip for 20 minutes and data were read after removing the α source. This tests were carried out three times under respective conditions and the obtained data were averaged. The error probability (EP) is used to evaluate soft-error tolerance. EP was calculated using Eq. 1. The error bars are within 95.44% confidence (2σ).

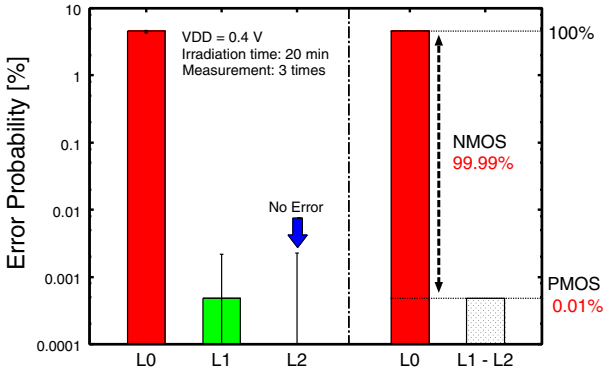
$$EP = \frac{N_{\mathrm{error}}}{N_{\mathrm{FF}}} \tag{1}$$

The EP was the number of errors (N_{error}) divided by the number of FFs (N_{FF}).

Table II summarizes the average number of errors by α particles under each static condition. Figure 6 shows experimental results of α-induced error probabilities (EPs) at V_{DD} = 0.8 V and 0.4 V. No distinct difference is observed in the EPs of L1 and L2 when V_{DD} = 0.8 V. The results clearly show that soft errors in L0 are originated from NMOS transistors with 100% probability when V_{DD} = 0.8 V. The ratio of soft errors at an NMOS transistor to the total soft errors in L0 is 99.99% by α particles even at V_{DD} = 0.4 V. Thus, soft errors by α particle irradiation are dominant on NMOS transistors.

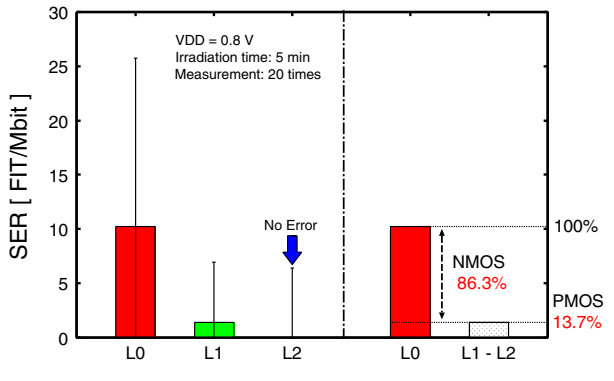


(a) V_{DD} = 0.8 V

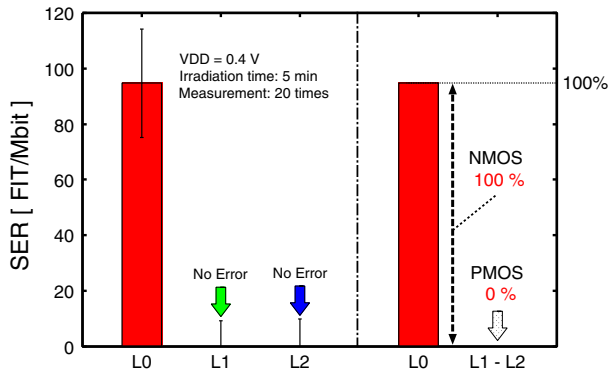


(b) V_{DD} = 0.4 V

Fig. 6. Experimental results of α-induced error probabilities. Error bars are within 95.44% confidence. Down arrows mean no error.



(a) V_{DD} = 0.8 V



(b) V_{DD} = 0.4 V

Fig. 7. Experimental results of neutron-induced soft error rates. Error bars are within 95.44% confidence. Down arrows means no error.

B. Spallation Neutron Irradiation

The spallation neutron experiments were carried out at the research center for nuclear physics (RCNP), Osaka University, Japan [9]. The average acceleration factor (AF) is about 4.3×10^8 compared with the sea level in New York city. To increase the number of upset FFs within a limited time, stacked device under test (DUT) boards were used. Four chips are mounted on a DUT board. We measured soft error rates (SERs) under two conditions used in the α particle irradiation tests. The SER was calculated using Eq. 2. Tests were repeated in 20 times under each condition and the obtained data are averaged at V_{DD} = 0.8 V. Irradiation tests when V_{DD} = 0.4 V were repeated for ten times at the node N = 1 in Fig. 1. The error bars are within 95.44% confidence (2σ).

$$SER\ [\mathrm{FIT/Mbit}] = \frac{N_{\mathrm{error}} \times 10^9 \times 1024^2}{5/60 \times AF \times N_{\mathrm{FF}}} \qquad (2)$$

Table III summarizes the average number of errors by neutrons and AF under each static condition. Figure 7 shows neutron-induced SERs. The experimental results of L0 are quoted from [7]. The ratio of the SERs at an NMOS transistor to the total soft errors in L0 is caused 86.3% by neutron irradiation when V_{DD} = 0.8 V. No distinct difference is observed in the SERs of L1 and L2 when V_{DD} = 0.4 V. Soft errors in L0 are originated from NMOS transistors with 100% probability by neutron irradiation when V_{DD} = 0.4 V.

α particles which pass in SOI layers directly deposit charge. While only secondary ions by nuclear reactions between neutrons and silicon atoms deposit charge. Thus, the number of errors by α particles is much larger than that by neutrons.

C. Heavy-Ion Irradiation

Heavy-ion irradiation test was carried out at the takasaki ion accelerators for advanced radiation application (TIARA),

TABLE II

THE NUMBER OF ERRORS BY α PARTICLES ON AVERAGE UNDER EACH STATIC CONDITION WHEN V_{DD} = 0.8 V AND 0.4 V.

	# of errors		
VDD	L0	L1	L2
0.8 V	1.12×10^3	1.67×10^{-1}	1.67×10^{-1}
0.4 V	1.82×10^3	3.33×10^{-1}	0.00

TABLE III

THE NUMBER OF ERRORS BY NEUTRONS ON AVERAGE UNDER EACH STATIC CONDITION WHEN V_{DD} = 0.8 V AND 0.4 V.

	# of errors			$AF \times 10^8$		
VDD	L0	L1	L2	L0	L1	L2
0.8 V	0.20	0.05	0.00	3.81	4.30	
0.4 V	1.85	0.00	0.00	3.81	3.95	

TABLE IV

ENERGY AND LET OF HEAVY IONS.

	Energy [MeV]	LET [MeV-cm^2/mg]	Range [μm]
Ne	54.0	7.60	25.7
Ar	107	17.5	24.7
Kr	230	40.9	27.7

TABLE V

THE NUMBER OF ERRORS BY NEUTRONS ON AVERAGE UNDER EACH STATIC CONDITION WHEN $V_{\rm DD}$ = 0.8 V AND $N_{\rm ion}$.

	# of errors			$N_{\rm ion} \times 10^6$ [/cm^2]		
ion	L0	L1	L2	L0	L1	L2
Ne	43.1	0.00	0.00	3.41	4.07	
Ar	47.5	6.30	3.70	2.18	2.59	
Kr	91.6	30.6	13.3	2.53	2.42	

Japan. Figure 8 shows a vacuum chamber and an engineering tester. The radiation hardness was investigated by three ions as described in Table IV.

We measured the number of upsets caused by heavy ions when $V_{\rm DD}$ = 0.8 V. Heavy ions were exposed with the static conditions for 30 seconds. Ion exposures are done under the static conditions. Measurements were five times per condition by Ne, Ar and Kr. The cross section (CS) is used in order to evaluate soft-error tolerances. Eq. 3 is used in order to calculate the CS [10].

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\rm error}}{N_{\rm ion} \times N_{\rm FF}} \tag{3}$$

The CS is calculated from the number of errors ($N_{\rm error}$), the number of ions per unit area ($N_{\rm ion}$), and the number of FFs ($N_{\rm FF}$).

Table V summarizes the average number of errors by heavy ions and $N_{\rm ion}$ under each static condition. Figure 9

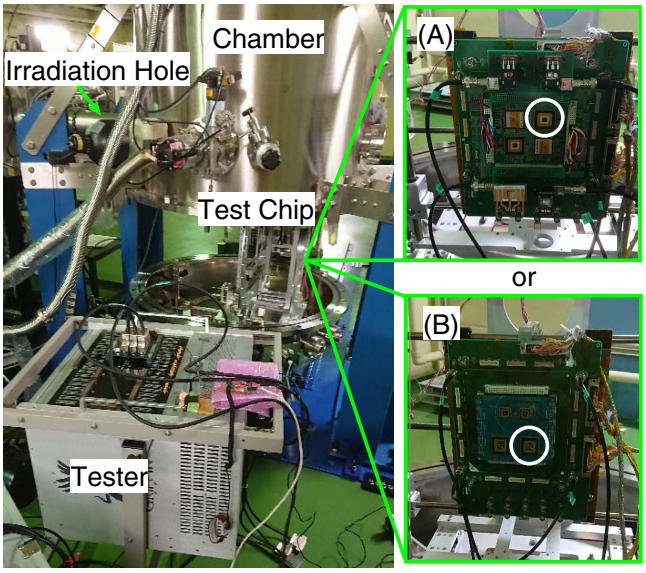
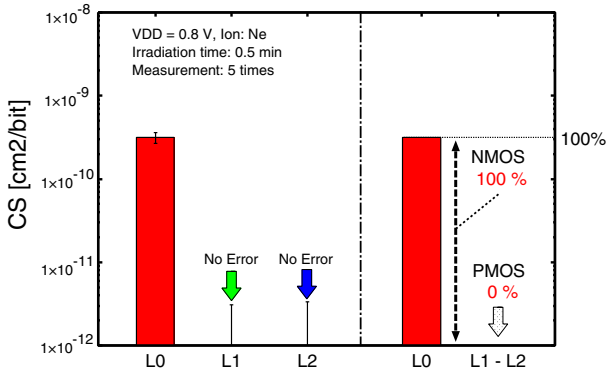
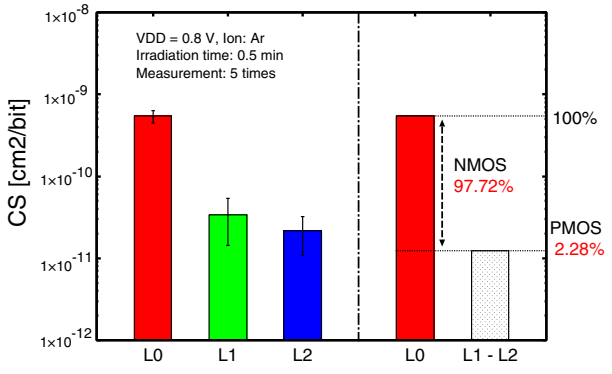


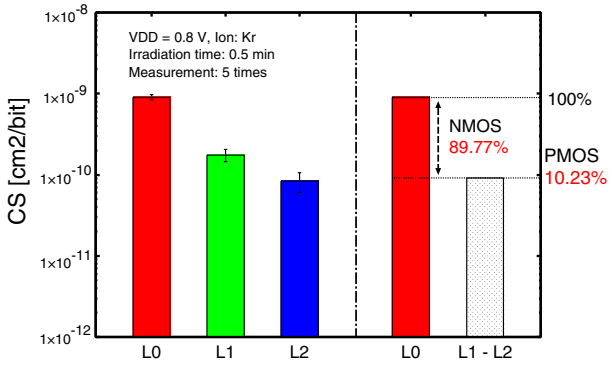
Fig. 8. A vacuum chamber and an engineering tester. (A) is the test chip (a) which contains L0 in Fig. 3. (B) is the test chip (b) which contains L1 and L2 in Fig. 3.



(a) Ne



(b) Ar



(c) Kr

Fig. 9. Experimental results of heavy-ion cross sections. Error bars are within 95.44% confidence. Down arrows means no error in (a).

shows heavy-ion-induced CSs. No distinct difference is observed in the CSs of L1 and L2 by Ne. Soft errors in L0 are originated from NMOS transistors with 100% probability by Ne. The CS at an NMOS transistor by Ar accounts for 97.72% of the total CS in L0. These results show that soft errors from PMOS transistors start to cause by heavy ions whose LET is between 7.6 MeV-$\mathbf{cm^2}$/mg and 17.5 MeV-$\mathbf{cm^2}$/mg. The ratio of the CS at an NMOS transistor to the total CS in L0 is 89.77% by Kr. The higher the energy of heavy ion is, the bigger the CS of an PMOS transistor is. The number of particles with over 40 MeV-$\mathbf{cm^2}$/mg is much less than those with less than 40 MeV-$\mathbf{cm^2}$/mg in outer space [11]. Thus, soft errors originated from an NMOS

transistor account for more than 89% of the total soft errors on FDSOI processes in outer space.

V. Conclusion

We compared the radiation hardness of three latches to identify a weak transistor type in a 65 nm FDSOI process. According to the TCAD simulations and experimental results, the ratio of soft errors at NMOS transistors to the total soft errors in the conventional unstacked latch is more than 86.3% by $\boldsymbol{\alpha}$ particles and neutrons and heavy ions. It is possible to reduce more than 86.3% soft error rate not only in terrestrial regions but also in outer space by suppressing soft errors only from NMOS transistors instead of radiation-hardened techniques on both PMOS and NMOS transistors with large overheads in 65 nm FDSOI processes. While, soft errors from PMOS transistors start to cause by heavy ions whose LET is between 7.6 MeV-$\mathbf{cm^2}$/mg and 17.5 MeV-$\mathbf{cm^2}$/mg. The number of secondary ions with over 18MeV-$\mathbf{cm^2}$/mg by neutron in Si is much less than those with less than 18MeV-$\mathbf{cm^2}$/mg [12]. We must suppress soft errors from NMOS and PMOS transistors if we need reliable semiconductor chips completely without causing SEU in terrestrial regions and outer space.

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