Influence of Layout Structures to Soft Errors Caused by Higher-energy Particles on 28/65 nm FDSOI Flip-Flops

Masashi Hifumi, Haruki Maruoka, Shigehiro Umehara, Kodai Yamada, Jun Furuta and Kazutoshi Kobayashi
Kyoto Insititute of Technology
Graduate School of Science & Technology, Kyoto Insititute of Technology
Kyoto, Japan
phone: (+81)-080-1465-0030, e-mail: mhifumi@vlsi.es.kit.ac.jp

***Abstract*— The effects from layout structures of flip-flops for soft errors are investigated. Three flip-flops with different layouts but identical layout areas are fabricated in 28/65 nm FDSOI. Heavy ion irradiation by 40 MeV-cm^2/mg reveals that the layout with separated diffusions in 28 nm have 2x cross section than that with shared diffusion. Flip-flops in 65 nm have almost equivalent cross sections at any energy. It is due to fluctuations of soft-error tolerance caused by layout structures of the highly-scaled 28 nm.**

***Index Terms*— Soft error, Heavy ion, FDSOI, Charge sharing, stress**

I. Introduction

As semiconductor devices continue scaling, reliability issues of semiconductor chips are becoming dominant[1]. Soft error are caused by radiation particles. Highly-reliable systems for automotive, aerospace and medical use must mitigate soft errors[2], [3]. Heavy ions are one of main sources of soft errors in the outer space in which the energy spectrum are distributed as shown in Fig. 1. Semiconductor chips in the outer space must be tolerant below the heavy ions with the LET of 40 MeV-cm^2/mg. Typically, process scaling worsens SERs (soft error rates) per chip[3]. But SERs per logic gate is becoming small especially in SOI since the sensitive volume is scaled[4].

Layout strctures influences SERs, however there are lots of unknown effects on nanometer devices. Pulse quenching effects decrease single event transient pulse width causing soft errors[5]. If the distance of adjacent transistors is close, charge sharing decreases the pulse widths on the bulk process[6]. Layout structures give some amount of stress to transistors. Local stress effects caused by Shallow Trench Isolation (STI) enhance or degrade performance of transistors[7], [8]. Stress effects on entire chips improve the soft-error tolerance of SRAM on 40 nm bulk[9]. However, local stress effects on the soft-error tolerance has not been investigated.

In this paper, we evaluate soft-error tolerance of Flip-flops (FFs) fabricated in 28 nm and 65 nm FDSOI technologies. Test chips includes three FFs with different layout structures but identical layout areas to investigate how stress or pulse quenching affects soft error hardness. Their radiation hardnesses were investigated by heavy ion irradiation. Section II shows the layout structures of FFs and test chips. Section III shows experimental method and how to evaluate soft-error tolerances. Section IV shows experimental results and disscutions. Section V concludes this paper.

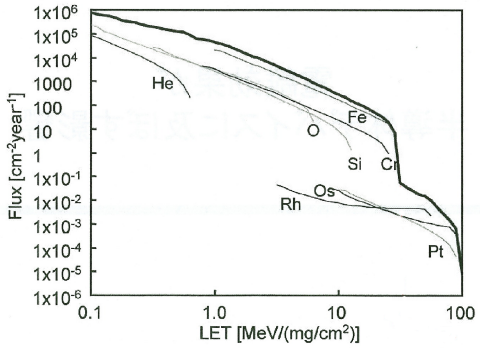


Fig. 1. Spectrums of heavy ions at the galactic system[10].

II. Design

In Fig. 2, the structure of a FDSOI (Fully Depleted Silicon On Insulator) CMOS process. It has higher tolerance for soft errors than bulk. BOX layers under transistors eliminate charge by a particle hit from collecting to drain. Two chips were fabricated by the 28 nm and 65 nm thin-BOX FDSOI processes called SOTB (Silicon on Thin-BOX) and UTBB (Ultra Thin Body and BOX) respectively[11], [12]. In Table I, parameters of 28 nm UTBB and 65 nm SOTB. They can control body biases through 25 nm and 10 nm thin BOX layers. Three different layout structures of delayed flip-flops (DFFs) are implemented on the fabricated chips.

A. Layout Structures of Flip-Flops

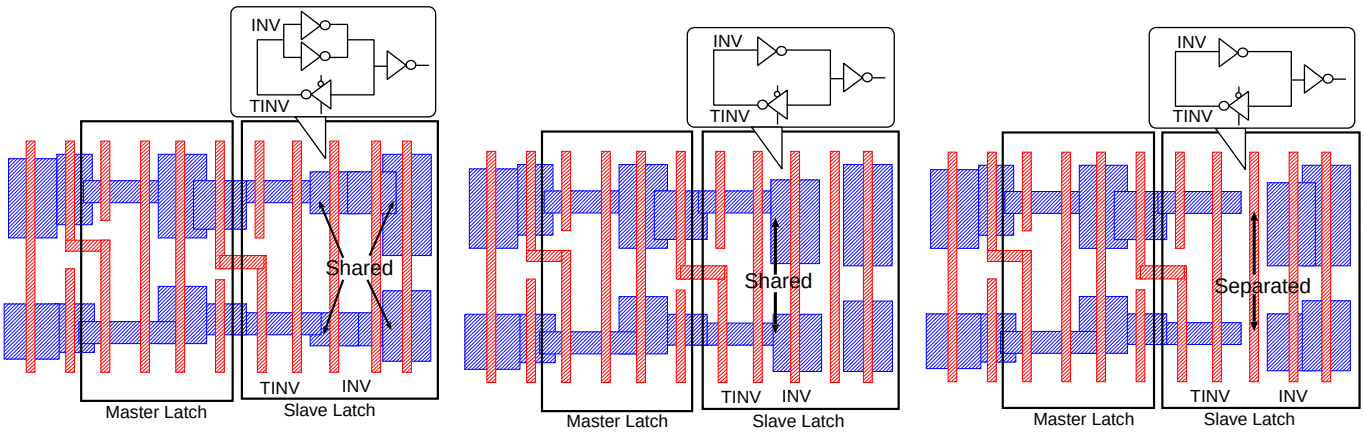
In Figs. 3 and 4, the layout structures and schematics.

- L0 Diffusions in SL (Slave Latches) and the output inverter are shared (Fig. 3 (a)).
- L1 Diffusions in SL are shared (Fig. 3 (b)).
- L2 Diffusions in SL are separated (Fig. 3 (c)).

The layout structures of slave latches as follows are differentiated. Circuit areas and transistor sizes are all equivalent. On L0, The inverter in SL divided into two parallel inverters with the half transistor width in order to remove STI among the latch and the output inverter.

B. Test Chips

Test chips fabricated in 65 nm bulk/SOTB and 28 nm UTBB are shown in Fig. 5. The test chip on the 65 nm bulk process is fabricated compare the soft-error tolerance with the 65 nm SOTB. Several types of DFFs with different layout structures L0, L1, and L3 are embedded in two test chips as shown in Fig. 6. All DFFs are connected as a shift register.



(a) L0 :Diffusions in SL and output inverter are shared.

(b) L1 : Diffusions in SL are shared.

(c) L2 : Diffusions in SL are separated.

Fig. 3. Three difference layouts of DFFs. All layouts have same circuit area.

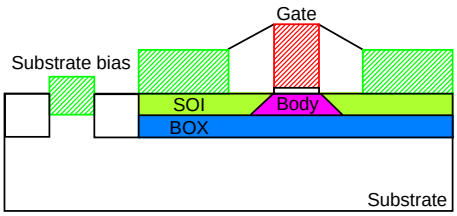


Fig. 2. A FDSOI CMOS process.

TABLE I
PARAMETERS OF FDSOI.

	Gate length [nm]	Body thickness [nm]	BOX thickness [nm]
SOTB	65	12	10
UTBB	28	7	25

III. HEAVY IONS IRRADIATION TEST

Heavy ion irradiation was carried out at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA). Fig. 7 shows a vacuum chamber and an engineering tester. The radiation hardness were investigated by three ions as described in Table II.

We measured the number of upsets caused by heavy ions as below.

1) Initialize serially-connected FFs.
2) Heavy ions are exposed with the static conditions without applying clock signals.
3) Read out all FFs to count the number of upsets.

Ion exposures are done by the static conditions of (DATA, CLK) = (1, 0), (0, 0). Slave latches repeated for hold the state when CLK = 0. Measurements were five times per one of the conditions by Ar and Kr. By Ne but, they are carried out three times. The cross section (CS) is used in order to evaluate soft-error tolerances. Eq. 1 is used in order to calculate the CS[13].

$$CS\ [\mathrm{cm}^2/\mathrm{bit}] = \frac{N_{\mathrm{error}}}{N_{\mathrm{ion}} \times N_{\mathrm{FF}}} \quad (1)$$

The CS is calculated from the number of errors (N_{error}), the number of ions per unit area (N_{ion}), and the number of FFs (N_{FF}).

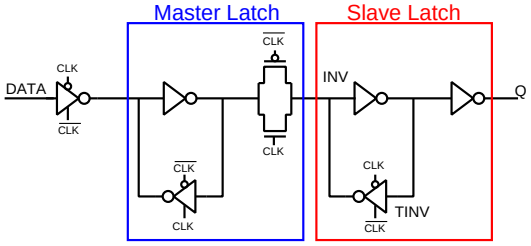
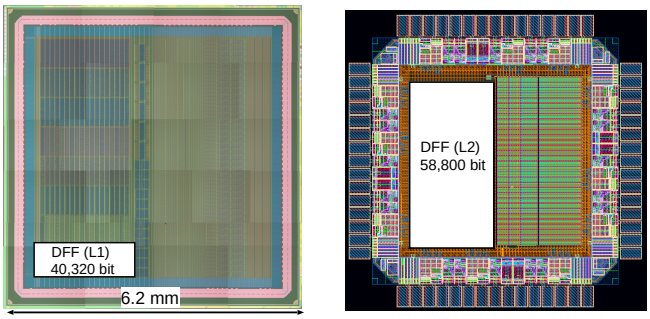


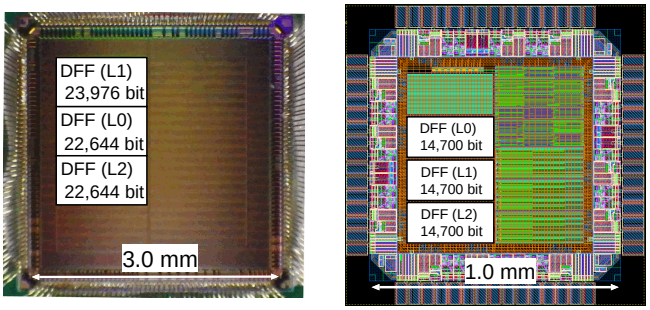
Fig. 4. Conventional Flip-Flop (DFF).



(a) 65 nm bulk/SOTB

(b) 28 nm UTBB

Fig. 5. Test chips to compare three processes.



(a) 65 nm SOTB

(b) 28 nm UTBB

Fig. 6. Test chips to investigate layout structure effects.

IV. EXPERIMENTAL RESULTS

CS of FFs by heavy-ion irradiation on 65 nm bulk, SOTB, and 28 nm UTBB are shown in Table III and Fig 8. The

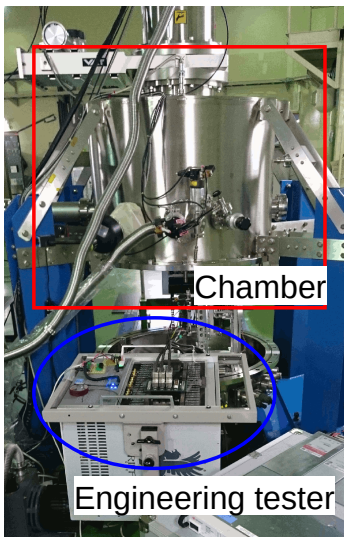


Fig. 7. A vacuum chamber and an engineering tester.

TABLE II
ENERGY AND LET OF HEAVY IONS.

	Energy [MeV]	LET [MeV-cm^2/mg]	Range [μm]
Ne	75	6.5	38.9
Ar	150	15.8	36.1
Kr	322	40.3	37.3

average of all static conditions were calculated. The CS of 65 nm SOTB at 1.0V by Kr is 1/50 of 65 nm bulk and 18x higher than 28 nm UTBB at 1.0 V.

In Figs. 9 and 10 , the CS of the three different layouts in 65 nm and 28 nm. The average of the CS were calculated at two conditions of (DATA, CLK) = (0, 0), (1, 0). On 65 nm SOTB, no distinct difference is observed. But on 28 nm, at Kr with the LET of 40.3 MeV-cm^2/mg, the CS of L2 is 2x higher than others.

V. DISCUSSIONS

According to the experimental results, we have these two assumptions to differentiate the tendency of the CS between 28 and 65 nm.

Charge Sharing and Pulse Quenching: Single Event Transient (SET) pulses are degraded by charge sharing in L0 and L1. In Table IV, distances between inverters (INVs) and tristate inverters (TINVs) denoted by D_{g} as described in Fig. 11. This figure also shows pulse quenching effects by charge sharing. These effects do not happen in 65 nm because D_{g} is larger than the charge sharing region. In 28 nm, charge sharing effects attenuate the pulse width in TINVs of L0 and L1 because D_{g} is short or the pulse quenching effects are enhanced by irradiation of higher-LET heavy ions[5]. On the other hand, the CS of L2 is 2x higher than those of L0 and L1 in 28 nm because D_{g} of L2 is longest and STI intercepts

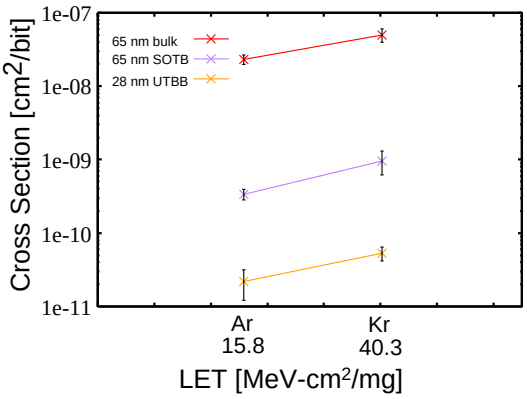


Fig. 8. Heavy ion cross sections of FFs at 1.0V.

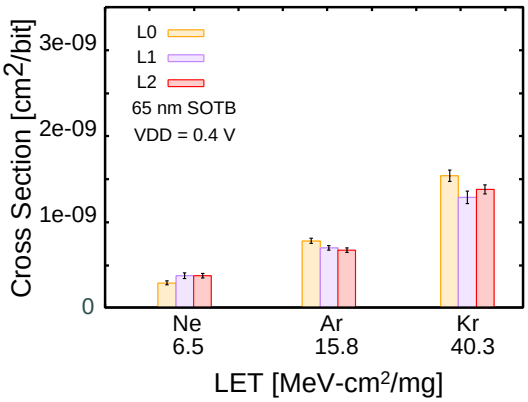


Fig. 9. Heavy ion cross sections of FFs on 65nm SOTB at 0.4V.

charge sharing.

Stress Effects: The tolerance against soft errors is fluctuated by stress effects. In order to alleviate mobility degradations from STI pressures, the wafer notch of 65 nm processes is set to <100> orientation[14]. We assume that the wafer notch of 28 nm is also <100>. However, stress effects in 28 nm are stronger than 65 nm. The compression stress enhances the hole mobility which promotes charge collection. Due to longer compression strain in 28 nm, collected charge in 28 nm is higher rate of increase than that in 65 nm.

VI. CONCLUSION

We fabricated test chips in 28/65 nm thin-BOX FDSOI technologies including three types of flip-flops with different layout structures. Heavy-ion irradiation shows that the cross sections of 28 nm UTBB at 1.0V by Kr is 1/18 of 65 nm SOTB. No distinct differences by the energy of heavy ions were observed in 65 nm. But in 28 nm, Kr with the LET of 40.3 MeV-cm^2/mg doubles the cross section of the layout

TABLE III
HEAVY ION CROSS SECTION OF FFS AT 1.0V.

Heavy ions	Cross Section [$\times 10^{-9}$ cm^2/bit]		
	28 nm UTBB	65 nm SOTB	65 nm bulk
Kr	5.29×10^{-2}	9.65×10^{-1}	5.02×10
Ar	2.18×10^{-2}	3.38×10^{-1}	2.32×10

TABLE IV
DISTANCE BETWEEN INV AND TINV (D_{g}).

	D_{g} [nm]		
Process	L0	L1	L2
28 nm UTBB	133	133	274
65 nm SOTB	390	300	780

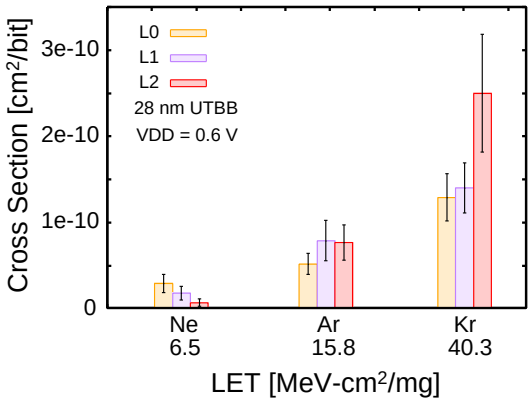


Fig. 10. Heavy ion cross sections of FFs on 28nm UTBB. Cross section of L2 is 2× than others at Kr, 0.6V condition.

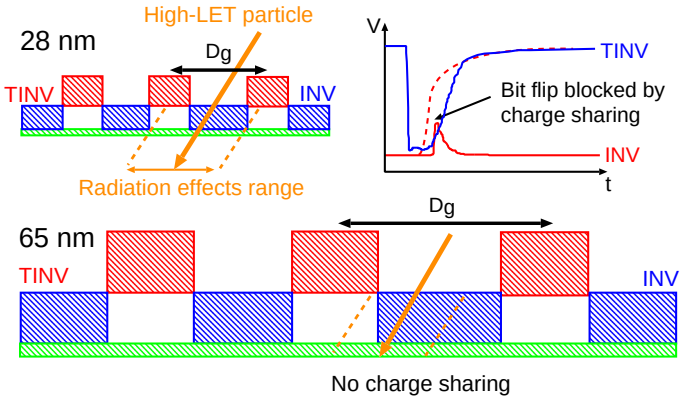


Fig. 11. Pulse quenching effects in latch. Charge sharing eliminate soft errors.

with separated diffusions in the slave latch compared to those of shared diffusions. It is because the distance of the inverters and the tristate inverter in the latch is longer and STI intercepts charge sharing in the latch with separated diffusions. For the outer space applications such as satellites, it is better to sharing diffusions of the inverter and the tristate inverter in latches to enhanced soft-error tolerance.

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References

[1] N. Seifert, V. Ambrose, B. Gill, Q. Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, and A. Balasubramanian. On the radiation-induced soft error performance of hardened sequential elements in advanced bulk cmos technologies. In *Proc. Int. Rel. Phys. Symp.*, pages 188–197, May 2010.

[2] S. Buchner, M. Baze, D. Brown, D. McMorrow, and J. Melinger. Comparison of error rates in combinational and sequential logic. *IEEE Transactions on Nuclear Science*, 44(6):2209–2216, Dec 1997.

[3] H. Liu, M. Cotter, S. Datta, and V. Narayanan. Technology assessment of si and iii-v finfets and iii-v tunnel fets from soft error rate perspective. In *IEDM*, pages 25.5.1–25.5.4, Dec 2012.

[4] K. Zhang, S. Kanda, J. Yamaguchi, J. Furuta, and K. Kobayashi. Analysis of the soft error rates on 65-nm sotb and 28-nm utbb fd-soi structures by a phits-tcad based simulation tool. In *2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pages 1–4, Sept 2015.

[5] L. Sheng, H. Wei, Z. Zhun, H. Lingxian, C. Jianmin, and W. Qingyang. Investigation of double peak voltage in pulse quenching effect on the single-event transient. In *2016 IEEE International Nanoelectronics Conference (INEC)*, pages 1–2, May 2016.

[6] J. R. Ahlbin, M. J. Gadlage, D. R. Ball, A. W. Witulski, B. L. Bhuva, R. A. Reed, G. Vizkelethy, and L. W. Massengill. The effect of layout topology on single-event transient pulse quenching in a 65 nm bulk cmos process. *IEEE Transactions on Nuclear Science*, 57(6):3380–3385, Dec 2010.

[7] R. Radojcic. Design-for-stress for cmos technologies - the next frontier. In *2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC)*, pages 98–98, May 2016.

[8] C. C. Tan and P. B. Y. Tan. Shallow trench isolation stress effect on cmos transistors with different channel orientations. In *2016 IEEE International Conference on Semiconductor Electronics (ICSE)*, pages 228–231, Aug 2016.

[9] N. N. Mahatme, B. L. Bhuva, Y. P. Fang, and A. S. Oates. Impact of strained-si pmos transistors on sram soft error rates. In *2011 12th European Conference on Radiation and Its Effects on Components and Systems*, pages 202–206, Sept 2011.

[10] Y. Takahashi. "Space Radiation Effects on Semiconductor Devices (Reliability Engineering in Astronautics)" in Japanese. *REAJ:Reliability*, 36 (8):460–467, 2012.

[11] G. Gasiot, D. Soussan, M. Glorieux, C. Bottoni, and P. Roche. Ser/sel performances of srams in utbb fdsoi28 and comparisons with pdsoi and bulk counterparts. In *Reliability Physics Symposium, 2014 IEEE International*, pages SE.6.1–SE.6.5, June 2014.

[12] Y. Morita, R. Tsuchiya, T. Ishigaki, N. Sugii, T. Iwamatsu, T. Ipposhi, H. Oda, Y. Inoue, K. Torii, and S. Kimura. Smallest vth variability achieved by intrinsic silicon on thin box (sotb) cmos with single metal gate. In *VLSI Tech. Symp.*, pages 166–167, June 2008.

[13] J. S. Kauppila, T. D. Loveless, R. C. Quinn, J. A. Maharrey, M. L. Alles, M. W. McCurdy, R. A. Reed, B. L. Bhuva, L. W. Massengill, and K. Lilja. Utilizing device stacking for area efficient hardened soi flip-flop designs. In *2014 IEEE International Reliability Physics Symposium*, pages SE.4.1–SE.4.7, June 2014.

[14] T. Iwamatsu, T. Terada, K. Ishikawa, H. Oda, and Y. Inoue. Electrical characteristics and crystal quality analysis of thin-body channel silicon-on-insulator metal-oxide-semiconductor field-effect transistors using two-step elevated silicon epitaxial process. *Japanese Journal of Applied Physics*, 48(4S):04C045, 2009.