Influence of Layout Structures to Soft Errors Caused by Higher-energy Particles on 28/65 nm FDSOI Flip-Flops

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Abstract—The effects from layout structures of flip-flops for soft errors are investigated. Three flip-flops with different layouts but identical layout areas are fabricated in 28/65 nm FDSOI. Heavy ion irradiation by 40 MeV-cm$^2$/mg reveals that the layout with separated diffusions in 28 nm have 2x cross section than that with shared diffusion. Flip-flops in 65 nm have almost equivalent cross sections at any energy. It is due to fluctuations of soft-error tolerance caused by layout structures of the highly-scaled 28 nm.

Index Terms—Soft error, Heavy ion, FDSOI, Charge sharing, stress

I. INTRODUCTION

As semiconductor devices continue scaling, reliability issues of semiconductor chips are becoming dominant[1]. Soft error are caused by radiation particles. Highly-reliable systems for automotive, aerospace and medical use must mitigate soft errors[2], [3]. Heavy ions are one of main sources of soft errors in the outer space in which the energy spectrum are distributed as shown in Fig. 1. Semiconductor chips in the outer space must be tolerant below the heavy ions with the LET of 40 MeV-cm$^2$/mg. Typically, process scaling worsens SERs (soft error rates) per chip[3]. But SERs per logic gate is becoming small especially in SOI since the sensitive volume is scaled[4].

Layout structures influences SERs, however there are lots of unknown effects on nanometer devices. Pulse quenching effects decrease single event transient pulse width causing soft errors[5]. If the distance of adjacent transistors is close, charge sharing decreases the pulse widths on the bulk process[6]. Layout structures give some amount of stress to transistors. Local stress effects caused by Shallow Trench Isolation (STI) enhance or degrade performance of transistors[7], [8]. Stress effects on entire chips improve the soft-error tolerance of SRAM on 40 nm bulk[9]. However, local stress effects on the soft-error tolerance has not been investigated.

In this paper, we evaluate soft-error tolerance of Flip-flops (FFs) fabricated in 28 nm and 65 nm FDSOI technologies. Test chips includes three FFs with different layout structures but identical layout areas to investigate how stress or pulse quenching affects soft error hardness. Their radiation hardnesses were investigated by heavy ion irradiation. Section II shows the layout structures of FFs and test chips. Section III shows experimental method and how to evaluate soft-error tolerances. Section IV shows experimental results and discussion. Section V concludes this paper.

II. DESIGN

In Fig. 2, the structure of a FDSOI (Fully Depleted Silicon On Insulator) CMOS process. It has higher tolerance for soft errors than bulk. BOX layers under transistors eliminate charge by a particle hit from collecting to drain. Two chips were fabricated by the 28 nm and 65 nm thin-BOX FDSOI processes called SOTB (Silicon on Thin-BOX) and UTBB (Ultra Thin Body and BOX) respectively[11], [12]. In Table I, parameters of 28 nm UTBB and 65 nm SOTB. They can control body biases through 25 nm and 10 nm thin BOX layers. Three different layout structures of delayed flip-flops (DFFs) are implemented on the fabricated chips.

A. Layout Structures of Flip-Flops

In Figs. 3 and 4, the layout structures and schematics.

B. Test Chips

Test chips fabricated in 65 nm bulk/SOTB and 28 nm UTBB are shown in Fig. 5. The test chip on the 65 nm bulk process is fabricated compare the soft-error tolerance with the 65 nm SOTB. Several types of DFFs with different layout structures L0, L1, and L3 are embedded in two test chips as shown in Fig. 6. All DFFs are connected as a shift register.
III. Heavy Ions Irradiation Test

Heavy ion irradiation was carried out at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA). Fig. 7 shows a vacuum chamber and an engineering tester. The radiation hardness were investigated by three ions as described in Table II.

We measured the number of upsets caused by heavy ions as below.

1) Initialize serially-connected FFs.
2) Heavy ions are exposed with the static conditions without applying clock signals.
3) Read out all FFs to count the number of upsets.

Ion exposures are done by the static conditions of (DATA, CLK) = (1, 0), (0, 0). Slave latches repeated for hold the state when CLK = 0. Measurements were five times per one of the conditions by Ar and Kr. By Ne but, they are carried out three times. The cross section ($CS$) is used in order to evaluate soft-error tolerances. Eq. 1 is used in order to calculate the $CS$[13].

$$CS \ [cm^2/bit] = \frac{N_{error}}{N_{ion} \times N_{FF}}$$

The $CS$ is calculated from the number of errors ($N_{error}$), the number of ions per unit area ($N_{ion}$), and the number of FFs ($N_{FF}$).

IV. Experimental Results

$CS$ of FFs by heavy-ion irradiation on 65 nm bulk, SOTB, and 28 nm UTBB are shown in Table III and Fig 8. The
average of all static conditions were calculated. The $CS$ of 65 nm SOTB at 1.0V by Kr is 1/50 of 65 nm bulk and 18x higher than 28 nm UTBB at 1.0 V.

In Figs. 9 and 10, the $CS$ of the three different layouts in 65 nm and 28 nm. The average of the $CS$ were calculated at two conditions of (DATA, CLK) = (0, 0), (1, 0). On 65 nm SOTB, no distinct difference is observed. But on 28 nm, at Kr with the LET of 40.3 MeV-cm$^2$/mg, the $CS$ of L2 is 2x higher than others.

V. DISCUSSIONS

According to the experimental results, we have these two assumptions to differentiate the tendency of the $CS$ between 28 and 65 nm.

**Charge Sharing and Pulse Quenching:** Single Event Transient (SET) pulses are degraded by charge sharing in L0 and L1. In Table IV, distances between inverters (INVs) and tristate inverters (TINVs) denoted by $D_g$ as described in Fig. 11. This figure also shows pulse quenching effects by charge sharing. These effects do not happen in 65 nm because $D_g$ is larger than the charge sharing region. In 28 nm, charge sharing effects attenuate the pulse width in TINVs of L0 and L1 because $D_g$ is short or the pulse quenching effects are enhanced by irradiation of higher-LET heavy ions[5]. On the other hand, the $CS$ of L2 is 2x higher than those of L0 and L1 in 28 nm because $D_g$ of L2 is longest and STI intercepts charge sharing.

**Stress Effects:** The tolerance against soft errors is fluctuated by stress effects. In order to alleviate mobility degradations from STI pressures, the wafer notch of 65 nm processes is set to $<100>$ orientation[14]. We assume that the wafer notch of 28 nm is also $<100>$. However, stress effects in 28 nm are stronger than 65 nm. The compression stress enhances the hole mobility which promotes charge collection. Due to longer compression strain in 28 nm, collected charge in 28 nm is higher rate of increase than that in 65 nm.

VI. CONCLUSION

We fabricated test chips in 28/65 nm thin-BOX FDSOI technologies including three types of flip-flops with different layout structures. Heavy-ion irradiation shows that the cross sections of 28 nm UTBB at 1.0V by Kr is 1/18 of 65 nm SOTB. No distinct differences by the energy of heavy ions were observed in 65 nm. But in 28 nm, Kr with the LET of 40.3 MeV-cm$^2$/mg doubles the cross section of the layout.

**TABLE III**

<table>
<thead>
<tr>
<th>Heavy ions</th>
<th>Cross Section $[\times 10^{-19} \text{ cm}^2/\text{bit}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kr</td>
<td>$5.29 \times 10^{-2}$</td>
</tr>
<tr>
<td>Ar</td>
<td>$2.18 \times 10^{-2}$</td>
</tr>
</tbody>
</table>

**TABLE IV**

<table>
<thead>
<tr>
<th>Process</th>
<th>$D_g$ [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 nm UTBB</td>
<td>133</td>
</tr>
<tr>
<td>65 nm SOTB</td>
<td>390</td>
</tr>
</tbody>
</table>
with separated diffusions in the slave latch compared to those of shared diffusions. It is because the distance of the inverters and the tristate inverter in the latch is longer and STI intercepts charge sharing diffusions of the inverter and the tristate inverter in the latch with separated diffusions. For the outer space applications such as satellites, it is better to sharing diffusions of the inverter and the tristate inverter in latches to enhanced soft-error tolerance.

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REFERENCES


