Negative Bias Temperature Instability Caused by Plasma Induced Damage in 65 nm Bulk and Silicon On Thin BOX (SOTB) Processes

Ryo Kishida, Azusa Oshima and Kazutoshi Kobayashi
Department of Electronics, Graduate School of Science and Technology, Kyoto Institute of Technology

***Abstract*—Reliability degradation caused by plasma induced damage (PID) has become a significant concern with the miniaturization of electronic devices. In this paper, we investigate negative bias temperature instability (NBTI) caused by PID measuring frequencies of ring oscillators with an antenna on a single stage. We fabricated a chip in 65 nm bulk and Silicon On Thin BOX (SOTB) processes. Degradation rates of NBTI are equivalent among antenna structures in the antenna ratio (AR) of 5k and 500. NBTI is accelerated by PID in AR of 50k. NBTI degradation caused by PID is equivalent in the bulk and SOTB. SOTB also prevents PID by connecting an antenna to a drain as same as the bulk.**

I. Introduction

In recent years, device size of semiconductor chip is becoming smaller. It has brought a lot of advantages, for example, a semiconductor device can be made highly integrated, improved operating frequency, reduced power consumption and so on. However, reliability problems have appeared in nanometer scales. Particularly, the degradation of reliability caused by Plasma Induced Damage (PID) has become a significant concern with the miniaturization of the device size [1]. Threshold voltage ($V_{\rm th}$) increases due to PID, which results in decreased frequency on operation. There is also negative bias temperature instability (NBTI) in the reliability problems. NBTI also impacts the $V_{\rm th}$ by raising it overtime. The impact of NBTI has been studied by many researches [2], [3]. The temporal shift in $V_{\rm th}$ of the transistor due to NBTI is accelerated by PID [4], [5]. Evaluating and preventing PID has become important. There is a method to prevent PID by connecting an antenna to a drain, but silicon-on-insulator (SOI) may not prevent PID by this method because buried oxide (BOX) layer disturbs the preventing. We fabricated a chip to evaluate PID in both bulk and Silicon On Thin BOX (SOTB), which is a type of SOI, processes. We measured frequencies of ring oscillators with an antenna structure on a single stage.

II. Degradation Caused by Plasma Induced Damage (PID)

An antenna is a metal wire that collects charge at the plasma etching process. During the production of MOSFETs, an aluminum wire collects charge because it is processed by plasma etching directly. A copper wire is being used instead of the aluminum wire in less than 180 nm process because the resistance of the aluminum wire is relatively larger. Although a copper wire is not processed by plasma etching, it collects static charge as shown in Fig. 1. Charge is induced in a metal wire when an interlayer dielectric around metal wires is processed. Plasma induced damage (PID) appears when the antenna is connected to a gate of MOSFETs. PID generates defects into a gate oxide. $V_{\rm th}$ increases when these defects trap carriers. It is explained by the atomistic trap-based BTI model [6] as shown in Fig. 2. Each defect has a time constant (τ) by trapping carriers. These defects induce BTI which is one of the aging degradations. $V_{\rm th}$ increases as voltage and temperature increase with time. BTI degradation is in proportion to a logarithm according to the atomistic trap-based BTI model because time constants are uniformly distributed on the log scale between 10^{-9} and 10^{9} s [7].

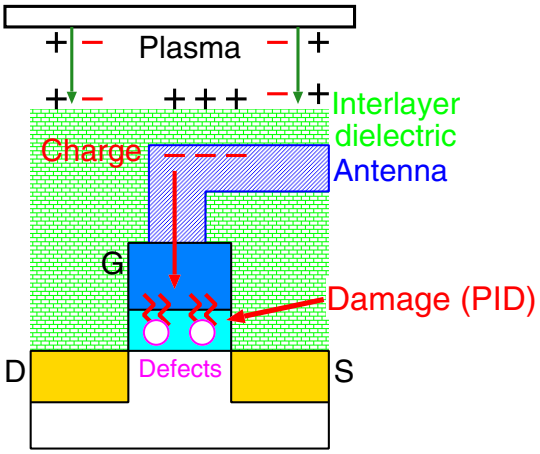


Fig. 1. PID by interlayer dielectric processes.

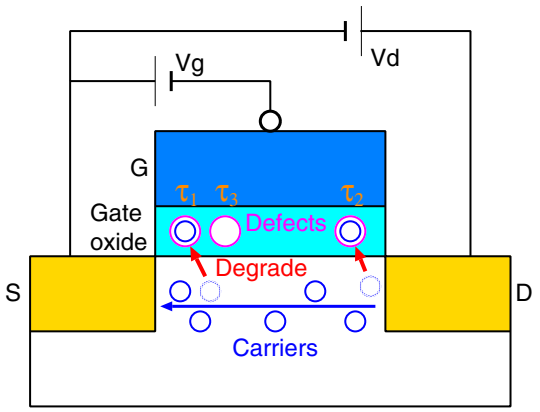


Fig. 2. Atomistic trap-based BTI model.

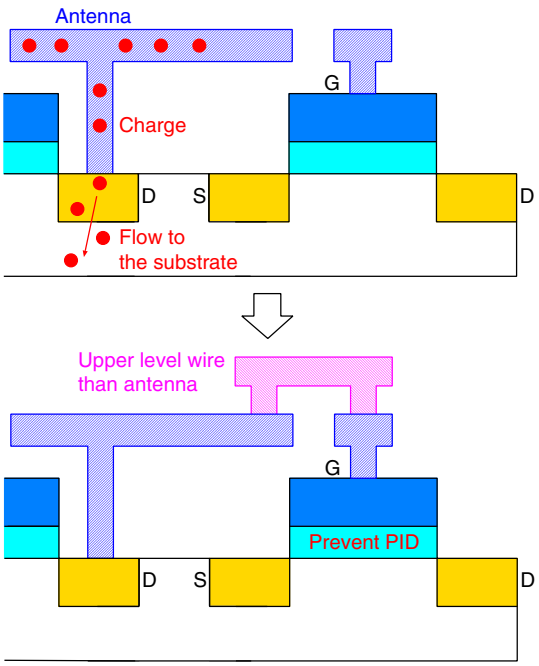


Fig. 3. Preventing PID by connecting the antenna to the drain before connecting to the gate.

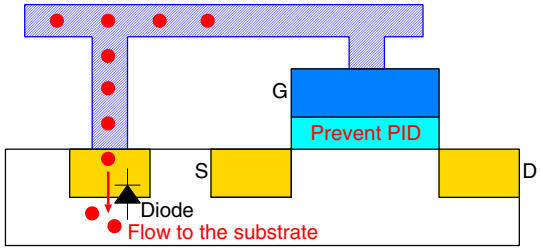


Fig. 4. Preventing PID by the diode.

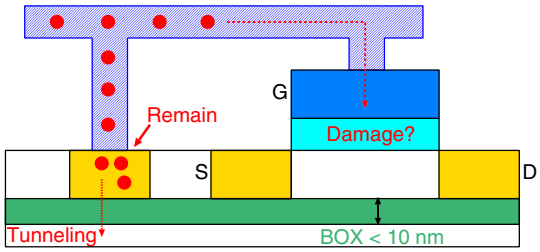


Fig. 5. Charge remaining or tunneling in SOTB.

There are NBTI (Negative BTI) and PBTI (Positive BTI). NBTI occurs in PMOS when V_{gs} is negative. Likewise, PBTI is observed in NMOS especially in technologies less than 45 nm with high-k gate dielectrics [8]. We consider only NBTI because our chip is fabricated in 65 nm.

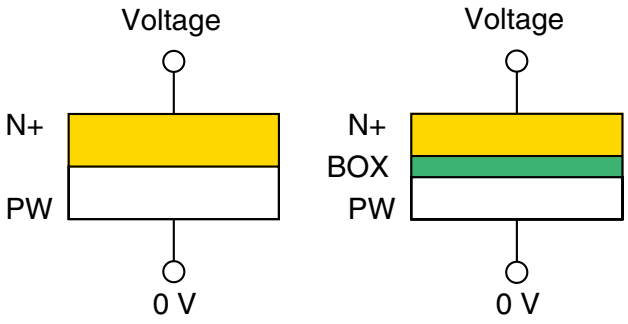
There are several methods to prevent PID. Fig. 3 shows one of those methods using a PN junction formed with drain and substrate regions as a discharge path. Charge flows to the substrate through the drain by connecting the antenna to the drain before connecting the antenna to a gate. The other method is using an isolated PN junction as a diode as shown in Fig. 4. The diode is inserted near a MOSFET which has the gate connected the antenna. Charge flows to the substrate through the diode. But silicon-on-insulator (SOI) does not prevent PID in the drain because it has buried oxide (BOX) layers embedded on a wafer between a body and a substrate. Charge remains in the drain and flows to another gate of MOSFETs. Silicon on thin BOX (SOTB) is a type of fully depleted silicon-on-insulator (FD-SOI) processes [9]. It reduces variations due to impurities because it does not add any dopant to a channel of MOSFETs. A special feature of SOTB is that the BOX layer is less than 10 nm. SOTB can control a back bias because of the thin BOX layer. It may prevent PID because charge flows to the substrate by quantum tunneling as shown in Fig. 5 in a similar manner as flash memories [10]. We measured substrate leakage in a single transistor if charge flows to the substrate. Fig. 6 shows circuits for measurement of substrate leakage. The voltage of the substrate is 0 V. We measure currents between the drain (N+ region) and the substrate by changing the drain voltage. Fig. 7 shows the results of the measurement of substrate leakage. These results are the averages of five transistors. The substrate leakage of the SOTB starts to increase from more than 2 V. Although the leakage current is too low to cause any problem in nominal operations, charge can pass through the thin BOX layer by quantum tunneling. We assume that the SOTB can prevent PID by connecting the antenna to the drain.

III. Measurement Circuits

We fabricated 11-stage ring oscillators (ROs) which have different antenna structures in a 65 nm bulk and SOTB processes. Note that the layout patterns are exactly the same in both processes except for the BOX layer. The 11-stage RO is composed of NOR gates [11] as shown in Fig. 8. We prepare an antenna which has large area. The antenna is connected to the NOR gate on the last stage. The NOR gate with the antenna at the input suffers from PID. The NOR gate at the first stage may get larger PID because a feed back wire is relatively long. A diode is inserted at the NOR gate at the first stage in order to prevent PID on it.

The RO composes NORs without NBTI as shown in Fig. 9. The NOR with NBTI next to the antenna is placed as shown in Fig. 10 in order to induce NBTI only in the NOR connected to the antenna. We call the PMOSFET in the NOR gate near VDD $\mathrm{PMOS_A}$ and the opposite one $\mathrm{PMOS_B}$. The RO stops when ENB controlling oscillation is “1”. The output of the NOR is “0”. There is no NBTI in $\mathrm{PMOS_B}$ since A is connected to ENB as shown in Fig. 9. The reason is that V_{gs} of the $\mathrm{PMOS_B}$ is 0 V. Conversely, $\mathrm{PMOS_A}$ gets NBTI if B is connected to ENB because V_{gs} of $\mathrm{PMOS_A}$ is less than 0 V as shown in Fig. 10.

Fig. 11 shows connection structures of antennas. M1, M2 and M3 are the first-, second- and third-level metal wires, respectively. M1 is processed earliest in the metal wires. We



(a)Bulk. (b)SOTB.

Fig. 6. Circuits for measurement of substrate leakage.

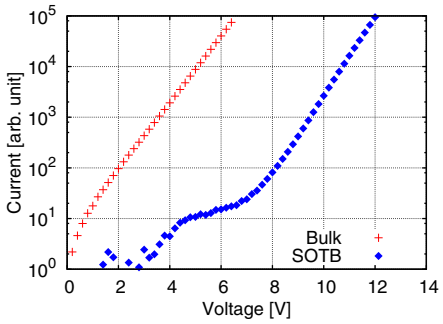


Fig. 7. Results of substrate leakage measurement.

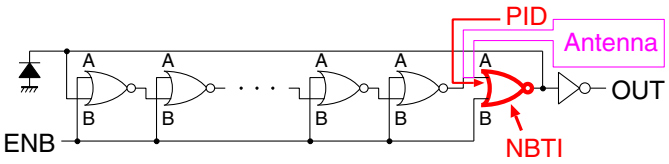


Fig. 8. 11-stage ring oscillator for measuring frequencies of PID.

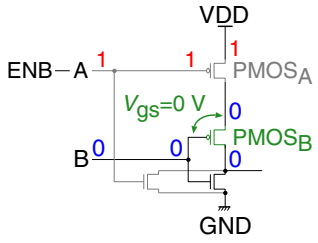


Fig. 9. NOR without NBTI.

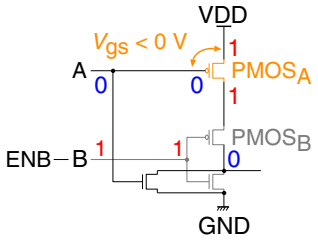
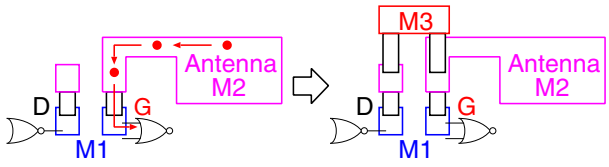
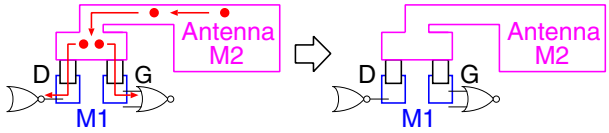


Fig. 10. NOR with NBTI.

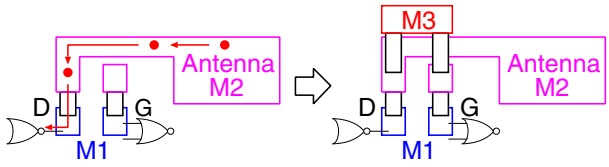
use M2 as the antenna. (a) AG (Antenna is connected to the Gate) induces PID most because all charge in the antenna flows to the gate first. (b) DG (antenna is connected to the Drain and Gate) prevents PID to some extent because the metal wire is connected with a gate and a drain simultaneously. Although charge flow to the gate, some charge flow to the substrate through the drain. (c) AD (Antenna is connected



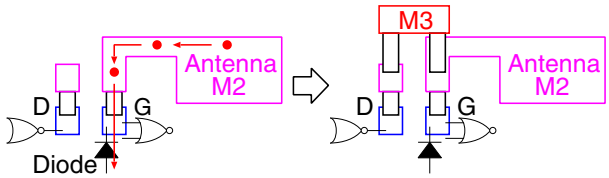
(a) AG. PID is caused because all charge flows to the gate.



(b) DG. PID is prevented by some amount because charge flows to the gate and drain.



(c) AD. PID is prevented at most because charge flows to the drain and does not flow to the gate.



(d) Diode. PID is prevented even if the antenna is connected to the gate because charge flows to the substrate through the diode.

Fig. 11. Connection structures of the antenna.

to the Drain) prevents PID most because charge flows to the substrate through the drain. (d) Diode also prevents PID even if the connection is as same as AG because the charge flows to the substrate through the diode. However, the DG, AD and Diode in SOTB may induce PID as same as the AG because the BOX layer disturbs charge flow.

The antenna ratio (AR), which is the area of an antenna divided by the area of a gate, indicates the strength of PID. The damage due to PID is more when the AR is more. The upper limit of AR is 500 in the antenna rule. We prepared ROs with three ARs that are 500, 5k (5,000), and 50k (50,000). AR500, 5k and 50k have 96, 98 and 70 ROs on a chip, respectively.

IV. Results and Discussions

We measure average oscillation frequencies and NBTI degradation of ROs. The measurement condition is at 1.5 V and 80°C to accelerate NBTI degradation. The inverter connected to an antenna is stressed when ENB is "1". We

keep ENB at "1" except when we measure its oscillation frequencies. We set ENB at "0" only for 24 μs during measurement phase. The degradation rate is based on the initial average frequency of each structure by calculating the following equation.

$$\text{Degradation Rate} = \frac{F_0 - F(t)}{F_0} \quad (1)$$

F_0 is the initial frequency at $t = 0$ s and $F(t)$ is the frequency at time t. Fig. 12 shows results of NBTI degradations in the bulk. Dots are average of degradation rate in measurements and solid lines are fitting functions of Eq. (2). This equation is followed by the atomistic trap-based BTI model.

$$f(t) = a * \log(t) + b \quad (2)$$

If the fitting parameter a is larger, NBTI degradation is larger. Table I shows the fitting parameter a of all structures.

All of the dots and lines overlap among antenna structures in the AR of 500 as shown in Fig. 12(a). Fitting parameter a of AG and AD are 0.161 and 0.157, respectively. The NBTI degradation is almost equivalent in AR of 500. Fig. 12(b) shows the NBTI degradation in the AR of 5k. This result is also equivalent to the result in the AR of 500. There is no effect of NBTI caused by PID in those small AR.

Fig. 12(c) shows the NBTI degradation in the AR of 50k. The AG relatively increases with time. The AG degradation rate is over 1.5 times larger than the others. Fitting parameter a of AG and AD are 0.374 and 0.331, respectively. NBTI degradation increases if PID is larger. PID generates defects and NBTI increases because the defects trap carriers. The AD, DG and Diode structures are almost same degradation rate. PID is prevented by connecting an antenna to a drain even if the antenna is connected to a gate such as DG. The diode also prevents PID because charge flows to a substrate through the diode. If a designer of a chip obey the antenna rule, there is no effect of PID to NBTI. However, NBTI degradation is accelerated in the chip that of AR is 100 times larger than the upper limit of the antenna rule.

Fig. 13 shows the NBTI degradation in the SOTB. The NBTI degradation is almost equivalent in bulk and SOTB. SOTB can prevent PID by connecting an antenna to a drain as same as the bulk. We assume that charge passes through the BOX layer less than 10 nm by quantum tunneling because there is no other route of charge flow. We have shown the substrate leakage of SOTB by the quantum tunneling in section 2. Charge of the antenna can flow to the substrate even if there is the thin BOX layer. SOTB can prevent PID by connecting the antenna to the drain.

TABLE I
FITTING PARAMETER a OF EACH STRUCTURE

	AG	AD	difference
AR500:Bulk	0.161	0.157	0.004
AR500:SOTB	0.240	0.236	0.004
AR50k:Bulk	0.374	0.331	0.043
AR50k:SOTB	0.375	0.322	0.053

V. CONCLUSION

We fabricated ring oscillators with antenna structures to verify PID in 65 nm bulk and SOTB processes and measured their frequencies. NBTI degradation is equivalent among antenna structures in less than the AR of 5k. In the AR of 50k, NBTI increases in the AG structure caused by PID most. NBTI has some correlation with PID because it generates defects into gate oxide and defects trap carriers. The NBTI degradations are equivalent in AD, DG and Diode structures. Connecting the antenna to the drain or the diode can prevent PID. Both bulk and SOTB prevent PID by connecting an antenna to a drain. Charge can pass through thin BOX layers of less than 10 nm by quantum tunneling. The thin BOX layers of 10 nm in SOTB are effective in relieving reliability issues besides the back bias controllability.

ACKNOWLEDGMENT

This work was done in "Ultra-Low Voltage Device Project" of LEAP funded and supported by METI and NEDO. The TEG for this work was designed by utilizing the EDA system supported by the VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys Inc., Cadence Design System and Mentor Graphics Inc.

REFERENCES

[1] R. Kishida, A. Oshima, M. Yabuuchi, and K. Kobayashi, "Initial and long-term frequency degradation on ring oscillators from plasma induced damage in 65 nm bulk and silicon on thin BOX processes," in *SSDM*, 2014, pp. 52–53.

[2] S. Arasu, M. Nourani, F. Cano, J. Carulli, and V. Reddy, "Asymmetric aging of clock networks in power efficient designs," in *ISQED*, 2014, pp. 484–489.

[3] V. Huard, C. Parthasarathy, C. Guerin, T. Valentin, E. Pion, M. Mammasse, N. Planes, and L. Camus, "NBTI degradation: From transistor to SRAM arrays," in *IRPS*, 2008, pp. 289–300.

[4] W. H. Choi, S. Satapathy, J. Keane, and C. H. Kim, "A test circuit based on a ring oscillator array for statistical characterization of plasma-induced damage," in *CICC*, 2014, p.14-3.

[5] K. S. Min, C. Y. Kang, O. S. Yoo, B. J. Park, S. W. Kim, C. Young, D. Heh, G. Bersuker, B. H. Lee, and G. Y. Yeom, "Plasma induced damage of aggressively scaled gate dielectric (EOT $<$ 1.0nm) in metal gate/high-k dielectric CMOSFETs," in *IRPS*, 2008, pp. 723–724.

[6] H. Kukner, S. Khan, P. Weckx, P. Raghavan, S. Hamdioui, B. Kaczer, F. Catthoor, L. Van der Perre, R. Lauwereins, and G. Groeseneken, "Comparison of reaction-diffusion and atomistic trap-based BTI models for logic gates," *IEEE Trans. on Dev. & Mat. Rel.*, vol. 14, pp. 182–193, 2014.

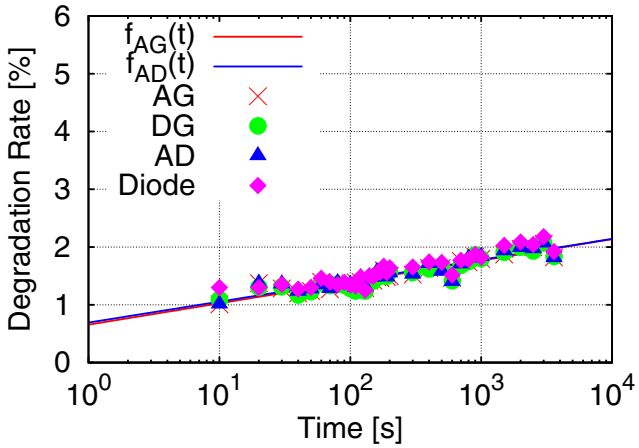
[7] B. Kaczer, S. Mahato, V. de Almeida Camargo, M. Toledano-Luque, P. Roussel, T. Grasser, F. Catthoor, P. Dobrovolny, P. Zuber, G. Wirth, and G. Groeseneken, "Atomistic approach to variability of bias-temperature instability in circuit simulations," in *IRPS*, 2011, pp. XT.3.1–XT.3.5.

[8] S. Zafar, Y. Kim, V. Narayanan, C. Cabral, V. Paruchuri, B. Doris, J. Stathis, A. Callegari, and M. Chudzik, "A comparative study of NBTI and PBTI (charge trapping) in SiO2/HfO2 stacks with FUSI, TiN, re gates," in *VLSI Tech. Symp.*, 2006, pp. 23–25.

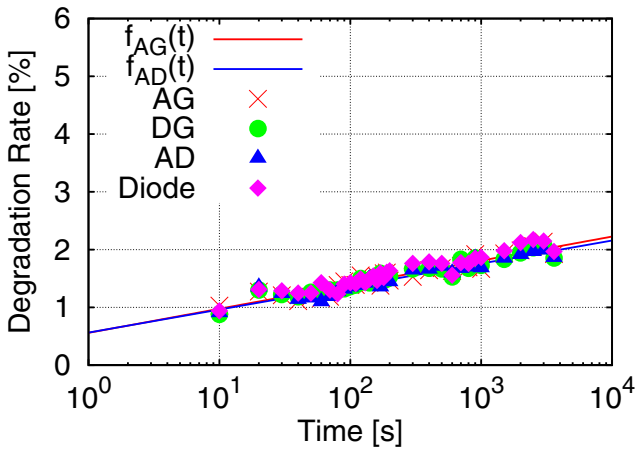
[9] R. Tsuchiya, M. Horiuchi, S. Kimura, M. Yamaoka, T. Kawahara, S. Maegawa, T. Ipposhi, Y. Ohji, and H. Matsuoka, "Silicon on thin BOX: A new paradigm of the CMOSFET for low-power high-performance application featuring wide-range back-bias control," in *IEDM*, 2004, pp. 631–634.

[10] T. Hori, "Gate dielectrics and MOS ULSIs: Principles, technologies, and applications," *Springer series in electronics and photonics*, 1997.

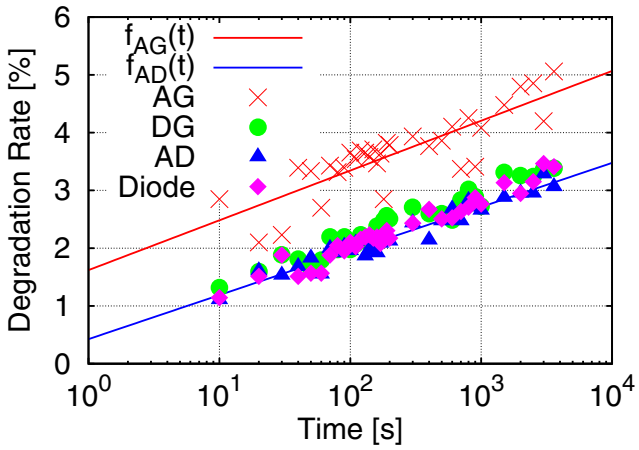
[11] B. P. Linder, J.-J. Kim, R. Rao, K. Jenkins, and A. Bansal, "Separating NBTI and PBTI effects on the degradation of ring oscillator frequency," in *IIRW*, 2011, pp. 1–6.



(a) AR500:bulk.

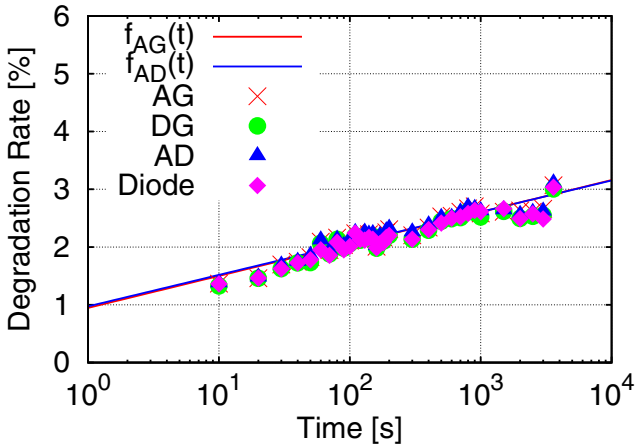


(b) AR5k:bulk.

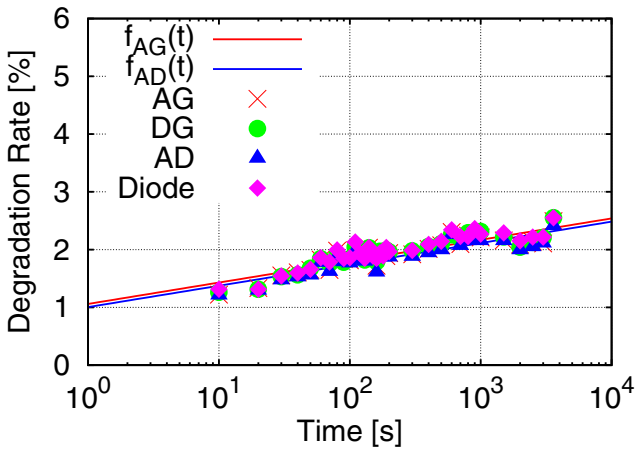


(c) AR50k:bulk.

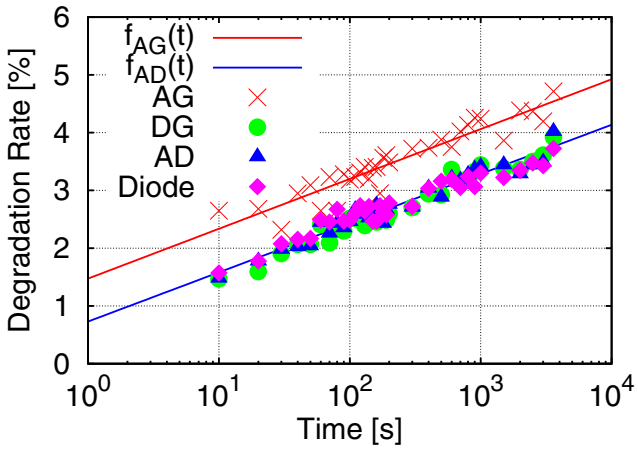
Fig. 12. Measurement results of NBTI degradation in bulk.



(a) AR500:SOTB.



(b) AR5k:SOTB.



(c) AR50k:SOTB.

Fig. 13. Measurement results of NBTI degradation in SOTB.