# Impact of Body Bias on Soft Error Tolerance of Bulk and Silicon on Thin BOX Structure in 65-nm Process

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***Abstract*— We analyze the soft error tolerance of DFF in 65-nm bulk and SOTB (Silicon on Thin BOX) process by alpha and neutron experiments and device-simulations. The experimental results reveal that by increasing the reverse body bias the soft error rate in the bulk structure is increased, while the number of soft errors in SOTB structure is decreased. The results from device-simulation show that the collected charge of bulk structure is increased, while the collected charge is decreased in SOTB as the reverse body bias increases.**

## I. Introduction

SEU (Single Event Upset) is caused by radiation induced charge collection at a single sensitive node, such as the drain region of a single transistor. Radiation-hardened circuits, such as Triple Modular Redundancy (TMR), Built-in Soft Error Resilience (BISER)[1], or Dual Interlocked storage CEll (DICE)[2] have been employed to suppress the effects of charge collection at a single circuit node. Silicon on Insulator (SOI) structure can suppress the charge collection by the BOX (Buried OXide)[3]. The soft error tolerance of SOI is stronger than bulk structure by TCAD simulation[4] and experiments[5], [6]. Silicon On Thin BOX (Buried OXide) (SOTB)[7] is an FDSOI with a thin BOX layer. It also can suppress the charge collected into device by the thin BOX. There is no dopant in the channel of SOTB. Variations are suppressed. Thus, the supply voltage of SOTB can be decreased to 0.5V[8].

The aggressive process scaling the charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the drift and diffusion, also the bipolar effect become dominant when a single event occur in the circuit[9]. Bipolar effect is closely related with the well potential[10].

Moreover, it is commonly used to reduce power consumption by body biasing. The charge collection and well potential is also influenced by body bias when a particle hits device in 130-nm process[11]. As the above factors, the soft error tolerance of the radiation-hard structures are changed a lot in 65-nm process. Thus, it is important to analyze the soft error tolerance of the conventional latch in bulk and SOTB structure by body biasing.

In this paper, we analyze the impact of reverse body bias on the soft error tolerance of the bulk and SOTB latch in a 65-nm process by alpha and neutron experiments and device-simulations. This paper is organized as follows. Section II describes device-simulation results. Section III shows the alpha and neutron experiment results. section IV concludes this paper.

## II. Impact of Body Bias on Soft Error Tolerance by Device-Simulation

### A. Simulation Setup

Fig. 1 shows a conventional latch circuit in a 65-nm process technology. A radiation particle hits the NMOS transistor of the inverter I0 perpendicularly. The layout structure of the latch is also shown in Fig. 1. Well contacts are placed side by side in the same rows. The nodes N1 is set as "1". We apply the reverse body bias on the device model from 0 V to 1.0 V. Based on the circuit and layout structures, the cross-section of 3D device-level NMOS models in bulk and SOTB structures are shown in Fig. 2. There is a thin BOX under the SOI body in the SOTB model as shown in Fig. 2(b). The thickness of the thin BOX and the SOI body is 10-nm and 12-nm respectively.

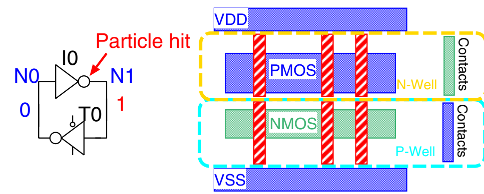
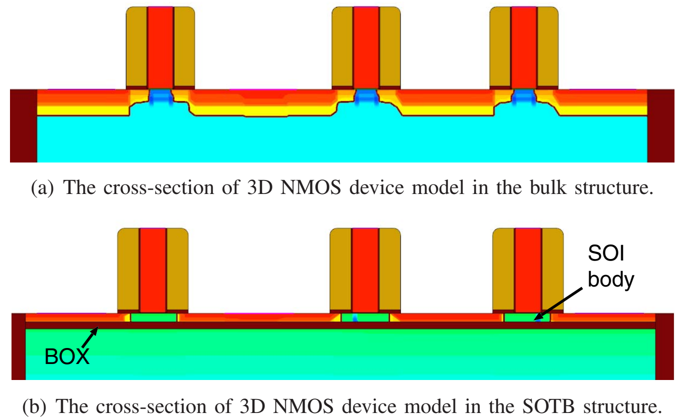



Fig. 1. A conventional latch and its layout structure.




(a) The cross-section of 3D NMOS device model in the bulk structure.

(b) The cross-section of 3D NMOS device model in the SOTB structure.

Fig. 2. The device-level models.

### B. Simulation Results in Bulk Structure

The current pulses of node N1 influenced by reverse bias in the bulk structure are shown in Fig. 3, when a heavy ion particle hits the drain of NMOS. LET of the particle is 1.5

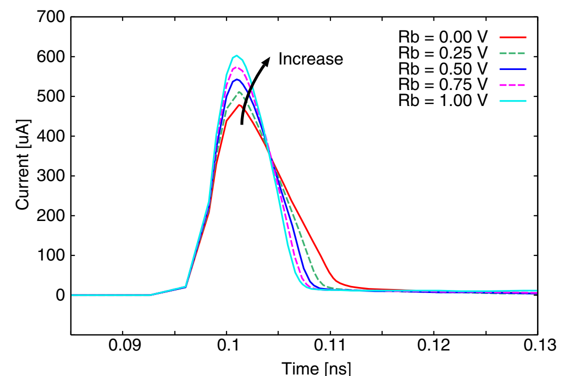



Fig. 3. The current pulses of N1 influenced by reverse bias in the bulk structure. (LET=1.5 MeV·cm$^2$/mg)

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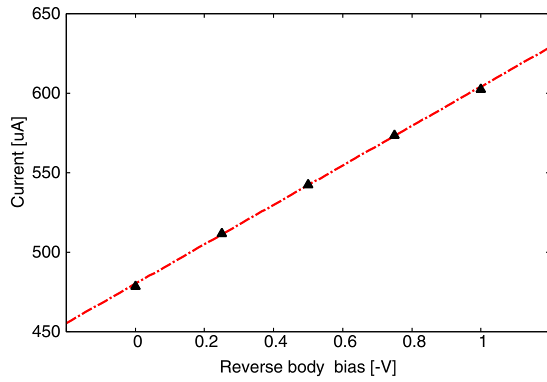



Fig. 4. Peak values of the current pulses influenced by reverse bias in bulk structure.

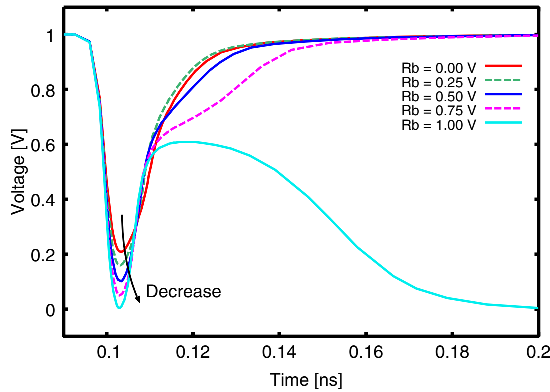



Fig. 5. The output voltages of N1 influenced by reverse bias in the bulk structure. (LET=1.5 MeV·cm$^2$/mg)

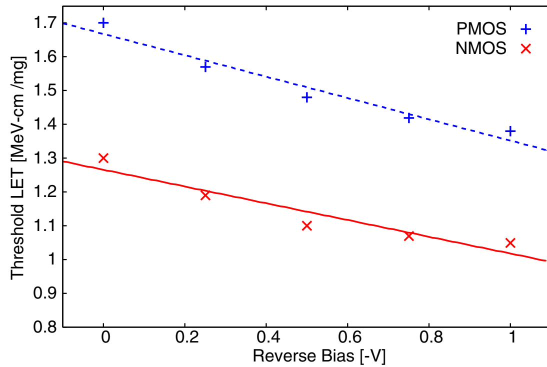



Fig. 6. Threshold LET influenced by reverse bias in bulk structure.

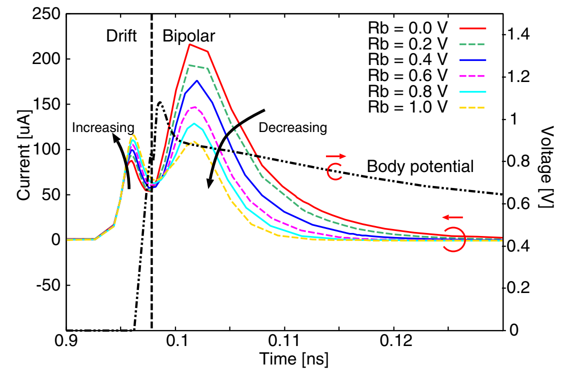



Fig. 7. The current waveforms of node N1 influenced by reverse bias in the SOTB structure.

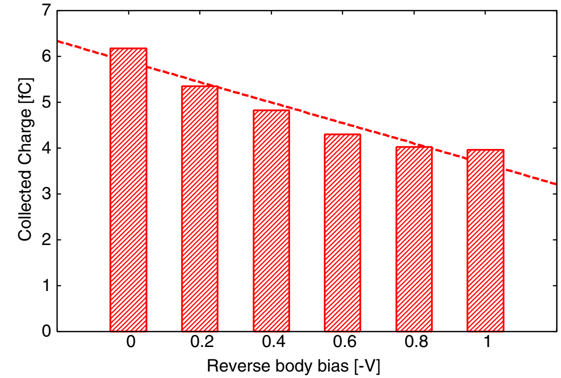



Fig. 8. The collected charge influenced by reverse bias in the SOTB structure.

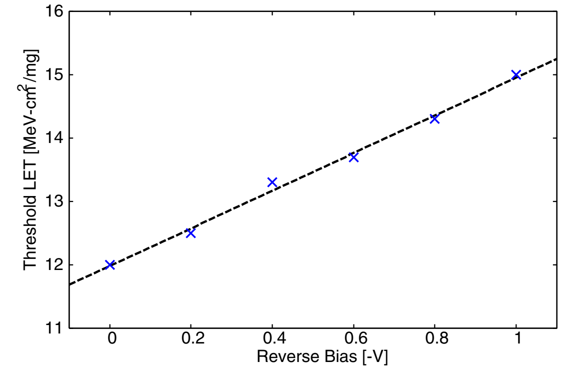



Fig. 9. The threshold LET influenced by reverse bias in the SOTB structure.

MeV·cm$^2$/mg. The reverse bias is increased from 0 to 1.0 V in increments of 0.25 V.

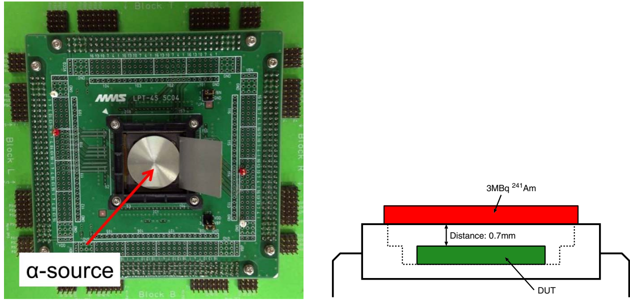
In bulk structure, the drift and diffusion mechanisms are the main factors of charge collection by a particle hit. Fig. 4 shows the peak values of the current pulses influenced by reverse body bias. As the reverse body bias widens the depletion region, more charge is collected into drain by drift after the particle hit. The peak values of the current pulses is linearly increased as shown in Fig. 4.

Fig. 5 shows the output voltages of node N1 by a particle hit, when increasing the reverse body bias. As more charge is collected into node N1, the output voltage of the latch reduces much more as the reverse body bias increases. It makes the bulk latch becomes more sensitive to a particle hit. The collected charge by a particle hit becomes larger than the $Q_{crit}$ of the bulk latch, when the reverse body bias is increased to 1.0 V. Node N1 is upset as shown in Fig. 5.

The threshold LET which flips the latch is shown in Fig. 6, when we apply the reverse bias on NMOS. The threshold LET decreases by increasing the reverse bias. The tolerance of bulk latch becomes weaker as the reverse body bias increases. Fig. 6 also shows the threshold LET when the reverse bias is applied on PMOS. The threshold LET also decreases by increasing the reverse bias. However, the threshold LET of PMOS is about 30% higher than that of NMOS. Thus, NMOS is much more sensitive than PMOS when reverse bias is applied on latches.

### *C. Simulation Results in SOTB Structure*

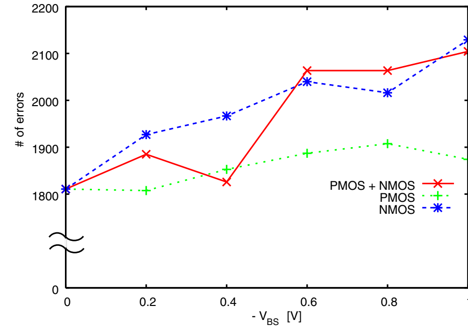
The pwell bias which influences current pulses of N1 are shown in Fig. 7 when a 1.5 LET particle hit the SOTB latch.



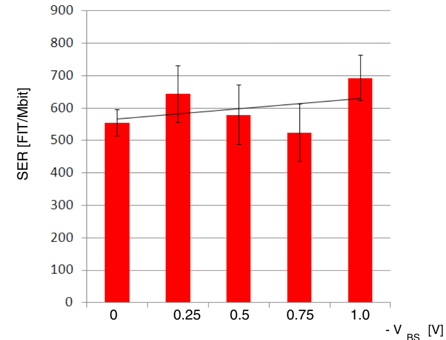

(a) Photo of the alpha source and chip.

(b) Image of the alpha experiments, the distance between alpha source and chip is 0.7 mm.

Fig. 10. Alpha experiment setup.




(a) Number of soft errors of one chip by alpha experiments




(b) Error rates of bulk structure by neutron experiments

Fig. 11. Experimental results of bulk structure.

There are two parts in the current pulse. The first part is caused by drift and the second part is caused by the bipolar effect. It is because that the potential of SOTB body increases to 0.6 V as shown in Fig. 7. It clearly shows that the second part current pulse of the SOTB is much larger than the first part. The first current pulse is very low because the drift mechanism is suppressed by the thin BOX. The bipolar effect becomes the main factor of charge collection in SOTB structure. When increasing the reverse body bias of the SOTB structure, little more charge is collected into the latch by drift. The peak values of the first part waveforms increase as shown in Fig. 7. However, the reverse bias also suppresses the elevation of well potential after the particle hit. The bipolar effect is suppressed. Thus, the peak values of second parts decrease by increasing the reverse bias.

Fig. 8 shows the volumes of collected charge of SOTB structure. The collected charge reduces by 50% as applying 1.0V reverse bias on NMOS of SOTB latch. The threshold LET influenced by increasing the reverse bias on NMOS of SOTB latch is shown in Fig. 9. The threshold LET of SOTB latch is 10 times higher than the bulk structure. The tolerance of SOTB structure is stronger to particle hits than the bulk structure. The threshold LET increases as the reverse body bias as shown in Fig. 9. According to the device simulations, the tolerance of bulk conventional latch becomes weaker by applying the reverse bias on the well. However, the tolerance of SOTB becomes stronger as the reverse body bias increases. The threshold LET of SOTB is 10 times higher than that of bulk structure.

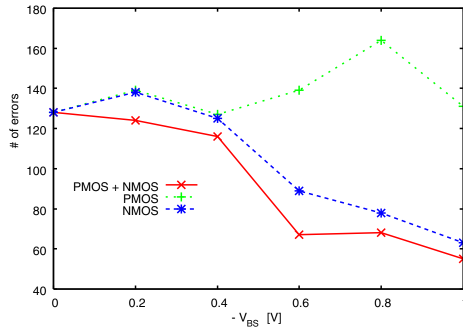
## III. Experimental Results by Alpha and Neutron Irradiation

A test chip was fabricated in 65 nm bulk and SOTB CMOS processes including a general D-FF array to show vulnerabilities of FFs by applying reverse body bias. A 3M Bq alpha source is used in our experiments. Fig. 10 shows the alpha experiment setup. A 3M Bq alpha source is used in our experiments. The distance between alpha source and chip is 0.7 mm. Spallation neutron-beam irradiation were carried out at RCNP of Osaka University.

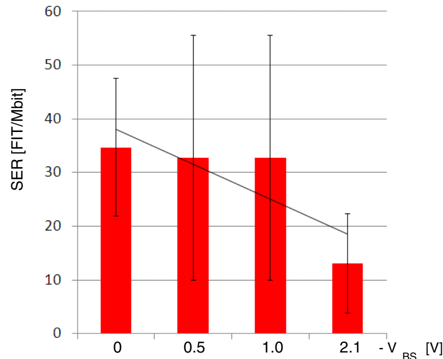
Fig. 11 shows the numbers of soft error of bulk structure by alpha (a) and neutron (b) experiments. The error numbers of one chip by alpha experiments are shown in Fig. 11(a). The clock is 0 and the measuring time is 60s. We apply the reverse bias on NMOS and PMOS. The number of errors increases by 13% when apply 1 V reverse bias on NMOS. However, The number of errors only increases by 5% when applying the reverse bias on PMOS. The tolerance does not change a lot by applying the reverse bias on PMOS. It is because that NMOS is much more sensitive than PMOS as explained in section II.

Fig. 11(b) shows FIT/Mbit of bulk structure by neutron irradiation. We apply the reverse bias on NMOS and PMOS at the same time. The clock is 35 MHz. The soft error rates increases by 27% by applying the 1 V reverse bias when we use the neutron. The alpha and neutron results in bulk structure coincides with device simulations.

Fig. 12 shows the experimental results of SOTB structure. The error numbers from alpha experiments decrease by 60% by applying 1 V reverse bias on NMOS as shown in Fig. 12(a). It is because that the reverse bias suppresses the bipolar effect. Less charge is collected into SOTB. Similar to the bulk structure, the numbers of error does not change a lot when applying the reverse bias on PMOS. It is because that the PMOS have stronger soft error tolerance than NMOS, and most errors occur in NMOS. Note that the soft error rate does not change a lot when the reverse bias is increased to 1.0 V. It is because that the SOTB latch have strong tolerance to soft errors. Only small number of errors occur in the circuit by the neutron experiments. However, the soft error rates decrease by 50% when we increase the reverse bias to 2.1 V. Reverse body bias increases the tolerance of SOTB to soft errors. The experimental results reveal that the tolerance of the SOTB structure is 10 times stronger than the bulk structure in 65-nm process.



(a) Number of soft errors of one chip by alpha experiments



(b) Error rates of SOTB structure by neutron experiments

Fig. 12. Experimental results of SOTB structure.

## IV. Conclusion

We show the soft error tolerance influenced by reverse body bias on the bulk and SOTB structures. According to the results of device simulations, the bulk latch become easier to flip by increasing the reverse bias. The threshold LET linearly increases influenced by reverse bias. The threshold LET of PMOS is 30% higher than that in NMOS. NMOS is much more sensitive than PMOS. In the SOTB structure, the bipolar effect is the main factor of charge collection. The reverse bias suppresses the bipolar effect. Thus, the collected charge reduces by applying the reverse body bias on the SOTB latch. The tolerance of the SOTB latch become stronger by increasing the reverse bias.

The alpha irradiation experimental results show that the number of errors increase by 13% by applying the reverse bias in NMOS the bulk structure. The soft error rates increase by 27% by neutron experiments when apply 1.0 V reverse bias.

In the SOTB structure, the numbers of error reduce by 60% by applying 1.0 V reverse bias on NMOS by alpha experiment. The soft error rate decrease to 50% when we increase the reverse bias to 2.1 V according to the neutron irradiation experiments results. The soft error tolerance of SOTB is 10 times stronger than the bulk structure in 65-nm process.

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