Contributions of Charge Sharing and Bipolar Effects to Cause or Suppress MCUs on Redundant Latches

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***Abstract*— There are two of main factors, charge sharing and bipolar effects to cause or suppress SEUs and MCUs. Technology scaling increases the role of bipolar effects with respect to multiple bit upsets. We analyze contributions of charge sharing and bipolar effects by changing the position of well contacts and the well structure. Device simulation results reveal that charge sharing and bipolar effect are suppressed effectively when the well contacts are placed in the middle of two latches.**

I. Introduction

Radiation induced charge collection at a single sensitive node, such as the drain region of a single transistor, is a possible source of SEU. Radiation-hardened circuits, such as Triple Modular Redundancy (TMR), or DICE[1] have been employed to suppress the effects of charge collection at a single circuit node. As circuits are scaled down, multiple node charge collection has an increasing impact on the response of the circuit[2]. Soft errors have become an increasingly troublesome issue for memories as well as combinational logic circuits. It makes radiation-hardened circuit design more challenging.

Recently, the charge collection mechanism has become more complex due to device shrinking and increasing circuit densities. Not only the charge sharing, also the bipolar effect become dominant when a particle hit on latches or flip-flops. It makes radiation-hardened circuit more sensitive to Multiple Cell Upsets (MCUs)[3]. It is important to suppress the charge sharing and the bipolar effect to mitigate multiple node charge collection.

In this paper, we analyze the impact of charge sharing and bipolar effect on redundant latches by device-level simulations. All device-level models are constructed based on a 65-nm process.

II. Charge Sharing and Bipolar Effects Analysis in Device-Level

A. Simulation Setup

A device simulator Sentaurus is used to do all device level simulations. Fig. 1 shows a circuit including two latches placed in two adjacent rows in a 65nm bulk technology. A radiation particle hits the NMOS transistor of the inverter I0 perpendicularly. The layout structure of the redundant latches in two rows is shown in Fig. 2. All of the NMOS transistors are placed in the same P-well. Well contacts are placed side by side in the same rows. The output nodes (N_{I0}, N_{I1}) of the inverter I0 and I1 are initially set to "1". The redundant latches in two rows are very sensitive to a particle hit. It is easy to analyze contributions of the charge sharing and the bipolar effects between redundant latches. Based on the circuit and layout structures, we construct a 3D device-level NMOS model as shown in Fig. 3. The 3D NMOS is initially constructed in a triple well structure. The distance between the well contacts and latches (D_{WC}) is 2.75 μm. The distance between the two latches L0 and L1 is 0.3 μm as shown in Fig 3. For researching the charge sharing between latches L0 and L1, the radius of ion track model is set to 0.3 μm.

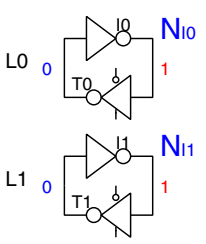


Fig. 1. Redundant latches.

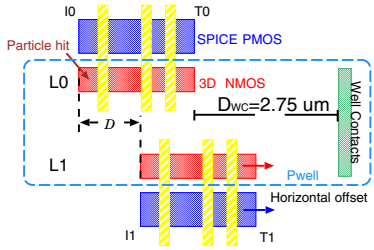


Fig. 2. layout of two latches in two rows.

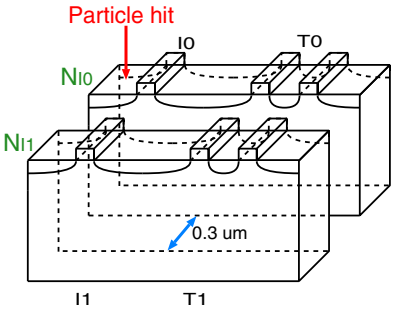
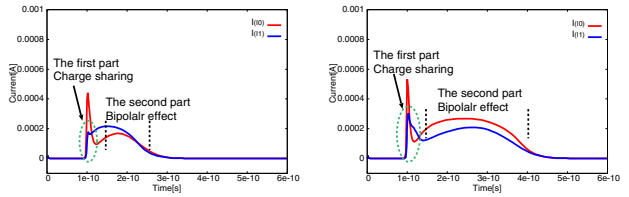


Fig. 3. 3D device-level structure of redundant latches in two rows. A particle hit at the drain of NMOS I0.

B. Charge Sharing and Bipolar Effect in Redundant Latches

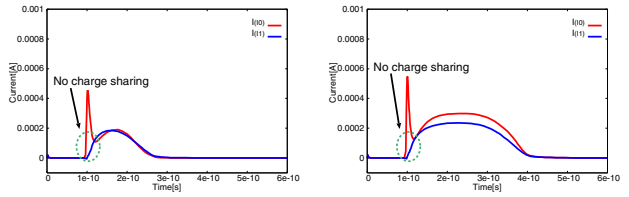
Fig. 4 (a) shows the drain current of inverters I0 and I1 when D=0. A particle with 10 MeV/(mg/cm^2) hits on I0. The current waveform of NMOS in I0 can be divided to two parts. The first part is very steep, that can be modeled by the double-exponential model, while the second part is shallow. From the simulation results, we can obviously recognize that there are two kinds of mechanisms in the whole charge collection. After the particle hit, a large amount of electrons are collected in the drain region immediately. There firstly appears a steep current by the drift. After that, holes still remain in the bulk region, which reduces the source-well potential barrier due to the increase in the potential of the p-well. Thus, the source injects electrons into the channel which can be collected at the drain. This effect is called the parasitic bipolar effect because the source-well-drain of the NMOS transistor acts as a n-p-n bipolar transistor. It will turn on the parasitic bipolar transistor. Then, the parasitic bipolar transistor under the tristate inverters turns on. The bipolar transistor can not turn off until the well potential decreases below 0.6V. The shallow current waveform in the latter part is caused by the bipolar effect.

There are also two parts in the output current of I1 as in Fig. 4 (a). Compared to the first part in the output current of I0, the peak of output I1 becomes much lower. There also exists the shallow current. When we increase the LET of the particle to 20 MeV/(mg/cm^2), the first part of I1 in the output current pulse becomes much steeper as shown in Fig. 4 (b). When D = 0, drift mechanism also occurs in both the inverter



(a) LET=10 MeV/(mg/cm^2) (b) LET=20 MeV/(mg/cm^2)

Fig. 4. Transient drain current (D=0) caused by a particle hit at NMOS in I0.



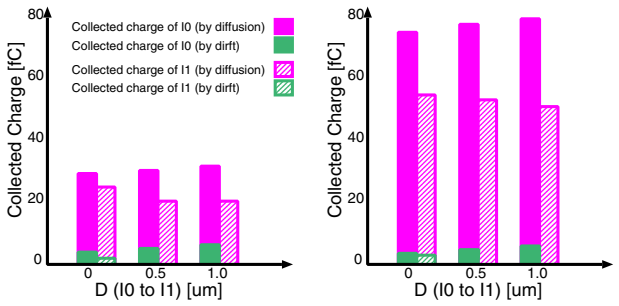
(a) LET=10 MeV/(mg/cm^2) (b) LET=20 MeV/(mg/cm^2)

Fig. 5. Transient drain current (D=0.5 μm) caused by a particle hit at NMOS in I0.

I0 and I1 as shown in Fig. 4, even though the particle does not hit I1 directly. Thus, generated charge is shared between I0 and I1. The charge sharing become stronger by increasing the energy of the particle.

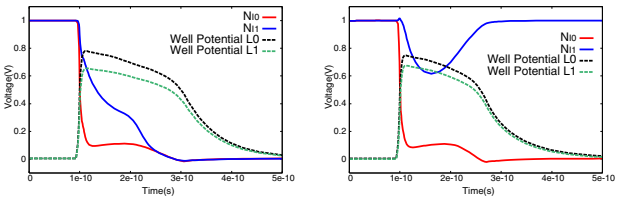
We horizontal offset the latch L1 to increase the distance D between the drain region of NMOS I0 and I1 as in Fig. 2. When D is increased to 0.5 μm, the drain current of I0 and I1 becomes Fig. 5. The output of I0 is still composed of two parts. However, there is no first part in the current waveform of I1. It obviously shows that little charge is collected in I1 by drift. Thus, charge sharing between Latches L0 and L1 is suppressed. The collected charge volume obtained by integrating the current waveforms of I0 and I1 are shown in Fig. 6. The volume of charge collected by drift and the total volume of collected charge are shown in these figures. As the distance D is increased, the collected charge by drift of I1 almost disappears, and the total collected charge become less. However, both parts of collected charge of I0 become larger as shown in Fig. 6. The charge sharing mechanism is suppressed by increasing the D. Thus, more quantity of charge are collected to the inverter I0.

Fig. 7 and 8 are drain output voltages of I0 and I1 when a particle hits on the inverter I0 with 10 and 20 MeV/(mg/cm^2) LET respectively. When D=0, the outputs of I0 and I1 are flipped at the same time as shown in Fig. 7 (a) and 8 (a). However, when the distance D is increased to 0.5 μm, less charge is collected by I1 and more charge is collected by I0, because charge sharing between I0 and I1 is suppressed when increase D. Thus, N_{I1} is not flipped according to the less collected charge as shown in Fig. 7 (b) and 8 (b). When the particle hit increase to 20 MeV/(mg/cm^2) LET, the well potential under latches L0 and L1 keep high for longer time as show in Fig. 8. The bipolar transistor under tristate inverter T0 is turned on, N_{I0} goes back to its initial state by the parasitic bipolar effects[4]. No latch is flipped as shown in Fig. 8 (b). MCUs are suppressed when the distance D is increased to 0.5μm.



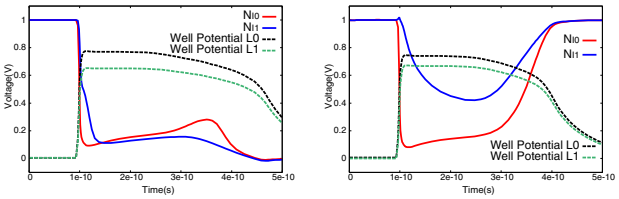
(a) LET=10 MeV/(mg/cm^2) (b) LET=20 MeV/(mg/cm^2)

Fig. 6. Collected charge by D and LET.



(a) D = 0 (b) D = 0.5 μm

Fig. 7. Transient drain voltage caused by a particle hit at NMOS in I0. LET=10 MeV/(mg/cm^2)



(a) D = 0 (b) D = 0.5 μm

Fig. 8. Transient drain voltage caused by a particle hit at NMOS in I0. LET=20 MeV/(mg/cm^2)

III. Suppress the Charge Sharing and the Bipolar Effect

A. Changing the well structure

Fig. 9 and 10 show the device models in the twin well and the triple well respectively. In triple well structure case, the p-well depth is 0.9 μm. Fig. 11(b) shows the volume of collected charge in the twin-well structure. Compared to the collected charge of the triple-well structure as shown in Fig. 11(a), the collected charge by drift mechanism does not change. However the total collected charge decreases by 50% in the twin-well structure. The bipolar effect in the triple well easily occurs than in the twin well, thus more charge is collected in triple-well structure. The drain output voltage of I0 and I1 are shown in Fig. 12 in the twin well. Compared to the output voltages in the triple well as shown in Fig. 7(a)

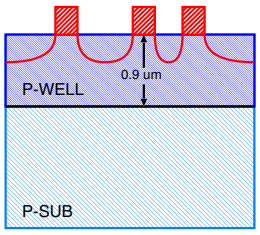


Fig. 9. Twin-well cross-section

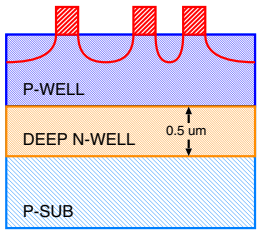
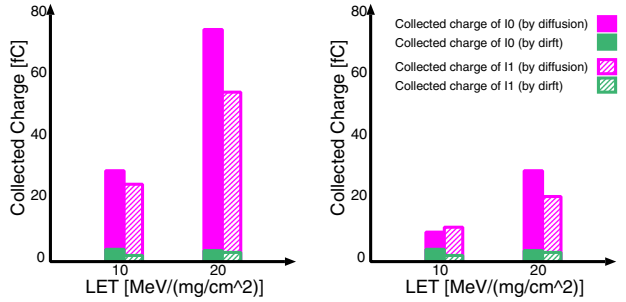
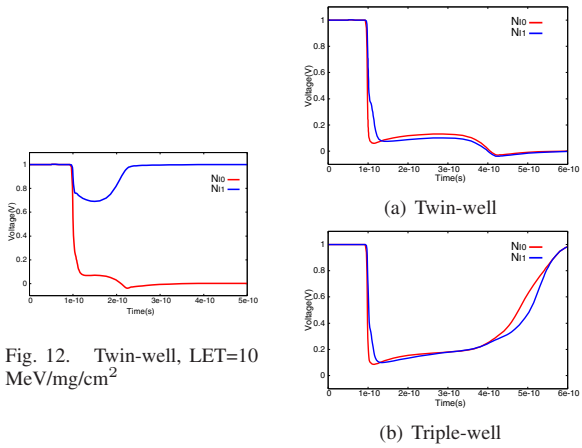


Fig. 10. Triple-well cross-section



(a) Triple-well (b) Twin-well

Fig. 11. Collected charge according to the well structure. The distance between latches L0 and L1 is fixed to 0.3 μm. D = 0.



(a) Twin-well

(b) Triple-well

Fig. 12. Twin-well, LET=10 MeV/mg/cm^2

Fig. 13. Transient drain voltage caused by a particle hit at NMOS in I0. LET = 30 MeV/mg(mg/cm^2)

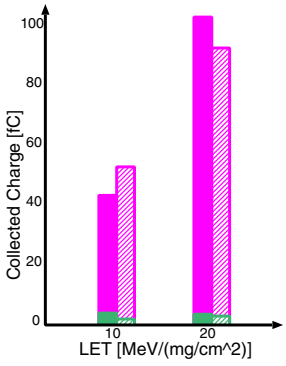
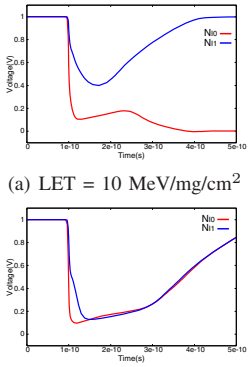


Fig. 14. Collected charge. P-well potential is increased to 0.3V.



(a) LET = 10 MeV/mg/cm^2

(b) LET = 20 MeV/mg/cm^2

Fig. 15. Transient drain voltage caused by a particle hit at I0. P-well potential is 0.3V.

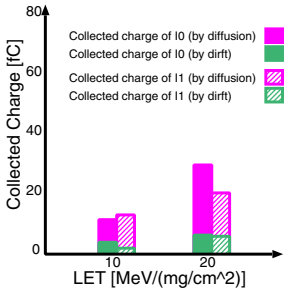
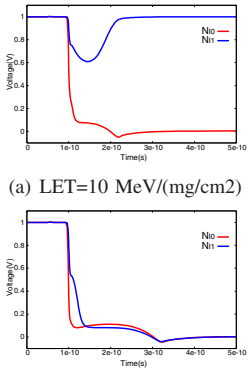


Fig. 16. Collected charge when well contacts are placed at adjacent to redundant latches.



(a) LET=10 MeV/(mg/cm2)

(b) LET=20 MeV/(mg/cm2)

Fig. 17. Transient drain voltage caused by a particle hit at NMOS in I0. The well contacts are placed at adjacent to latches.

and 8(a), the latches L0 and L1 upset at the same time in the triple well, while only L0 upsets in twin-well, when LET is 10 MeV/(mg/cm^2). There is MCU occurrence in triple-well structure while only SEU occurrence in the twin-well structure. When LET is over 30 MeV/(mg/cm^2), however, the outputs N_{I0} and N_{I1} upset at the same time in the twin well as shown in Fig 13(a), while outputs N_{I0} and N_{I1} go back to its initial state in the triple well as shown in Fig. 13(b). Thus, a redundant latch in the twin well is sensitive to higher energy particle, while a redundant latch in the triple well is sensitive to lower energy particle.

B. Changing the well potential

Fig. 14 shows the volume of the collected charge when the p-well potential is increased to 0.3V in the triple-well structure. D is 0 in this case. Compared to the collected charge volume in the triple-well structure as shown in Fig. 11(a), the collected charge by drift mechanism does not change. The total collected charge is about 1.5 times more than Fig. 11(a). The drain voltages are shown in Fig. 15 when particle energies are 10 and 20 MeV/mg/cm^2. The bipolar transistors under the tristate-inverter T0 and T1 become easier to turn on because of the 0.3V well potential. The output of tristate inverter T1 keeps "0" strongly be the parasitic bipolar effects. The output N_{I1} is hard to upset. Only the output N_{I0} is upset when particle energy is 10 MeV/mg/cm^2. When it is increased to 20 MeV/mg/cm^2, the bipolar transistor under T0 turns on. The output N_{I0} goes back to its initial state by the parasitic bipolar effect. Thus in the triple well case, the bipolar transistors under tristate inverters become easier to turn on by increasing the p-well potential. The MCU rate is decreased in this case, because the parasitic bipolar effects suppress MCUs.

C. Changing the position of well contacts

We place the well contacts adjacent to latches, 0.25 μm away from the latches L0 and L1. The distance between the redundant latches (D) is 0. The volume of collected charge of I0 and I1 are shown in Fig. 16. The collected charge caused by drift mechanism does not change. However, Compared to the collected charge in Fig. 11(a) when the distance D_{WC} is 2.75 μm, the total volume of collected charge decreases by 50%. The well potential under latches keeps steady by placing well contacts adjacent to latches. The bipolar effects under the inverter I1 is suppressed. Thus, Less charge is collected to the latch L1. Fig. 17 show the drain voltages when the well contacts are placed adjacent to latches. Only the latch L0 is upset when LET is 10 MeV/(mg/cm^2) as shown in Fig. 17 (a). However, two latches are upset at the same time when LET is 20 MeV/(mg/cm^2).

When the well contacts are placed between latches L0 and L1 as in Fig. 18, the volume of collected charge is shown in Fig. 19. Even though the lower latch is placed as in Fig. 18, there is no charge collected by drift mechanism in N_{I1} as in Fig 19. Total charge collected by I0 and I1 decreases by 75%

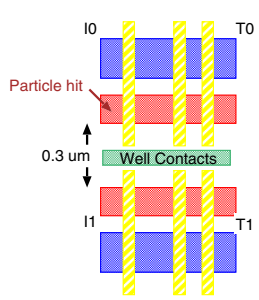


Fig. 18. Well contacts are placed between redundant latches.

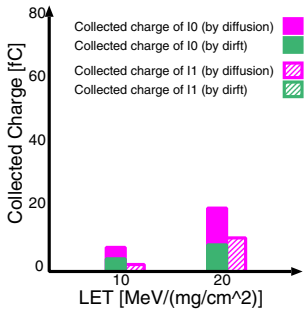


Fig. 19. Collected charge when well contacts are placed in the middle of latches

TABLE I

PARAMETERS FOR SER ESTIMATION

F ($cm^{-2}s^{-1}$)	5.65e-3
Q_s (fC)	5.72
K	2.2e-5

TABLE II

QCRIT AND MCU RATES FROM DEVICE SIMULATIONS.

	Structure	D	Q_{crit}	MCU rates
(a)	Triple well, D_{WC} = 2.75	0	9.1 fC	15.40 FIT/Mbit
(b)	Twin well, D_{WC} = 2.75	0	12.8 fC	8.07 FIT/Mbit
(c)	Triple well, D_{WC} = 2.75	0.5	–	0
(d)	Triple well, D_{WC} = 0.25	0	12.3 fC	8.81 FIT/Mbit
(e)	Middle well contacts Fig. 18	0	–	0

compared to the Fig. 11(a). In this case, generated charge under the latch L0 can not cross the well contacts to the L1 side. Thus the charge sharing between L0 and L1 is almost prevented. Also the bipolar effects is suppressed effectively, because the well contacts suppress the well potential elevation. There is no MCU occurrence in this case. According to the results of neutron-experiments[5], MCUs rates are reduced when the well contacts are placed between latches. However, the well potential is fixed in this layout structure. This kind of structure can not be used if the well potential is changed to mitigate variations or to control performance.

D. Soft Error Rate Calculation

Eq. (1) [6] is used to calculate SER in FIT (Failure In Time, error number/10^{10} s).

$$N_{\mathrm{SER}}(Q_{\mathrm{crit}}) \quad = \quad F \times A \times K \times \exp\left(-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}\right) \qquad (1)$$

where F is the high-energy neutron flux and A is the drain area of transistors related to soft errors. K is a fitting parameter. Q_s is called "charge collection efficiency" that strongly depends on doping and supply voltage[7]. We use the parameter values as in Table I that are scaled from 100 nm[6] to 65-nm.

MCU rates of all presented structure are calculated by the critical (minimum) charge which two latches flipped at the same time as shown in Table II. D_{WC} is the distance between the redundant latches and well contacts as in Fig.2. According to the results of device simulations, there is no MCU occurrence in these two kinds of device models. One is to place two latches in two rows with 0.5 μm horizontal offset (Table II (c)). The other is to place the well contacts between two latches (Table II (e)). When D_{WC} is decreased from 2.75 μm (Table II (a)) to 0.25 μm (Table II (d)), the MCU rate is decreased by 50%.

IV. Conclusion

Based on the results of device simulations, we show that charge sharing and bipolar effect are two main factors when SEUs or MCUs occur in two redundant latches. MCUs are suppressed when the distance between these latches is increased to 0.5 μm by shifting the latches. Collected charge in twin-well structure decreases 50% compared to the triple-well structure. The tolerance of former to MCUs is stronger than latter when the particle energy is lower than 20 LET. The bipolar transistors under tristate inverters become easier to turn on by increasing the p-well potential in triple-well structure. Output of the latch L1 is hard to upset by parasitic bipolar effects which decreases the MCU rates. Total charge collected by L1 and L0 decreases by 50% to placed the well contacts adjacent to the latches. The MCU rates decrease about 2 times. Total collected charge is decreased by 75% and the MCU rates decrease to 0, when the well contacts are placed in the middle of two redundant latches.

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