Parasitic Bipolar Effects on Soft Errors to Prevent Simultaneous Flips of Redundant Flip-Flops

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Abstract— **Parasitic bipolar effects are intentionally used to prevent a simultaneous flip of redundant FFs, which make them more fault-resilient to soft errors. Device simulations reveal that a simultaneous flip of redundant latches is suppressed by storing the opposite values instead of storing the same value due to its asymmetrical structure. The state of latches always becomes a specific value after a particle hit due to the bipolar effects. Spallation neutron irradiation proves that no MCU is observed in the D-FF arrays in which the stored values of latches are equivalent to the specific value. The redundant latch structure storing the opposite values is robust to the simultaneous flip.**

I. Introduction

Various redundant flip-flop structures are proposed such as TMR, DICE[1] and BISER[2] to mitigate soft errors, However, aggressive process scaling makes the probability of multiple cell upsets (MCUs) greater. MCUs are one of critical issues to diminish soft-error resilience of rad-hard designs because these designs are very sensitive to simultaneous flips. Parasitic bipolar effect plays an important role on soft errors in a current deep-submicron process[3]. If a particle hit on a transistor, adjacent transistors are affected by parasitic bipolar effects, which results in an MCU of redundant components. In this paper, we show that two latches storing the opposite values do not flip simultaneously due to the parasitic bipolar effect. The latch is composed of a inverter and a tristate inverter. When a particle hit near the latch, the parasitic bipolar transistors turn on in the inverter and the tristate inverter. Both output values becomes equivalent. But the output of the inverter is changed faster than that of the tristate inverter. Thus the state of the latch becomes a specific value after a particle hit.

This paper is organized as follows. Section II explains the redundant latch structure to prevent the simultaneous flip. In Section III, device-level simulations investigate the simultaneous flip of redundant latches in detail. Section IV shows the experimental results by spallation neutron irradiation of a D-FF array. Finally, we conclude this paper in Section V.

II. Redundant Latch Structure to Prevent MCUs

When a neutron hits to an Si atom, generated carriers elevate well potential. Then parasitic bipolar transistors are turning on. SRAMs in the triple-well has 3.5x higher probability of MCUs compared to twin-well in a 65-nm process by neutron irradiation[4]. Due to these bipolar effects, adjacent transistors are affected, which results in simultaneous upsets of latches. These simultaneous upsets diminish the error resilience of redundant latchs. But it is possible to eliminate simultaneous upsets from soft errors by enhancing circuit structures which utilizes these bipolar effects.

Fig. 1 shows a conventional latch structure. Fig. 3 shows two circuit level simulation results[5] when generated charge (Q) is 10 fC and 20 fC respectively when a particle hit on the NMOS transistor of I0 in Fig. 1. If generated charge is more than the critical charge, the latch is upset as in Fig. 3(left). Thus the latch is always upset by a particle hit with higher energy without considering parasitic bipolar effects. On the

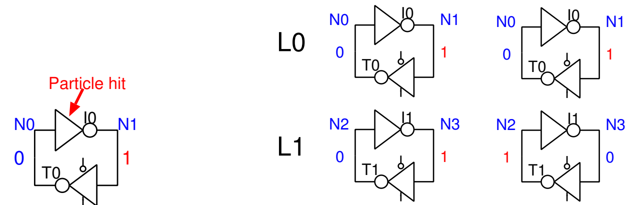


Fig. 1. Conventional latch circuit.

(a) Store the same value (b) Store opposite values

Fig. 2. Two redundant latch structures.

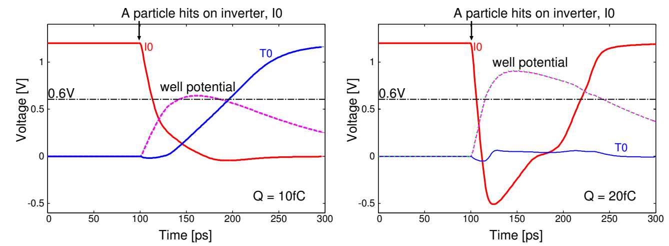


Fig. 3. Circuit-level transient simulation by hit on I0 in Fig. 1 with Q=10 fC (left) and Q=20 fC (right).

other hand, if generated charge is large enough to elevate well potential above a certain level, the latch is not upset because of the parasitic bipolar effect as in Fig. 3(right). In this case, the output values of the inverter and the tristate inverter become around 0 V at the same time just after the particle hit. But when the well potential falls to a certain level at which the bipolar transistors turn off, the output of the inverter always goes back to its original state of 1.2 V. It is because the delay time of the inverter is faster than the tristate inverter. By utilizing these parasitic bipolar effects. It is possible to enforce redundant flip-flops to soft errors.

Fig. 2(a) shows a pair of redundant latches which store the same value in conventional redundant FFs such as TMR or BISER, while Fig. 2(b) shows of those storing the opposite values in the BCDMR FF[6] as shown in Fig.4. In the BCDMR FF, two latches (ML0+ML1 or SL0+SL1) and a keeper (KM or KS) construct a triple-modular redudancy (TMR). In order to eliminate a simulaneous flip among these

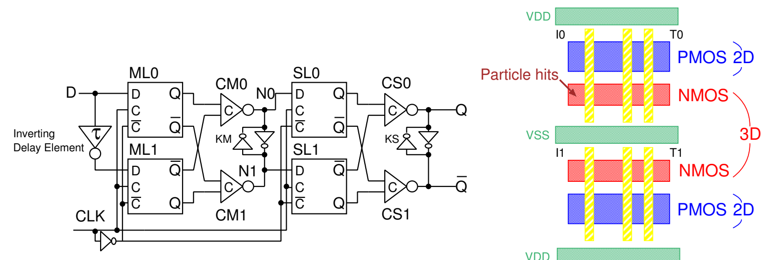


Fig. 4. BCDMR FF

Fig. 5. Two latches placed in two rows (DHC).

TMR components, these two latches are placed in two rows as shown in Fig. 5, which structure is called the double-height cell structure[7]. The keeper is in the same row as one of two latches but it is placed as far apart as possible[8] from the latch. The double-height cell structure sharing NMOS regions is very robust to soft errors on PMOS regions. However, it is very weak to soft errors on NMOS regions. If both redundant latches stores the same value as in Fig. 2(a), they can be upset at the same time by a particle hit. It is because the parasitic bipolar effects change the latches to the same value. On the other hand, if both latches store the opposite values, a particle hit with large amount of charge may change the latchs to the same value. At least one of two latchs is in the original state when they stores the opposite values. The output of the redundant FF is not flipped. Thus the possibility of the simultaneous flip can be drastically reduced when both latches stores the opposite values.

III. Device-Level Simulation Results

A. Simulation setup

Fig. 5 shows the layout structure of two latches placed in two rows sharing the NMOS region in the p-well. Fig. 6 depicts the mixed-mode device-simulation model in which the 2D PMOS and 3D NMOS device-level models are connected by wires in the circuit-level. The well contact is placed at 2.75 μm from T0 and T1. The distance between I0 (T0) and I1 (T1) is 0.3 μm. The area of the p-well is 10 μm x 10 μm. All device-level structures are constructed in the triple-well.

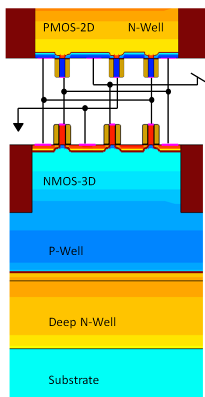


Fig. 6. Mixed-mode device-simulation model of two redundant latches (PMOS in 2D /NMOS in 3D).

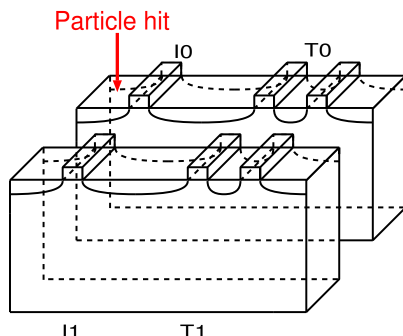


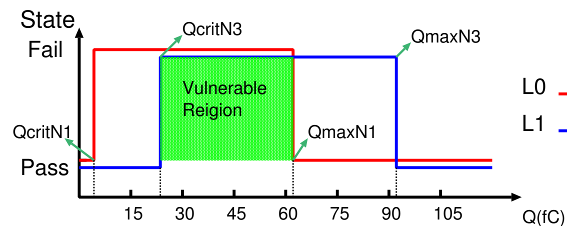
Fig. 7. A perpendicular particle hit on NMOS of I0.

B. Perpendicular particle hit

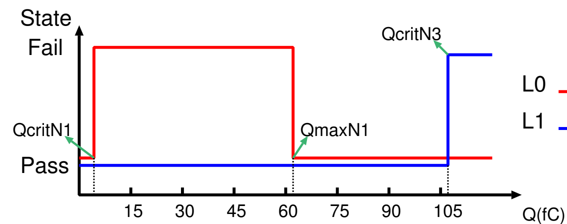
When a particle hit on the NMOS transistor of I0 perpendicularly as shown in Fig. 7, the upper latch (L0 in Fig. 2(a)) is affected by the collected charge and the bipolar effect while the lower latch (L1) is mainly affected by the bipolar effect.

Fig. 8(a) and Fig. 8(b) represent the states of the pair of two latches according to the charge "Q" collected to the node N1 and N3 in which latches stores the same value as shown in Fig. 2(a) and opposite values as shown in Fig. 2(b), respectively. The values of "Q", $Q_{\mathrm{crit}N_x}$, $Q_{\mathrm{max}N_x}$ denote the collected charge "Q" when latches is flipped and goes back to its original state by the parasitic bipolar effect, respectively.

When two redundant latches store the same value, they are flipped at the same time by "Q" between $Q_{\mathrm{crit}N_3}$ and

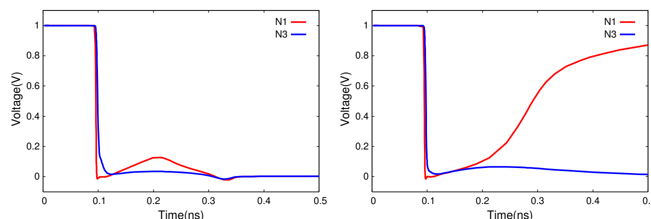


(a) Store the same value



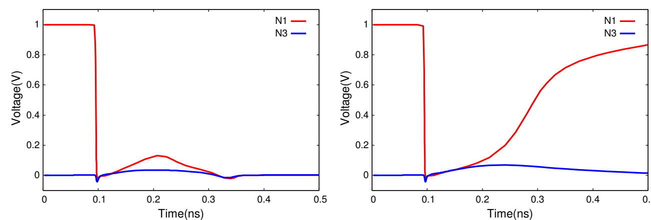
(b) Store opposite values

Fig. 8. States of N1 and N3 by a perpendicular particle hit according to the charge "Q".



(a) Q=30 fC (b) Q=80 fC

Fig. 9. State of N1 and N3 vs. Q in structure that storing the same value



(a) Q=30 fC (b) Q=80 fC

Fig. 10. State of N1 and N3 vs. Q in structure that storing opposite values.

$Q_{\mathrm{max}N_1}$ as shown in Fig. 3(left). The inverter I0 goes back to its original state and the tristate inverter T0 does not flip at the "Q" above the $Q_{\mathrm{max}N_x}$ by the parasitic bipolar effect as shown in Fig. 3(right). A vulnerable region exists between $Q_{\mathrm{crit}N_3}$ and $Q_{\mathrm{max}N_1}$ as in Fig. 8(a) when storing the same value. On the other hand, when they store the opposite values, they are not flipped at the same time as shown in Fig. 8(b). In that case, T1 is vulnerable, but the charge "Q" is much more than I0 because of its poor durability. Therefore, there is no region in which both redundant latches are flipped at the same time. Fig. 9(a) and 9(b) show transient voltage waveforms obtained from device-level simulations of particle hits with collected charge Q=30 fC and 80 fC in which the latches storing the same value. The node N1 flips at Q=30 fC but goes back to its original state at Q=80 fC. The node N3 flips in the both cases. On the other hand, Fig. 10(a) and 10(b) show transient voltage waveforms obtained when the collected charge Q=30 fC and 80 fC in which the latches storing the opposite values. The node N3 does not flip in both cases. No simultaneous flips are observed.

C. Angular particle hits

In the perpendicular particle hit in the previous section, one of two latches is affected by the both of collected charge and the bipolar effect, while the other is mainly affected by the bipolar effect. We investigate the vulnerability of two redundant latches by changing the angles of particle hits as in Fig. 11.

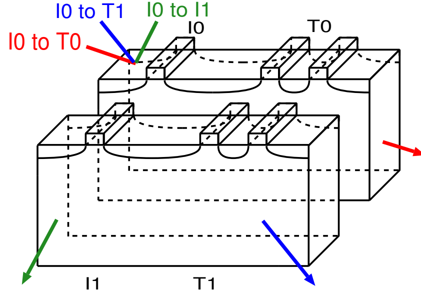


Fig. 11. Diagonal particle hits on I0 to I1, T1 and T0.

The angles of particle hits are set to 30 degree in all three cases. Fig. 12(a)-12(c) show the results when the two latches store the same value. In the case of I0 to I1, the vulnerable region becomes wider mainly due to lower Q_{critN3}. Since the diagonal hits promote the parasitic bipolar on I1, Q_{critN3} becomes lower. This is the weakest case when storing the same value. However, the vulnerable region becomes narrower when a particle passes from I0 to T1. It is mainly due to lower Q_{maxN1}. The bipolar transistor on T0 turns on by a lower-energy particle because it passes much closer to T0. When a particle passes I0 to T0, there is no vulnerable region because of lower Q_{maxN1} and higher Q_{critN3}. On the other hand, there is no vulnerable region in the structure storing the opposite values in any particle direction. Table. I and II summarises the detail LET values of N1 and N3 in both cases of the perpendicular and diagonal particle hits.

TABLE I
COLLECTED CHARGE "Q" (FC) IN THE LATCHES WHICH STORING THE SAME VALUE.

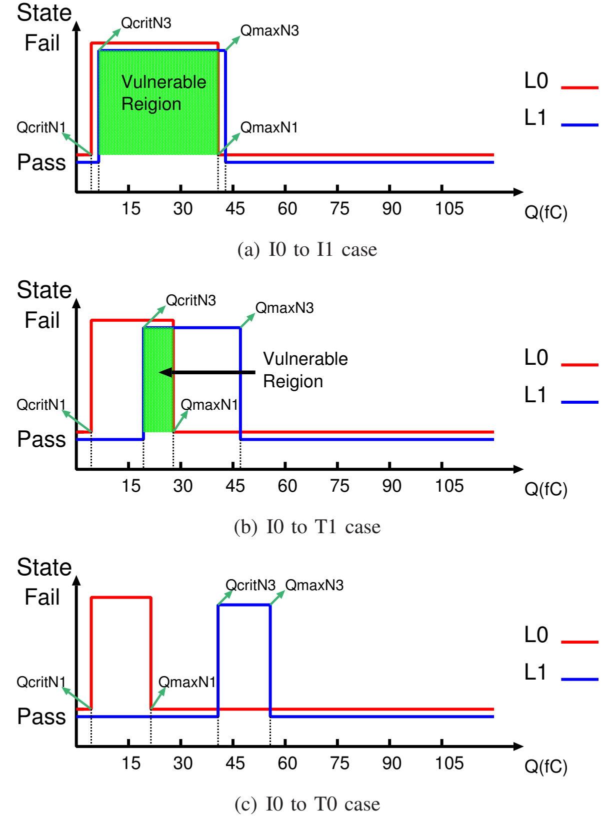
	Q_{critN1}	Q_{maxN1}	Q_{critN3}	Q_{maxN3}
Perpendicular	5.2	62.0	22.5	93.6
I0 to I1	5.2	41.8	5.5	44.0
I0 to T1	5.2	29.0	18.4	46.6
I0 to T0	5.2	22.6	40.8	53.0

TABLE II
COLLECTED CHARGE "Q" (FC) IN THE LATCHES WHICH STORING OPPOSITE VALUES.

	Q_{critN1}	Q_{maxN1}	Q_{critN3}
Perpendicular	5.2	62.0	101.1
I0 to I1	5.2	41.8	57.5
I0 to T1	5.2	29.0	69.7
I0 to T0	5.2	22.6	79.5

IV. Experimental Results by Neutron Irradiation

A test chip was fabricated in a 65 nm bulk CMOS process including a general D-FF array to show vulnerabilities of FFs by the parasitic bipolar effect. Fig. 13 show the layout structure of the FF array[9] which consists of a D-FF in Fig. 14. Spallation neutron-beam irradiation were carried out at RCNP of Osaka University. Clock is fixed to 0 or 1 to keep master or slave latches in the latch state. Table. III shows



(a) I0 to I1 case

(b) I0 to T1 case

(c) I0 to T0 case

Fig. 12. State of N1 and N3 according to collected charge "Q" when a particle hit diagonally on two latches which store the same value.

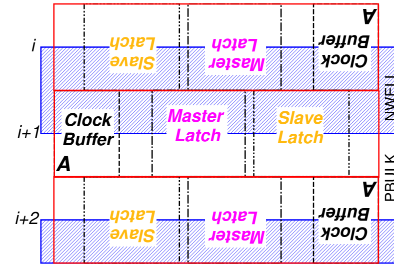


Fig. 13. Floor plan of the general D-FF array to measure MCU/SEU rates.

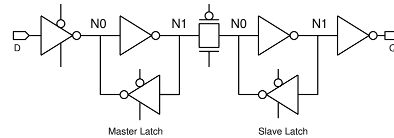


Fig. 14. Schematic of D-FF.

the numbers of SEUs and MCUs according to the state of the master and slave latches. As for the number SEUs, the latch with N1=1 is less sensitive. It is because a particle hit with higher energy does not flip N1 in the same way as explained by Fig. 3. MCUs are observed when N1=0. The MCU rates are 16.2% and 3.9% on the master and slave latches respectively. But no MCU is observed when N1=1. When N1=1, the parasitic bipolar effect suppresses a flip of latches. But SEUs are caused by collected charge without any bipolar effect. When N1=0, the bipolar effect changes the state of latches to N1=1 since the delay time of the inverter is faster than that of the tristate inverter as explained in Section II.

TABLE III

SEUs AND MCUs RATES ON FFs ACCORDING TO STORED VALUES IN MASTER OR SLAVE LATCHES BY NEUTRON IRRADIATION[?].

Vulnerable Latch	State of N1	# of SEUs (n/Mb/h)	# of MCUs (n/Mb/h)	#SEU/ #MCU
Master (CLK=1)	0	541	88	16.2%
	1	222	0	0.0%
Slave (CLK=0)	0	493	19	3.9%
	1	112	0	0.0%

V. **Conclusion**

We show that two redundant latches storing the opposite values are not flipped at the same time due to the parasitic bipolar effect. On the other hand, redundant latches storing the same value are very sensitive to MCUs. From device-level simulations, both latches storing the same value are flipped between a certain range of the particle energy which is called a vulnerable region. Because of the asymmetric structure, latches become a specific state when the parasitic bipolar transistors turn on by a particle hit. When storing the opposite values in two latches, both latches become the same state by a particle hit. But it does not change the output of the redundant FFs because one of these two latches stores the correct value. Experimental results on a D-FF array fabricated in a 65- nm CMOS prove that no MCU is observed when latches are in the specific state due to the parasitic bipolar effects. The parasitic bipolar effect is one of dominant factors of MCUs to decrease the reliability of redundant FFs. But the simple circuit-level technique of storing the opposite values enhances the tolerance to MCUs without any area, power or delay overhead.

Acknowledgment: The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.

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