Evaluation of Parasitic Bipolar Effects on Neutron-Induced SET Rates for Logic Gates

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***Abstract*— We measure neutron-induced SET (Single Event Transient) pulse width distributions from inverter chains with four drive strengths in a 65-nm CMOS process. The SET rates on 16x inverters are 17% and 38% of those on 1x in the twin- and triple-well structures respectively. Our measured results are in line with circuit simulation results that account for bipolar amplification. For higher SET mitigation, clock buffers could be placed adjacent to tap cells to reduce the number of SET pulses caused by the parasitic bipolar effect.**

I. Introduction

According to process scaling and higher clock frequency, SEU (Single Event Upset), SET, and MCU (Multiple Cell Upset) become significant issues for LSI reliability[1]. Parasitic bipolar effect is considered as one source of MCU. It is caused by well-potential perturbation due to a particle hit[2]. It also affects SET rates on logic gates and SET pulse widths[3]. It is important to estimate SET rates of logic gates constructed by multiple transistors since the parasitic bipolar effect can flip outputs of multiple logic gates.

In this paper, we measure pulse width distributions of neutron-induced SETs from inverters with four different drive strengths. To measure SET pulse widths, we propose a measurement circuit which achieves wide range and fine resolution with smaller area than conventional circuits. We calculate SET rates using circuit-level simulations considering the parasitic bipolar effect and investigate SET rates on inverters from experiments and simulation results.

The rest of this paper is organized as follows. Section II explains the proposed circuit structure in detail. Section III shows our neutron-beam experimental setup in RCNP, followed by Section IV which discusses experimental results. Section V shows simulation results and compare them with experimental results. Section VI concludes this paper.

II. SET Pulse Width Measurement Circuit

A. Conventional SET Pulse Width Measurement Circuits

Fig. 1 shows a conventional SET pulse width measurement circuit proposed by [4]. The target circuit consists of a long inverter chain and the capturing circuit consists of a D-latch chain and an SR-latch. If a particle hits on the target circuit and a SET is injected, it propagates to the D-latch chain. The SR-latch detects the SET pulse and then D-latch chain turns to be in the hold state. Therefore, the SET pulse width can be computed by the number of flipped D-latches and delay time of them. In that structure, measurable range of SET pulse widths linearly depends on the number of D-latches. Since the propagation delay is reduced by process scaling, the number of D-latches increases to keep equivalent measurable range in an advanced process. Longer the SET pulse is, more D-latches must be required. Therefore, compared with the target circuit, circuit area of D-latches becomes relatively-large according to process scaling.

Nakamura proposes another SET pulse structure[5] to reduce the pulse shrinking effect caused by the long inverter chain. But its measurement granularity is too coarse. We have proposed another circuit structure by using the pulse shrinking effect[6]. It achieves good accuracy and wide-ranged pulse capturing. But its area penalty is huge because of its structure connecting the target and capturing circuit in parallel.

B. Proposed Area-efficient SET Pulse Width Measurement Circuit

Fig. 2 shows the proposed circuit structure to measure SET pulse widths. It contains a target circuit and a capturing circuit composed of several logic gates, an FF, a 7-stage ring oscillator and a counter. Prior to irradiation, the output of the target is lowered and the FF is reset. If an SET is injected from the target, the NOR gate is activated and the ring oscillator keeps on oscillating while the SET pulse is injected. The SET pulse width can be computed by the number of oscillation stored in the counter and the states of the latches. The latches hold each output value of the logic gates in the oscillator immediately when it stops. A SET pulse is injected to the latches as a single clock signal and the latches hold input values when a clock signal becomes low. Thus, the proposed circuit can measure SET pulse width by the resolution of each gate delay. The FF detects SET occurrence and prevents further SET capture.

In the proposed circuit structure, SET pulse width is roughly measured by the counter circuit and precisely measured by the D-latches. Its measurement range exponentially increases according to the number of bits in the counter. Therefore, the proposed circuit achieves very wide measurable range of SET pulse widths with very small circuit area overhead. Fig. 3 shows comparison of the circuit area between the conventional[4] and proposed circuit. Each circuit area is computed by summing the area of the logic gates in a 65-nm process. It includes the area of scan flip-flops which read stored values of the D-latches and the counter circuit. The circuit area of the conventional circuit linearly increases according to the measurable range, while that of the proposed circuit increases logarithmically. As the result, the proposed circuit achieves smaller area overhead than the

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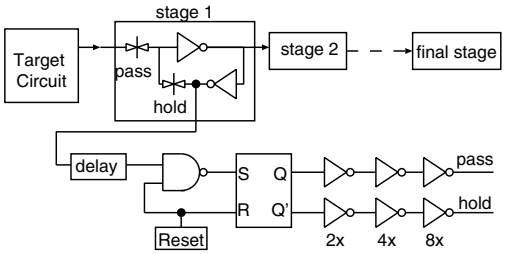

Fig. 1. Conventional SET pulse width measurement circuit[4].

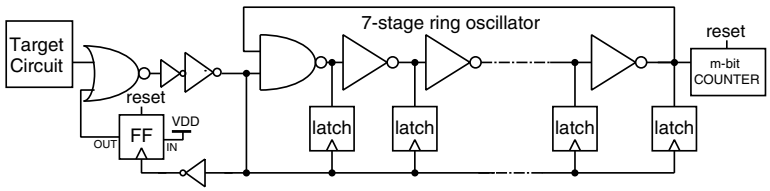

Fig. 2. Proposed SET pulse width measurement circuit.

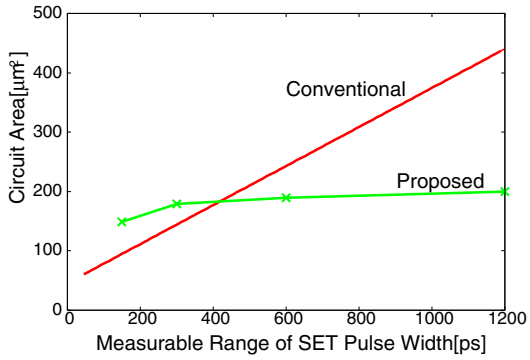

Fig. 3. Comparison of circuit area between conventional and proposed circuit in a 65-nm process.

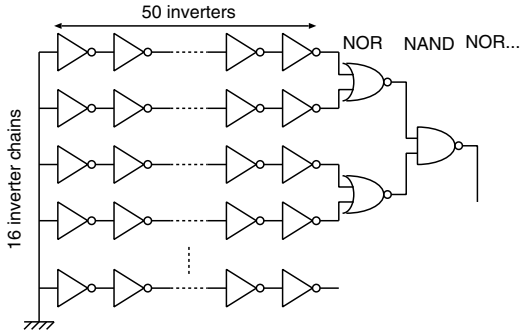

Fig. 4. Target circuit structure including 800 inverters.

conventional circuit when the measurement range is wider than 400 ps.

C. Target Circuit Structure

To accurately measure SET pulse widths, the target circuit structure is very important. It is because that when a SET is injected into the target circuit, it linearly shrinks or expands as it propagates by a propagation-induced effect[7]. Therefore, if a long inverter chain are implemented as the target circuit, measured pulse width strongly depend on where a SET is injected. Fig. 4 shows the target circuit structure based on [8]. To reduce the propagation-induced effect, it contains 16 chains composed of 50 inverters. They are connected to the capturing circuit as shown in Fig. 2 by the NOR and NAND gates tree.

III. Experimental Setup

Fig. 5 shows a test chip micrograph fabricated in a 65-nm bulk CMOS process. It includes twin-well and triple-well areas and its supply voltage is 1.2 V. It is implemented

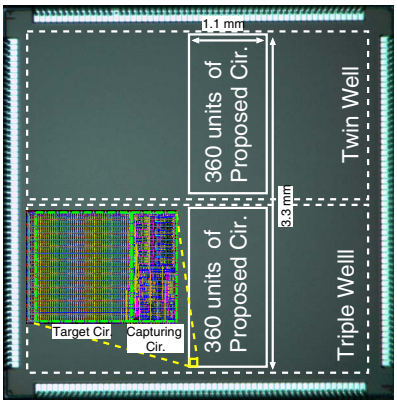

Fig. 5. Chip micrograph and floor plan.

TABLE I
STRUCTURES AND DRAIN AREAS OF INVERTERS NORMALIZED TO THAT OF 1X INVERTER.

Drive Strength	Finger		Drain Area	
	PMOS	NMOS	PMOS	NMOS
1x	1	1	1	1
2x	2	2	1.3	1.1
4x	4	4	2.5	2.2
16x	16	12	10	6

by tapless standard cells and the tap-cell interval is about 50 μm[9]. In order to measure neutron-induced SET pulse widths, 720 units of the proposed circuit are implemented with four different types of inverter chains as shown in Table I. The capturing circuit has an 8-bit counter and its circuit area is about 300 μm^2. In this test chip, another SET measurement circuit based on Ref. [10] is connected to the target circuit in order to detect SEUs on the proposed circuit. All units are implemented in a 1.1×3.3 mm^2 region on a 4×4 mm^2 die.

Accelerated tests were carried out at RCNP (Research Center for Nuclear Physics, Osaka University). The average accelerated factor is 3.8×10^8. In order to increase error counts, we measured 12 chips at the same time using stacked DUT boards. An engineering LSI tester is used to control DUTs and collect shifted error data. During irradiation, all stored values of the latches and counters were retrieved every 5 minutes.

IV. Experimental Results and Discussions

To measure the effective resolution of the proposed circuit, rectangular pulses are injected into one of the inverter chains and measure stored values of the latches and counter. They

TABLE II

SET RATES BY NEUTRON IRRADIATION.

Drive Strength	Twin-well [FIT/M inv.]	Triple-well [FIT/M inv.]
1x	19	26
2x	5.0	18
4x	11	34
16x	3.3	10

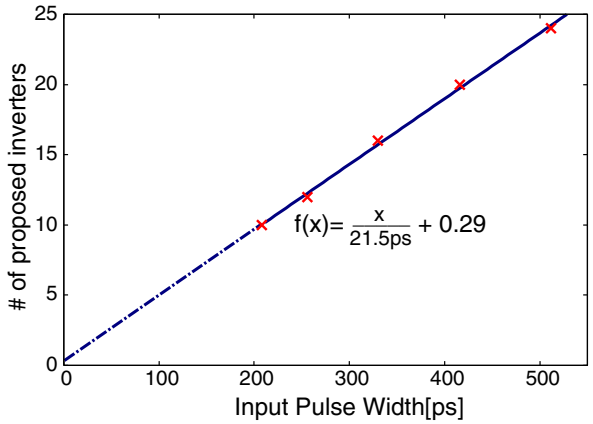

Fig. 6. Calibration result of the proposed circuit.

are generated by an embedded pulse generator constructed by a ring-oscillator and dividers. Fig. 6 shows a calibration result of the proposed circuit. Input pulse widths are calculated by frequency of the ring-oscillator. Measured results linearly increase according to the input pulse width. It reveals that the proposed circuit can measure SET pulse widths and its effective resolution is 21.5 ps, which is calculated by the slope of the fitted line. This result also shows that the pulse shrinking does not affect measurement results since the fitted line starts from the origin.

Table II shows the number of SETs on each inverter chain. The number of SETs on 16x inverters is smaller than that of other inverters but within the same order of magnitude. The SETs on 16x is 17% and 38% of those on 1x in the twin- and triple-well structure. Compared with SEU rate on FFs in a 65-nm process[11], the SET rate on 16x is about 1/50 in the triple-well structure. However, a SET on a clock tree may simultaneously flip several storage cells. Multiple flips affect chip operations with much higher probability than a single flip[12]. Therefore SETs from the clock tree is not negligible even on ordinal FFs. They become dominant if radiation-hardened clocked storage cells such as the DICE latch[13] are used.

Fig. 7 and 8 show the distributions of SET pulse widths on each inverter chain. All chains have almost similar distributions and shorter SETs have higher probability than longer SETs excluding SETs below 40 ps. Low probability of SETs below 40 ps is caused by the minimum clock pulse width of D-latches in the proposed circuit. Circuit-level simulations reveal that they cannot capture input signals below 35 ps. It is consistent with measurement results of Ref. [5] and our previous work[6].

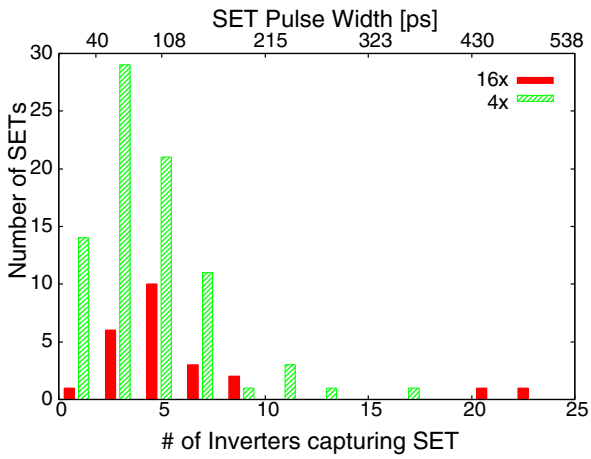

Fig. 7. Distribution of SET pulse width on 16x and 4x inverters.

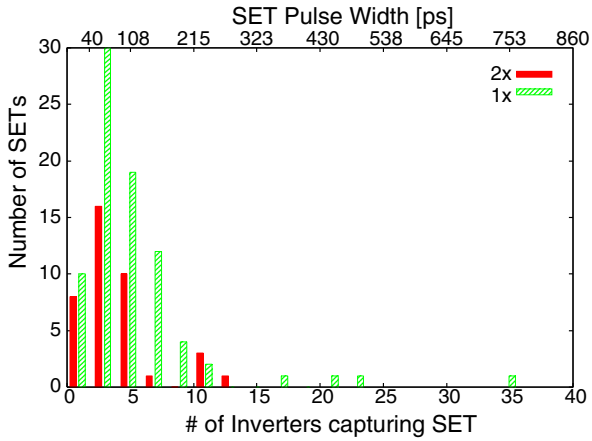

Fig. 8. Distribution of SET pulse width on 2x and 1x inverters.

V. Simulation Analysis

To analyze measurement results, we estimate SET rates on the inverter chains from circuit-level simulations. We use a single-exponential current source as shown Esq. (1) to obtain the critical charge $Q_{40\mathrm{ps}}$ which is defined as the charge to inject an SET pulse of 40 ps[14].

$$I(t) = Q\frac{2}{T\sqrt{\pi}}\sqrt{\frac{t}{T}}\exp\left(\frac{-t}{T}\right) \quad (1)$$

Then, the SET rate is computed from the empirical model in [15] as follows.

$$N_{\mathrm{SET}} = F \times A \times K \times \exp\left(-\frac{Q_{40\mathrm{ps}}}{Q_{\mathrm{s}}}\right) \quad (2)$$

F : Neutron Flux, A : Drain Area

Q_{s} : Charge Collection Efficiency

The parameter T and Q_{s} are 30 ps and 10 fC respectively obtained from [15].

Fig. 9 shows a circuit structure to obtain the $Q_{40\mathrm{ps}}$ It has two current sources, parasitic bipolar transistors, and R/C ladders for well resistance and capacitance. One current source injects current induced by drift, diffusion and funneling, while the other injects current by hole injection into the p-well. Two current sources have the same values of parameters, T and Q_{s} and they turn on simultaneously. The well resistance and the parameter β of the bipolar transistor are

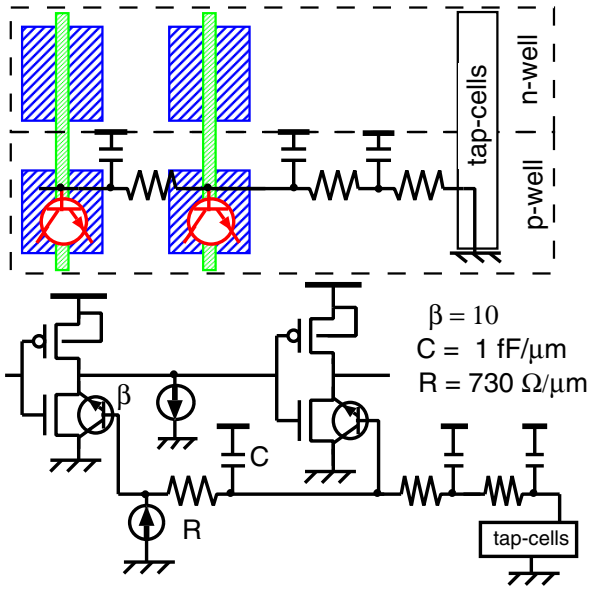

Fig. 9. Circuit structure for the circuit-level simulations with the bipolar effect.

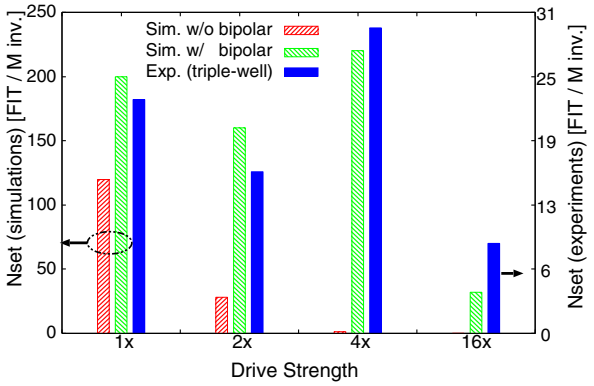

Fig. 10. Simulation results w/ and w/o parasitic bipolar effect.

730 Ω/μm and 10 respectively obtained from measurement results while well capacitance is 1 fC/μm obtained from the drain capacitance by circuit level simulations.

Fig. 10 shows simulation results. The parasitic bipolar effect increases N_{SET} and it has almost equivalent tendency to the experiment results. Simulation results clearly show that the parasitic bipolar effect must be considered to compute SETs in 65 nm. However, these simulation results strongly depend on parameter value of Q_{s}. When Q_{s} is 5 fC, SET rate on 1x inverter is 2 times bigger than that on 4x inverter.

Fig. 11 shows simulation results of SET rate on 16x inverters according to the distance from tap-cells. SET rate is drastically reduced when the distance from tap-cells is below 5 μm. In the tested 65nm bulk technology, clock inverters could be placed adjacent to the tap-cells to reduce SET pulse rates when we implement radiation-hardened FFs which have over 100x higher soft error mitigation than conventional FFs.

VI. Conclusion

We propose a SET pulse width measurement circuit based on the ring oscillator structure. It achieves smaller area overhead with wide measurement range of SET pulse widths.

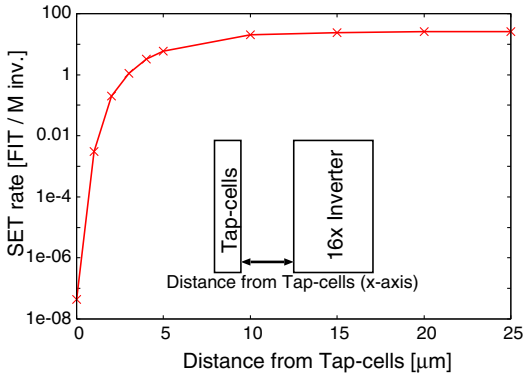

Fig. 11. Simulation result of SET rate on 16x inverters according to the distance from tap-cells.

We measure SET pulse widths of inverters with four different drive strengths. The SET rate on 16x drive strength inverters is smaller than that on 1x drive strength inverters but within the same order of magnitude. Measurement results are almost equivalent to simulation results considering the parasitic bipolar effect. In the tested 65nm bulk technology, accounting for bipolar effects is crucial to explaining the observed SET pulse width distributions. As a potential mitigation technique, we suggest placing clock inverters adjacent to tap-cells. Our simulations indicate a drastic reduction in SET upset rates for 16x inverters if this mitigation technique is applied.

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