

# The Impact of RTN on Performance Fluctuation in CMOS Logic Circuits

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**Abstract**—In this paper, the impact of Random Telegraph Noise (RTN) on CMOS logic circuits observed in a Circuit Matrix Array is reported. We discuss the behavior of RTN under circuit operation, and reveal that the impact of RTN, which is much smaller than that of within-die variation in a 65nm process, can have a severe effect on the performance of a sequential logic gate under low voltage operation.

## I. Introduction

With recent aggressive technology scaling of LSIs for power reduction and die shrink, designing reliable systems becomes more and more challenging. Besides conventional problems such as transistor leakage, degradation and variation of transistor performance have a severe impact on the dependability of VLSI systems [1], [2], [3]. Random Telegraph Noise (RTN) has attracted much attention as a temporal variation caused by the capture and emission of mobile charge carriers by defects inside the dielectric [4], [5]. It has been reported that RTN will emerge as a serious reliability and variability issue in accordance with scaling [6], [7], and even in 90nm process node RTN already has a severe impact on CMOS image sensors [8], Flash memories [9], SRAMs [10]. However, the impact of RTN on CMOS logic circuits has not been well addressed yet. Therefore, we focus on the impact of RTN on circuit delay and have measured RTN-induced delay fluctuation using a circuit matrix array fabricated in a 65nm process.

The remainder of this paper is organized as follows. In Section 2, we will show the test structure fabricated in a 65nm CMOS technology for RTN-induced delay fluctuation measurement. In Section 3, from the measurement data, we discuss RTN characteristics under circuit operation, and evaluate the impact of RTN on combinational circuits and sequential circuits quantitatively. Finally, Section 4 summarizes this paper.

## II. Test Structure for RTN-induced Delay Fluctuation Measurement

Fig. 1 shows a test structure fabricated in a 65nm CMOS technology for RTN-induced delay fluctuation measurement. The circuit matrix array contains a  $20 \times 15$  array sections and each section is constructed by a various types of ring oscillators (ROs) including a 7-stage inverter RO. We therefore have 300 identical 7-stage ROs on a chip, which we consider as representatives of combinational circuits. By measuring the fluctuation of oscillation frequencies, we can evaluate the fluctuation of delays in a chain of inverters. ROs are

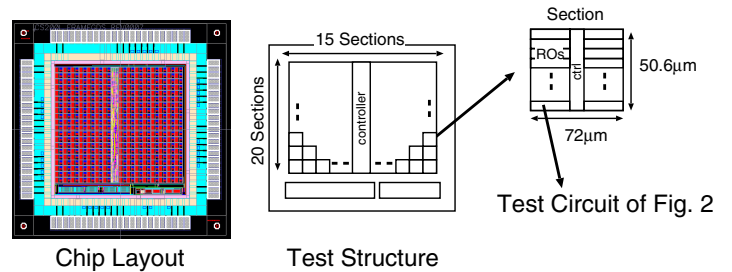


Fig. 1. A test structure for process variation and RTN-induced delay fluctuation measurement in 65nm CMOS technology

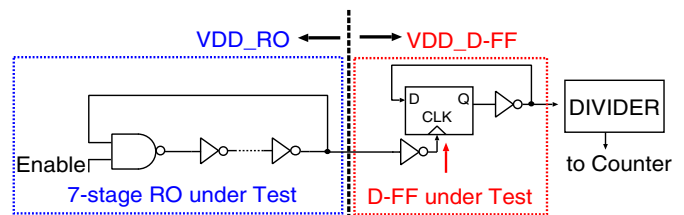


Fig. 2. A test circuit that consists of a ring oscillator (RO) and a divider with a D-FF, for evaluating the impact of process variation and RTN in a combinational circuit(RO) and a sequential circuit(D-FF).

connected to dividers as shown in Fig. 2. The frequency of an RO can be tuned by changing its supply voltage  $VDD_{RO}$ , and the output of the RO is connected to the clock input of a D-FF through one inverter so that the circuit acts as a frequency divider as shown in Fig. 2. The power supply of the D-FF ( $VDD_{D-FF}$ ) can also be varied. In this experiment, we have measured the fluctuation of oscillation frequencies for a period of 250 s by counting the number of oscillation over 20 ms at room temperature. Supply voltages  $VDD_{RO}$  and  $VDD_{D-FF}$  are set to 0.8 V and 1.0 V, respectively

## III. Experimental Results and Discussion

### A. Behavior of RTN under circuit operation

Considering the source of  $1/f$  noise is superposition of multiple RTN [4], the power spectrum density (PSD) of the oscillation frequency fluctuation of a 7-stage ring oscillator, which consists of 18 MOSFETs, is found to be well represented by an  $1/f^s$  response where the power  $s$  is between 1 and 2.

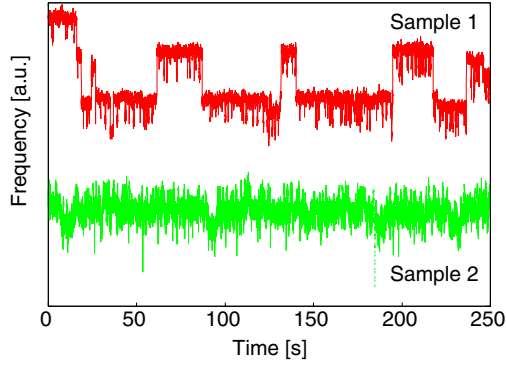


Fig. 3. Two examples of measured RTN-induced frequency fluctuations.

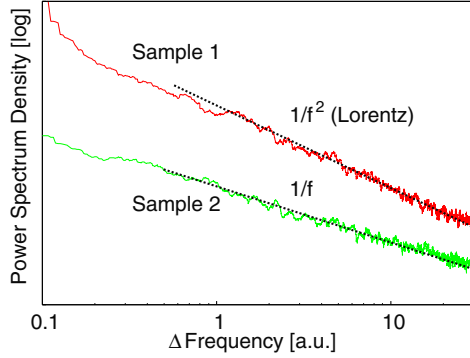


Fig. 4. PSD of RTN-induced frequency fluctuations shown in Fig. 3.

Fig. 3 shows two examples of measured frequency fluctuation observed in 300 samples. Sample 1 has a discrete fluctuation which is a characteristic of RTN while Sample 2 does not. Fig. 4 is the PSD of these frequency fluctuations. Since the PSD of Sample 1 is  $1/f^2$ -shaped and that of Sample 2 is  $1/f$ -shaped, they are both believed to be originated from RTN. The increase of  $V_{DD_{D-FF}}$  has no influence on the frequency fluctuation. This confirms that the frequency fluctuation is caused by the phase-noise of the ring oscillator due to RTN, not by any functional fluctuation of the D-FF.

The emission time  $\tau_e$  (averaged time of high  $V_{th}$  state) and the capture time  $\tau_c$  (averaged time of low  $V_{th}$  state) are also important factors of RTN. They are known to depend on trap position, trap energy and bias condition strongly (Shockley-Read-Hall statistics [4]). Considering Fermi energy level varies widely under circuit operation, there is a possibility that RTN under circuit operation behaves differently from RTN under DC bias.

Fig. 5 shows an example of measured 2-level frequency fluctuation and its idealized 2-level waveform. From the idealized 2-level fluctuation, we have measured emission times and capture times. Statistical characteristics of those intervals are listed in Fig. 6 where we can extract the time constants of  $\tau_e$  and  $\tau_c$  by exponential fitting. This suggests that RTN under circuit operation obeys similar mechanism to that under DC condition.

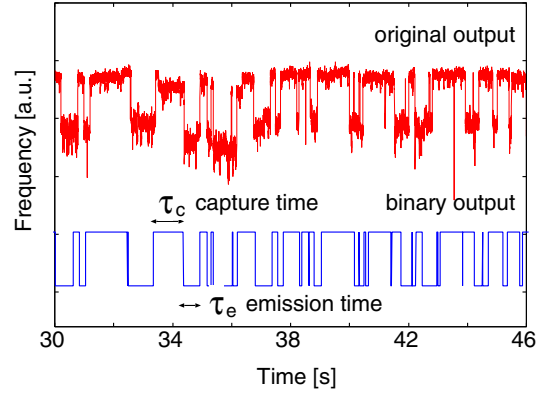


Fig. 5. A measured 2-level frequency fluctuation and its idealized RTN waveform from the noisy measurement data

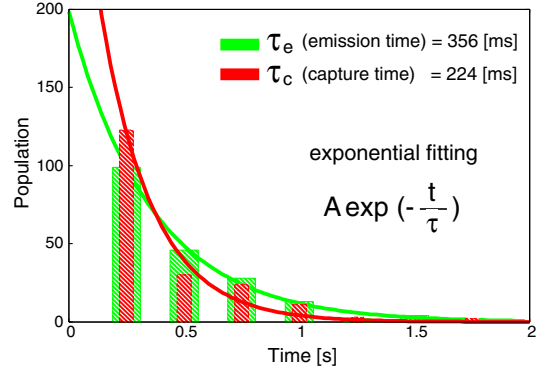


Fig. 6. Under circuit operation (AC bias),  $\tau_e$  (emission time) and  $\tau_c$  (capture time) of RTN can be uniquely extracted.

### B. Impact of RTN on delay of combinational circuits

We define the variation of averaged frequencies over measurement time of 250 s for 300 ROs on a chip as WID variation, whereas the maximum frequency shift for each RO in 250s is caused by RTN. Fig. 7 shows the distribution of frequency variation by the WID variation and the frequency fluctuation by RTN measured at  $V_{DD_{RO}} = 0.8V$  and  $V_{DD_{D-FF}} = 1.0V$ .

As shown in Fig. 7, the impact of RTN on delay is as small as 4% of that of WID variation at  $3\sigma$ . This is because RTN-induced  $\Delta V_{th}$  is much smaller than that caused by WID variation in a 65nm process for normal logic cells.

Fig. 8 shows the scatter plots of measured RTN-induced frequency fluctuation and WID variation-induced frequency variation. Frequency fluctuation by RTN appears to be uncorrelated to WID frequency variation. This indicates that RTN-induced  $\Delta V_{th}$  does not depend on the amount of  $V_{th}$ .

The distribution of RTN-induced frequency fluctuations at various  $V_{DD_{RO}}$  is shown in Fig. 9. We have observed that the ratio of RTN-induced frequency fluctuation to WID variation-induced frequency variation increases as  $V_{DD_{RO}}$  increases, as shown in Fig. 10. It has been reported that RTN-induced  $\Delta V_{th}$  or detected number of traps has  $V_{gs}$  dependence [10]. The  $V_{gs}$  dependence of the ratio in Fig. 10 confirms the  $V_{gs}$

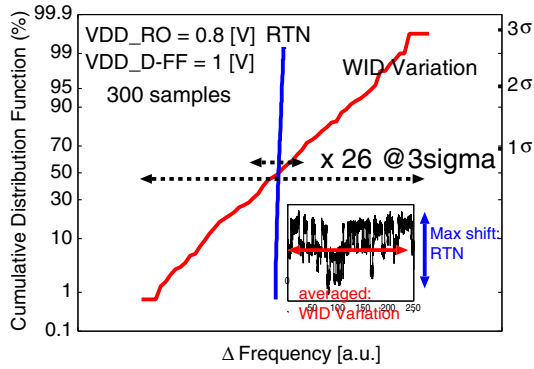


Fig. 7. Distribution of frequency variation by Within die (WID) variation and frequency fluctuation by RTN. In a 65nm logic circuit, the impact of RTN is much smaller than that of WID variation.

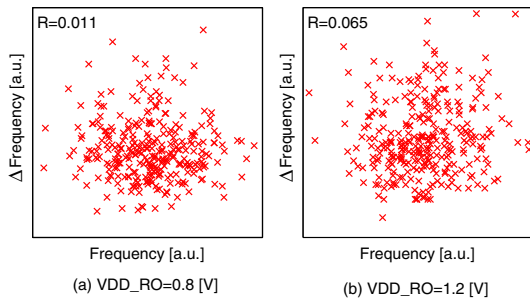


Fig. 8. Scatter plots of measured RTN-induced frequency fluctuation (“ $\Delta$  Frequency”) and WID variation-induced frequency variation (“Frequency”). “ $\Delta$  Frequency” appears to be uncorrelated with “Frequency”.

dependence of  $\Delta V_{th}$  under circuit operation.

Fig. 11 shows the estimated ratio of RTN-induced delay fluctuation to WID variation-induced delay variation which appears in a normal logic gate in future technology nodes. The ratio is derived assuming the WL dependence of WID variation ( $\sigma/\mu \propto 1/\sqrt{WL}$ ) known as Pelgrom Plot [11] and that of RTN ( $\sigma/\mu \propto 1/WL$  [7]) using the measured data at  $VDD_{RO} = 0.8V$ . This shows that in more scaled technology RTN is expected to have a non-negligible impact on the delay of combinational circuit, and RTN-aware design margin must be considered.

### C. Impact of RTN on sequential circuits

As explained in section II, a ring oscillator in the test circuit is connected to a divider. Fig. 12 shows the simulation result of the output frequency of the divider as a function of the input frequency. There exists a maximum frequency for correct operation (MOF: Maximum Operating Frequency). The MOF corresponds to a D-FF delay with an additional delay of an inverter. Under low voltage operation of the D-FF, we have observed a large frequency fluctuation at the output when the input frequency is close to the MOF, which is shown in Fig. 13. This large fluctuation comes from the failure operation of the D-FF due to the fluctuation of the MOF by RTN. The vulnerability of D-FF timing behavior[12] is triggered by RTN.

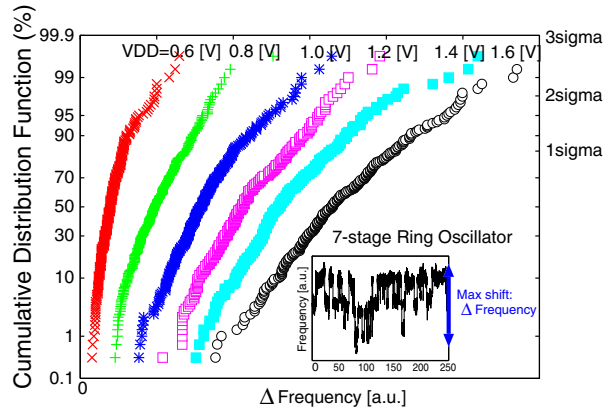


Fig. 9. Distribution of RTN-induced frequency fluctuations under various  $VDD_{RO}$ .

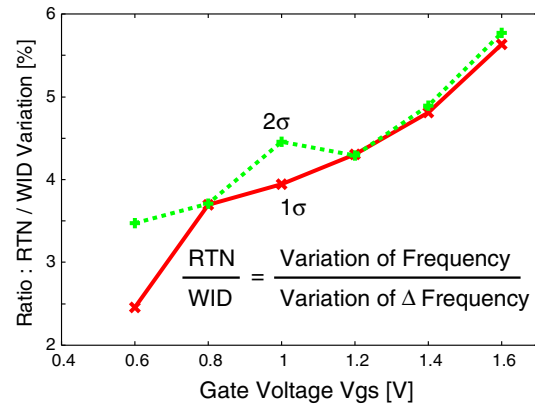


Fig. 10. The ratio of RTN-induced frequency fluctuation to WID variation-induced frequency variation as a function of  $VDD_{RO}$ .

Fig. 14 shows the comparison between the distribution of the oscillation frequency fluctuation measured at  $VDD_{RO} = 0.8 V$  and  $VDD_{D-FF} = 0.75 V$ , and the one at  $VDD_{RO} = 0.8 V$  and  $VDD_{D-FF} = 1.0 V$ . All D-FFs in 300 samples at  $VDD_{D-FF} = 1.0 V$  can divide the input frequency correctly. When  $VDD_{D-FF}$  is reduced to 0.7V, the number of D-FFs that work as a divider correctly decrease to 112 samples because 188 D-FFs stop working due to performance degradation caused by WID variability. Out of 112 working samples, however, 25 samples have exhibit a very large frequency fluctuation originated from RTN in D-FFs. This observation indicates that under low voltage operation, where PVT variation have a large impact, RTN can also have a severe impact on the functionality of a sequential logic such as a D-FF.

## IV. Conclusion

We have measured RTN-induced performance fluctuation in CMOS logic circuits using a circuit matrix array test structure. It is revealed that RTN under circuit operation has statistical properties similar to those under DC bias. The impact of RTN is much smaller than that of WID variation on combinational circuits in a 65nm process. However, we

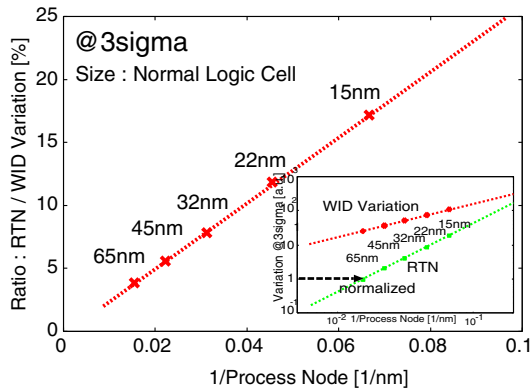


Fig. 11. Predicted comparison between RTN-induced delay fluctuation and WID variation-induced delay variation in a CMOS logic circuit. In more scaled process node, the impact of RTN will become visible on the circuit delay.

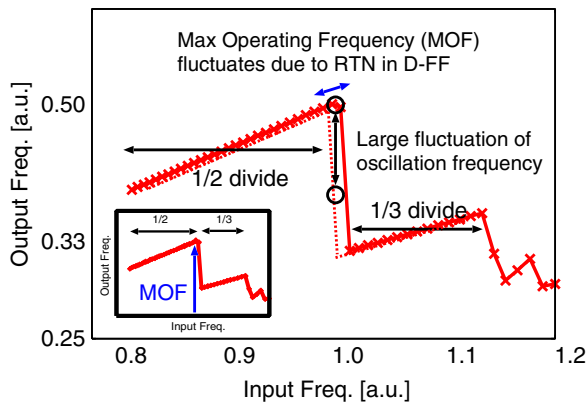


Fig. 12. Simulation result of the output frequency of the divider as a function of input frequency. Large frequency fluctuation results from Max Operating Frequency (MOF) fluctuation induced by RTN in the D-FF.

clarify that the impact of RTN on the circuit delay is expected to increase in more scaled technologies, and RTN has a severe impact on sequential circuits under low voltage operation.

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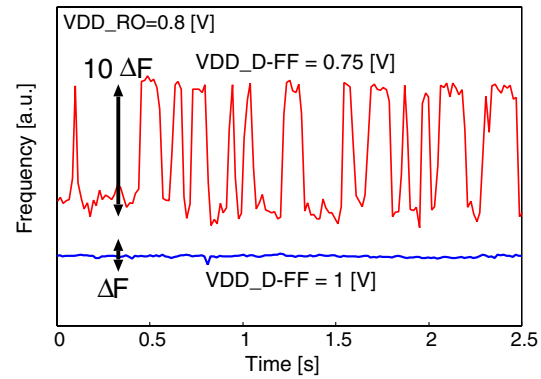


Fig. 13. Oscillation frequency fluctuation due to RTN. Fluctuation increases largely when lowering voltage of D-FF to certain point.

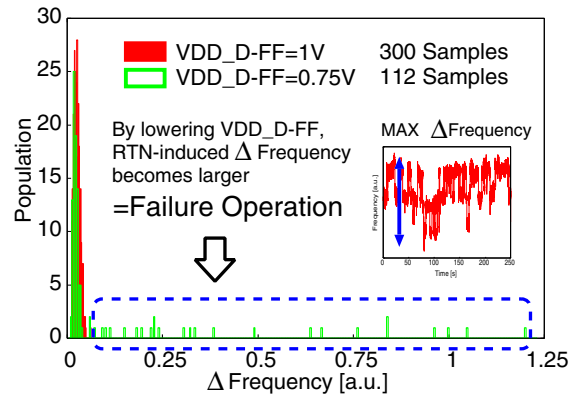


Fig. 14. Distribution of the frequency fluctuation under low  $VDD_{D-FF}$  (0.75V). Large frequency fluctuation results from MOF fluctuation due to RTN in the D-FF, as explained in Fig. 12. In low voltage, even RTN produces visible performance degradation in a sequential circuit such as a D-FF.

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