# Measurement of Neutron-induced SET Pulse Width Using Propagation-induced Pulse Shrinking

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*Abstract*— **We propose a single event transient (SET) pulse width measurement circuit using propagation-induced pulse shrinking on a clock buffer chain. It achieves the resolution of less than 1ps since the target circuit of the buffer chain is directly connected to the pulse capture FFs. Experimental results using the spallation neutron beam accelerated test show SET pulse widths are exponentially-distributed and number of SETs longer than 350 ps are reduced to 9% by inserting tap-cells closely. The SET rate on the clock buffer is 23x smaller than SEU rate on FFs.**

## I. Introduction

According to process scaling and increase in the clock frequency, not only SEU (Single Event Upset) but also SET (Single Event Transient) become more significant issues[1]. They are collectively called soft error. SEU flip a stored value on SRAMs or flip-flops (FFs), while SET generates temporal pulse on logic gates. To protect FFs from SET pulse, delay element and low-pass filter are commonly used. To optimize LSI reliability and performance, it is important to measure distribution of SET pulse widths. Previous works proposed several SET pulse width measurement circuits and reported its measurement results[2][3][4]. But, there are few measurement results of SET pulse distributions by neutron irradiation[5][6]. Previous work[5] measured neutron-induced SET pulse widths on an inverter chain using a D-latch chain. However, an SET pulse width linearly expands or shrinks as it propagates through the inverter chain[7]. SET pulse widths depend on where a pulse is injected.

In this paper, we propose a SET pulse width measurement circuit according to similar ideas to the process variability monitor[8] and the time-to-digital converter[9]. To measure SET pulse widths, it uses the propagation-induced pulse shrinking on a buffer chain and achieves the resolution of less than 1ps with no dependency where a pulse is injected. We also show accelerated test results of SET pulse widths on a 65 nm process using the proposed circuit. Accelerated tests were carried out by the spallation neutron beam at RNCP(Research Center for Nuclear Physics, Osaka University). The rest of this paper is organized as follows. Section II explains the proposed circuit design and propagation-induced pulse shrinking in detail. Section III shows our neutron-beam experimental setup in RCNP, followed by Section IV which discusses experimental results. Section V concludes this paper.

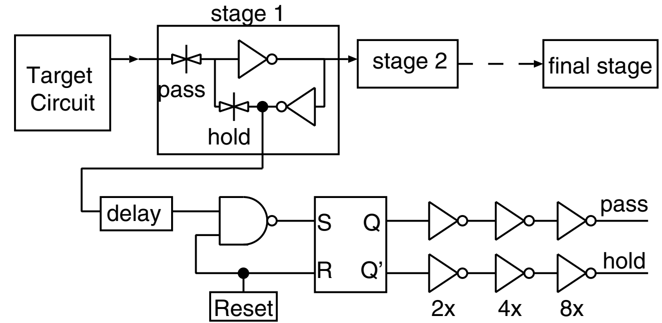


Fig. 1. Conventional SET pulse width measurement circuit[5].

## II. SET Pulse Width Measurement Circuit

### A. Conventional SET Pulse Width Measurement Circuit

Fig. 1 shows conventional SET pulse width measurement circuit proposed by Narasimham[5]. The target circuit consists of an inverter chain and the measurement circuit consists of a D-latch chain and an SR-latch. If a particle hits on the target circuit and an SET is injected, it propagates to the D-latch chain. The SR-latch detects the SET pulse and then D-latch chain turns to be in the hold state. Therefore, the SET pulse width can be computed by the number of flipped D-latches and delay time of them.

However, an SET pulse width linearly expands or shrinks as it propagates through an inverter chain, since measurement circuit is connected to target circuit in series[7]. Measurement results of the SET pulse width depend on where it is injected. Thus conventional circuit structures cannot measure pulse-width distributions accurately. It is difficult to eliminate the propagation-induced effect, since it is composed of target and capture circuits placed separately. Therefore, we propose a SET pulse width measurement circuit which explicitly utilizes the propagation-induced effect (pulse shrinking) to measure SET pulse width[9]. First, we explain propagation-induced pulse shrinking in the following section.

### B. Propagation-induced Pulse Shrinking on a Buffer Chain

As shown in Fig. 2, propagation-induced pulse shrinking is caused by the difference between the fall propagation delay, $d_{\mathrm{fall}}$ and the rise propagation delay, $d_{\mathrm{rise}}$ of each inverter along the buffer chain. They can be approximated

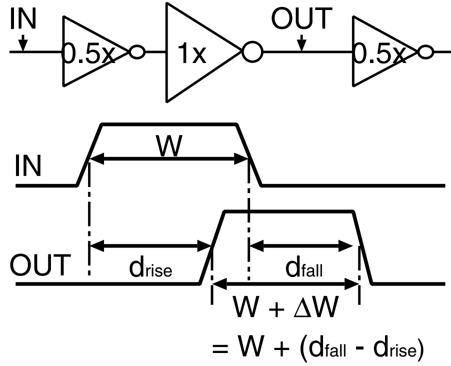


Fig. 2. Concept of propagation-induced pulse shrinking on a buffer chain.

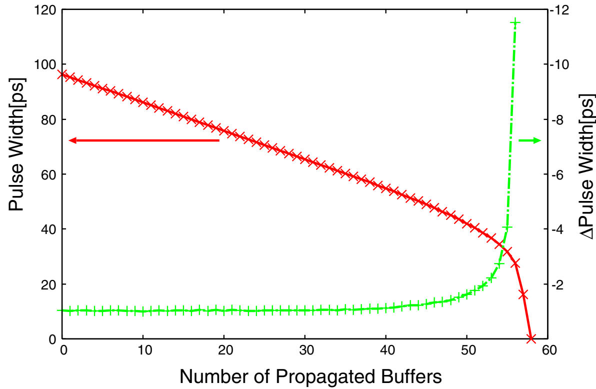


Fig. 3. Simulation result of propagation-induced pulse shrinking.

simplistically as follows[9].

$$d_{\mathrm{fall}} \approx k\left(\frac{C_{\mathrm{g}}}{0.5g_{\mathrm{mp}}}+\frac{0.5C_{\mathrm{g}}}{g_{\mathrm{mn}}}\right) \quad (1)$$

$$d_{\mathrm{rise}} \approx k\left(\frac{C_{\mathrm{g}}}{0.5g_{\mathrm{mn}}}+\frac{0.5C_{\mathrm{g}}}{g_{\mathrm{mp}}}\right) \quad (2)$$

where $g_{\mathrm{mp}}$, $g_{\mathrm{mn}}$ are the transconductance parameters of the 1x inverter, $C_{\mathrm{g}}$ is its gate capacitance and $k$ is a factor of proportionality. Then, amount of pulse width variation through a buffer, $\Delta W$ can be calculated as follow.

$$\Delta W = d_{\mathrm{fall}} - d_{\mathrm{rise}} = \frac{3}{2}kC_{\mathrm{g}}\left(\frac{1}{g_{\mathrm{mp}}}-\frac{1}{g_{\mathrm{mn}}}\right) \quad (3)$$

Therefore, $\Delta W$ can be controlled by PMOS and NMOS sizes of each inverter. If $g_{\mathrm{mp}}$ is bigger than $g_{\mathrm{mn}}$, $\Delta W$ is negative and pulse width is linearly shrunk as propagating through the inverter chain.

Fig. 3 shows a simulation result of pulse shrinking on a buffer chain. A 100 ps input pulse is linearly shrunk up to 40 ps. Then it vanishes immediately after becoming less than 40 ps. Therefore, if we can retrieve the location where SET is injected and vanishes on a buffer chain, the pulse width can be measured by pulse shrinking with the resolution of $\Delta W$.

### C. *Proposed SET Pulse Width Measurement Circuit*

Fig. 4 shows the proposed SET pulse width measurement circuit. To accurately measure SET pulse widths, each buffer output is directly connected to a clock input of an FF. All FFs

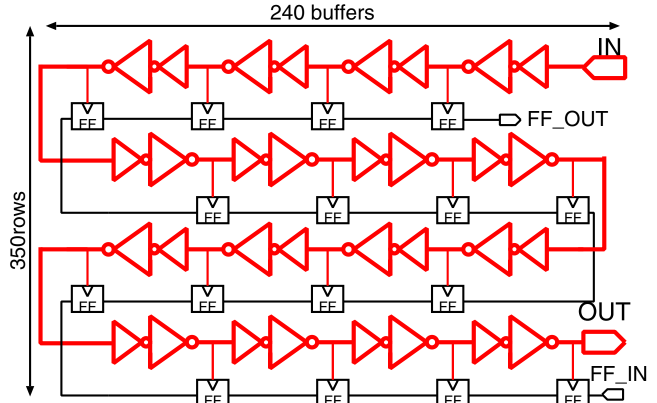


Fig. 4. Proposed SET pulse width measurement circuit.

TABLE I
COMPARISON OF CONVENTIONAL AND PROPOSED CIRCUIT.

| | conventional | proposed |
|---|---|---|
| connection to target cir. | in series | in parallel |
| influence of propagation (accuracy) | high (low) | low (high) |
| measurement method (resolution) | propagation delay (>10 ps) | pulse shrinking (< 1 ps) |
| measurement of SEU | no | yes |
| circuit size | small | big |

construct a shift register to retrieve stored values of FFs. In order to prevent malfunction of the shift register due to hold time violations, FFs are connected in the reverse direction of the buffer chain. In this structure, to detect where an SET is injected and vanishes on a buffer chain, all FFs are initialize to the stripe pattern as shown in the upper part of Fig. 5. If an SET is injected on the buffer chain, stored values of FFs are shifted from the injected point until SET vanishes as shown in the lower part of Fig. 5. The stripe pattern can detect where SET is injected and vanishes on a buffer chain and measure how many buffers SET propagated through. Therefore, SET pulse widths can be measured by the propagation-induced pulse shrinking using the proposed circuit.

Table I shows comparison of the conventional and proposed circuits. The proposed circuit is less affected by the propagation and achieves high accuracy since the measurement circuit (FFs) is directly connected to the target circuit (buffers). It also achieves high resolution of less than 1ps while that of the conventional circuit is more than 10 ps. It is because the resolution of the conventional circuit is eliminated by inverter propagation delay, while that of the proposed circuit can be changed by transistor sizes as shown Eq. (3). However, it has the drawback of bigger area than the conventional circuit. We can reduce the circuit area by changing insertion interval of FFs from every buffer to two or more buffers.

## III. **Experimental Setup**

Fig. 6 shows a chip micrograph fabricated in 65 nm bulk CMOS process. In order to measure neutron-induced SET pulse widths, the proposed circuit including 161,000 buffers and FFs is implemented in a $1.1\times1.3$ mm$^2$ region on a $2\times4$ mm$^2$ die. Tap-cells to stabilize potentials of well or bulk are

Fig. 5. Initial stripe pattern to detect an SET pulse (3bit stripe version).

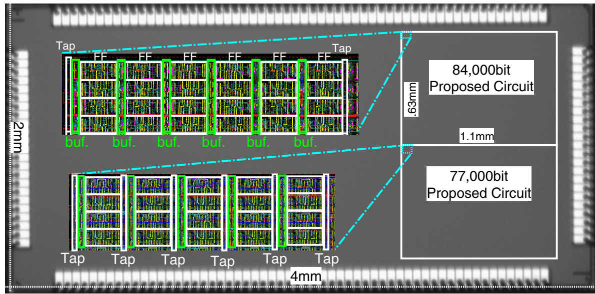


Fig. 6. Chip micrograph and partial layout structure.

inserted every 28 $\mu$m in the first 84,000 bit of the proposed circuit. On the other hand, they are inserted every 5$\mu$m during the latter 77,000 bit.

Fig. 7 shows the neutron beam spectrum compared with the terrestrial neutron spectrum at the ground level of Tokyo. The average accelerated factor is $3.8 \times 10^8$ in this measurement. We used 5-stacked DUT boards to increase error counts. Each DUT board has four segments, each of which is equipped with a single DUT. Note that input signals are common for every segment, while output signals are independent for 5 DUTs to minimize time for the shift operation. In this measurement, 18 DUTs out of 20 are fully functional. Fig. 8 depicts the neutron-beam opening and the stacked DUT boards. An engineering LSI tester is used to control DUTs and collect shifted error data.

During irradiation, input of the buffer chain is fixed to 1. Since the proposed circuit has no self-trigger circuit to detect SET, we must frequently retrieve stored values of FFs. In this measurement, stored values of all FFs were retrieved every 5 minutes. After finishing retrieving (shifting), all FFs are restored to the initial state of the stripe pattern. Note that we initialize FFs to 20 bit stripe pattern in this measurement.

## IV. Experimental Results and Discussions

### A. Effective Resolution of the Proposed Circuit

In order to accurately measure SET pulse widths, we must measure the effective resolution ($\Delta W$ as shown eq. (3)) of the proposed circuit. To calibrate effective resolution of

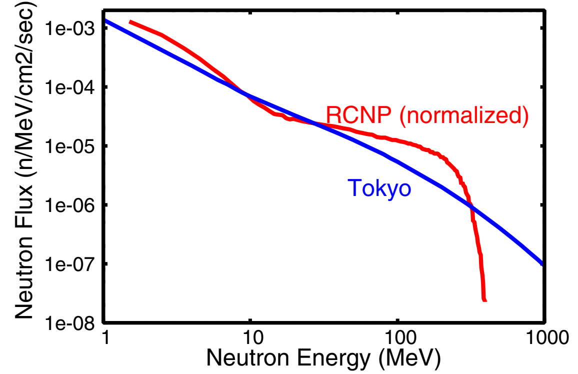


Fig. 7. Neutron spectrum at RCNP.

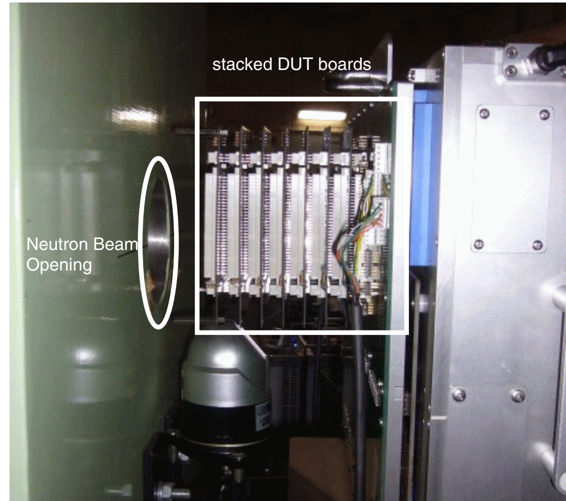


Fig. 8. Neutron-beam opening and stacked DUT boards.

the proposed circuit, rectangular pulses are injected into the buffer chain. Fig. 9 shows the relationship between the input pulse width and the number of shifted FFs from 3 DUTs. These measurement results are average results of 20 times measurement and each point has about $\pm 5\%$ margin of error. All DUTs have linear dependence between input pulse width and number of FFs. In this result, slopes are different by the tap-cell interval. We assume that it is caused by difference of well resistance.

Fig. 10 shows effective resolutions calculated by the slopes. Effective resolutions are different for each DUT. We expect that it is caused by die-to-die variations. Table II shows simulation results of effective resolutions in corner models. There are big difference between each corner especially SF and FS. It is because that effective resolution, $\Delta W$ is determined by difference in transconductances of PMOS and NMOS as shown Eq. (3).

TABLE II
SIMULATION RESULTS OF EFFECTIVE RESOLUTION IN A CORNER MODEL.

| corner model | SS | TT | FF | SF | FS |
|---|---|---|---|---|---|
| resolution | $-1.2$ ps | $-0.60$ ps | $-0.89$ ps | $-3.0$ ps | 1.1 ps |

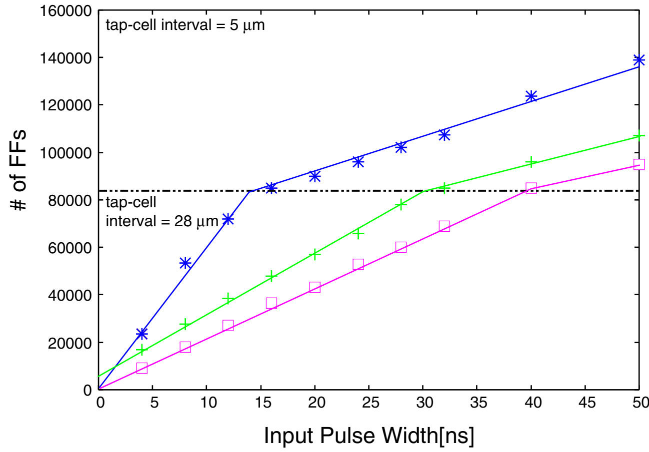

Fig. 9. Calibration results of 3 DUTs.

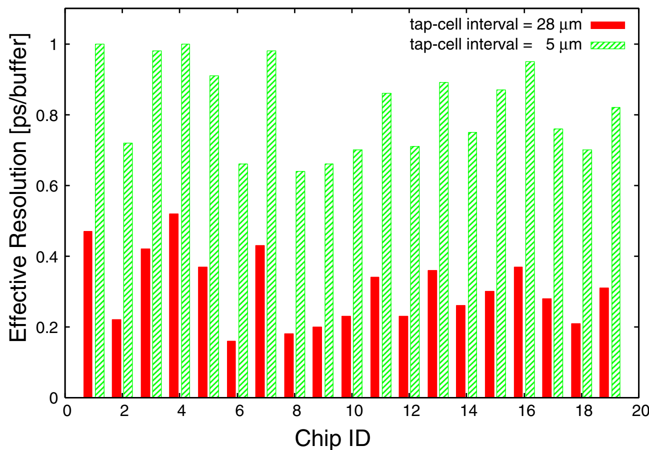

Fig. 10. Effective resolutions of 18 DUTs

### B. Measurement Result of SET Pulse Widths

Fig. 11 shows distribution of SET pulse widths and Table III shows total number of SETs and average pulse widths. Fig. 12 shows a stripe pattern affected by an SET pulse and SEUs. Note that SET pulse vanishes immediately after becoming less than 40 ps in the simulation as shown in Fig. 3. However, this measurement results do not consider this immediate disappearance. SET pulse widths are just calculated by number of FFs shifted by SET and the effective resolutions as shown Fig. 10. In this measurement, shorter SETs have higher probability, which is similar to [6]. SET pulse widths are reduced by inserting tap-cell closely and number of SETs longer than 350 ps is reduced to 9%. This result is similar to [10] and suggests that SET pulse widths are increased by the parasitic bipolar effect. Fig. 13 shows shows distribution of SET pulse widths in a log scale. SET pulse widths on the buffer chain inserted tap-cell every 5 $\mu$m are exponentially-distributed, and SET pulse widths up to 350 ps on the buffer chain inserted tap-cell every 28 $\mu$m are also exponentially-distributed. We assume parasitic bipolar effects prolong the pulse width over 350 ps in the case of the every-28 $\mu$m tap-cell insertion.

In this measurement, multiple SETs (MSETs) can be observed in different regions because the proposed circuit has 161,000 buffers and FFs to capture SETs. In addition, we also observed SEMTs(Single Event Multiple Transient) which indicate two or more SETs are caused by a single particle hit. Table IV shows total number of SET, MSET and SEMT. We regard two SETs as an SEMT when they started from the vertically-adjacent buffers as shown in Fig. 14. In this result, number of MSET is only 4 and SETs of MSET were surely injected on sufficiently separated buffers.

TABLE III
Total Number of SET and average SET pulse widths.

| tap-cell interval | # of SET[n/Mbuffer/h] | Avg. width[ps] |
|---|---|---|
| 28$\mu$m | 18.7 | 180 |
| 5$\mu$m | 17.2 | 130 |

TABLE IV
Total number of SET, MSET and SEMT.

| tap-cell interval | SET | MSET | SEMT |
|---|---|---|---|
| 28$\mu$m | 123 | 4 | 7 |
| 5$\mu$m | 110 | 6 | 12 |

As shown in Fig. 12, the proposed circuit can simultaneously measure SEU on the FF. Table V shows SET rate on a buffer and SEU rate on a FF. This result shows SET rate on a buffer is 23x smaller than SEU rate on a FF. For SEU hardened circuit such as DICE latch[11], SET cannot be ignored, especially SET injected on the clock buffer.

## V. Conclusion

We propose an SET pulse width measurement circuit using propagation-induced pulse shrinking on a clock buffer chain on a shift register. Pulse shrinking reduces an SET linearly as it propagates through the clock buffer chain. Pulse shrinking is a critical issue to measure SET pulse width with accuracy in the conventional circuit. On the contrary, the proposed circuit utilizes the pulse shrinking to measure the SET pulse.

TABLE V
Number of SEUs and SETs by the neutron irradiation.

| SEU[n/Mbit/h] | SET[n/Mbuffer/h] | SET/SEU[%] |
|---|---|---|
| 412 | 18.0 | 4.4 |

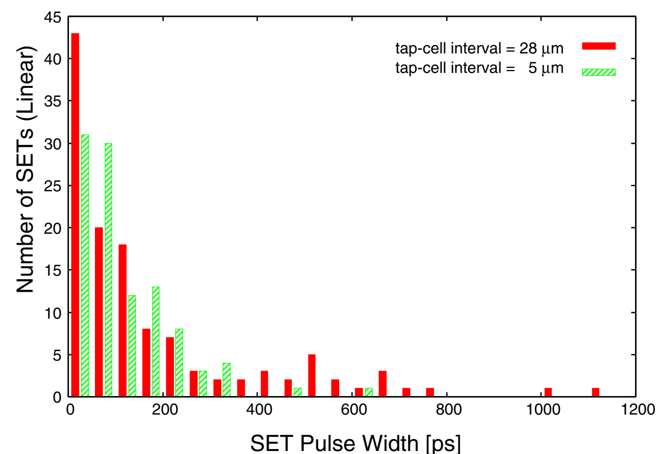

Fig. 11. Distribution of SET pulse width by the neutron irradiation.

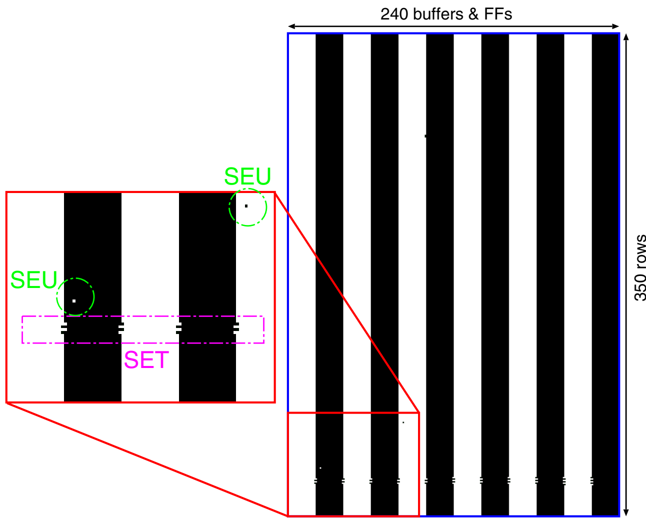

Fig. 12. Measured stripe pattern affected by an SET pulse and two SEUs.

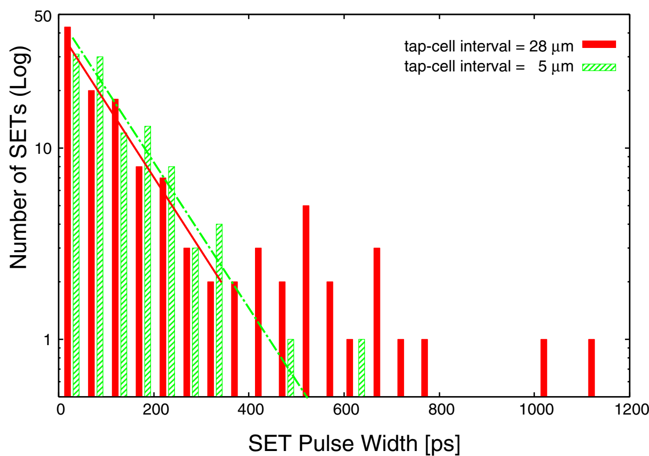

Fig. 13. Distribution of SET pulse width by the neutron irradiation (Number of SETs in log scale).

It achieves much higher accuracy of 1 ps resolution. It is because that a pulse is shrunk by 1 ps thorough one stage of the clock buffer, while the conventional circuit utilizes the delay time of logic gates which is usually over 10 ps.

Experimental results by the neutron irradiation show that SET pulse widths are exponentially-distributed and they are reduced by inserting tap-cell closely. Comparing the pulse width distributions of the closely-placed (every 5 $\mu$m) tap-cell with that of the sparsely-placed (ever 28 $\mu$m) one, the average pulse width is reduced from 180 ps to 130 ps and rate of SET pulses longer than 350 ps is reduced to 9% by it. Tap-cell density is very important thing to mitigate SET. SET rate on a buffer is 23x smaller than SEU rate on a FF. This results shows that if SEU hardened circuit has non-redundant clock buffer, its soft error resilience is only 23x better than that of the conventional FF.

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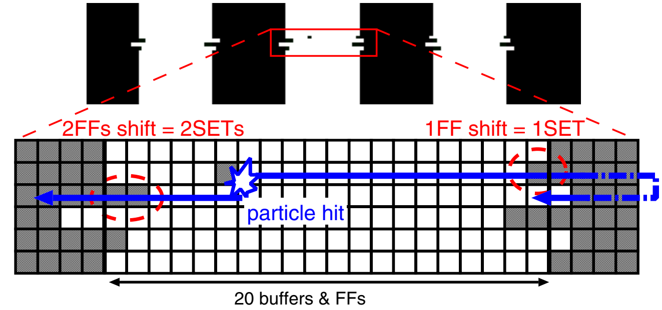

Fig. 14. a measurement result of a Single Event Multiple Transient (SEMT).

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