A Partially-redundant Flip-flip Suitable for Mitigating Single Event Upsets in a FD-SOI Process with Low Performance Overhead

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***Abstract*— We propose a radiation-hardened flip-flop (FF) combined with a transient-fault tolerant (TFT) structure and fabricated test chips in a 65 nm FD-SOI technology. Heavy ion irradiation tests show that the cross section of the proposed TFT FF is about two orders of magnitude lower than that of a standard FF when linear energy transfer of irradiated heavy ions is 69 MeV-cm^2/mg. The TFT FF achieves high error tolerance with 35% area, 15% delay and 9% power overhead, and its energy-delay product is half as large as a conventional stacked FF.**

I. Introduction

Fully-depleted silicon on insulator (FD-SOI) process is one of the most effective solutions to reduce single event effects. It is because a buried oxide layer can block transistors from collecting charge generated by a radiation strike without any performance overhead. However, the amount of improvement in error tolerance is still 10 - 100 times compared to bulk processes [1], [2], [3]. Some countermeasures on circuit structures are required to achieve error tolerance that can be used in a space environment. However, completely-redundant circuits such as DICE latches are excessive for FD-SOI technology [4].

Transistor stacking is a radiation-hardened methodology for FD-SOI processes [5], [6]. In FDSOI processes, single event upsets were caused by the parasitic bipolar effect which temporarily conducts between the drain and source regions of a MOSFET. Therefore, the conduction due to parasitic bipolar effects can be prevented by replacing a single MOSFET with two cascaded MOSFETs (stacked MOSFETs). Compared with redundant circuits, the transistor stacking methodology have less area penalty. However, it have large delay overhead. It is required a radiation-hardened circuit with small area and delay penalties.

In this paper, we propose a radiation-hardened FF combined with a transient-fault tolerant (TFT) structure for FD-SOI technology. The proposed TFT FF, standard FF and conventional stacked FFs were fabricated in a 65 nm process to compare the cross sections of single event upsets by heavy ion irradiation. Experimental tests were performed using Ar and Xe ions with linear energy transfer (LET) values of 16 MeV-cm2/mg and 69 MeV-cm2/mg, respectively.

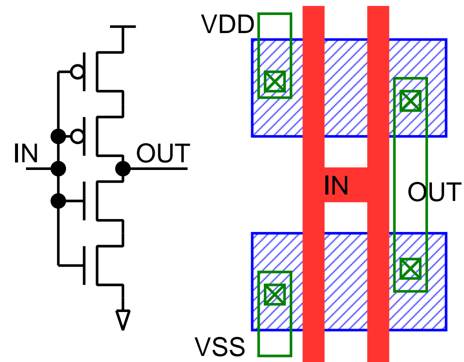

Fig. 1. Stacked inverter [5].

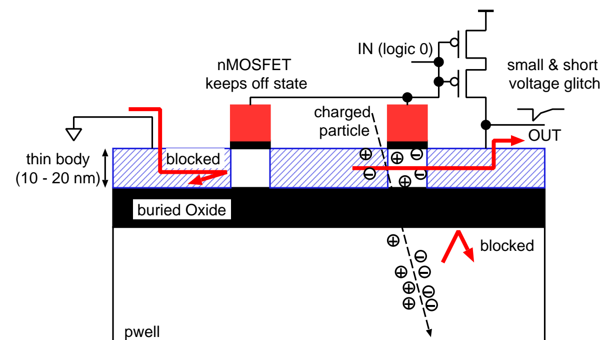

Fig. 2. Mitigation mechanism of the stacked structure.

II. RADIATION HARDENED STRUCTURES SUITABLE FOR FD-SOI PROCESSES

A. Stacked structures

Makihara et al. proposed the stacked inverter (Fig. 1) to mitigate a single event effective in any SOI process [5]. When one of off-state MOSFETs is struck by a charged particle, small amount of charge is collected to the output node because the buried oxide layer blocks charge collection from substrate. Additionally, the current by the bipolar effect completely blocked by the other off-state MOSFET as shown in Fig. 2. The stacked inverter is immune to single event transients (SETs).

The advantage is that there is no additional metal wiring

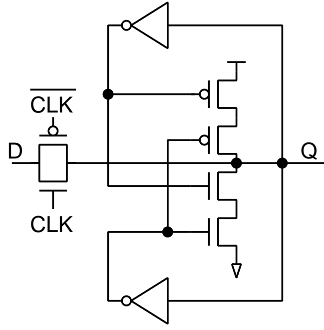

Fig. 3. Schematic diagram of transient fault-tolerant latch [7].

and logic gates can be easily converted to a stacked structure with small area penalty. One of the drawbacks is large delay penalty. Stacked logic gates have approximately four times long propagation delay time of the unstacked logic gate since their input capacitance and output resistance are doubled.

B. Transient-fault-tolerant structure

Omana et al. proposed a radiation-hardened latch for a bulk process as shown in Fig. 3 called TFT latch [7]. The feedback loop of the TFT latch consists of duplicated inverters and the C-element. Thus, an SET pulse from the inverters is blocked by the C-element. In contrast, the output of the C-element is easily flipped by a radiation strike in a bulk process. However, we find that the C-element can be considered as a stacked inverter when two input values are same and it is immune to SETs in a FD-SOI process. As a result, the TFT latch in a FD-SOI process achieves high SEU tolerance equivalent to the stacked structure. The TFT latch has better delay performance than stacked latch structure because the duplicated inverters do not influence delay time.

C. Test chip structure

We fabricated test chips in a 65nm FD-SOI process. The test chips include three kinds of FFs: a standard FF, a stacked FF and the TFT FF. Figs. 4 and 5 show schematic diagrams of the stacked FF and the TFT FF. All FFs construct a shift register to write and read their stored values. Table I shows the normalized circuit performance obtained from post layout simulations. Transistor sizes of each FF are optimized by the downhill simplex method [8] to minimize the energy-delay (ED) product. The ED product of the TFT FF is a half of that of the stacked FF because the delay overhead of the TFT FF is 22% of that of the stacked FF. In the TFT FF, the minimum transistor sizes are used for one of duplicated inverters (INV_P2 and INV_S2 in Fig. 4). Thus, the TFT structure was able to suppress the increase in gate capacitance as well as on-resistance and achieves better ED product than the stacked FF.

III. Heavy ion irradiation tests

A. Experimental setup

Heavy ion experiments were performed at Cyclotron and Radioisotope Center (CYRIC) and Takasaki Ion Accelerators for Advanced Radiation Application (TIARA). We used vertically-incident $^{40}Ar^{8+}$ and $^{129}Xe^{25+}$ ions. Their energy, LET and total fluence are summarized in Table II. As shown in Fig. 6, Ar ion tests at CYRIC were conducted in air and the distance between irradiation port and the test chip is about 2 mm. Therefore, energy and LET of Ar ions can be slightly reduced by air. In contrast, Xe ion tests at TIARA were conducted in a vacuum chamber. In both Ar and Xe ions irradiation tests, four chips in a package (Fig. 7) were

TABLE I
Performance of implemented FFs in the FD-SOI process normalized by the standard FF.

	Area	Setup time + CQ delay		Power	ED
		rise	fall		product
Standard FF	1	1	1	1	1
Stacked FF	1.22	1.68	1.65	1.04	2.89
TFT FF	1.35	1.15	1.14	1.09	1.43

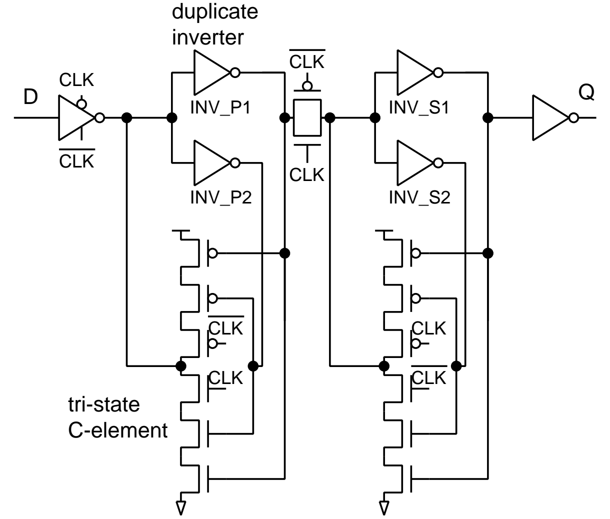

Fig. 4. Schematic diagram of proposed TFT FF.

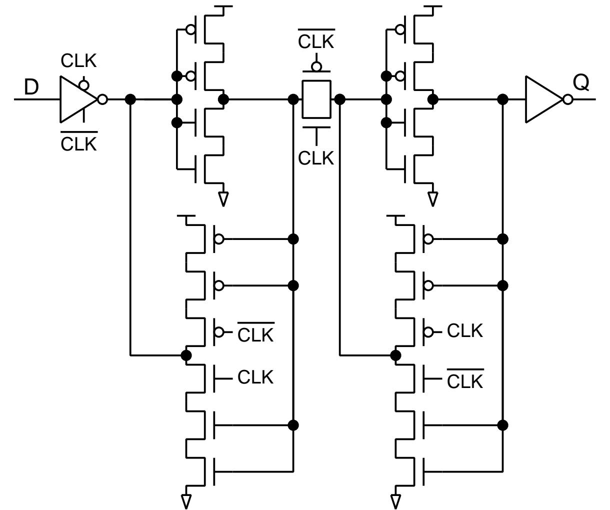

Fig. 5. Schematic diagram of conventional stacked FF.

TABLE II

ENERGY, LET AND TOTAL FLUENCE OF IRRADIATED HEAVY IONS.

ion	Ar	Xe
LET [MeV-cm^2/mg]	16	69
Energy [MeV]	150	455
Fluence [ions/cm^2]	3.8×10^9	5.4×10^8
Test Facility	CYRIC	TIARA
Beam diameter [cm]	2	6

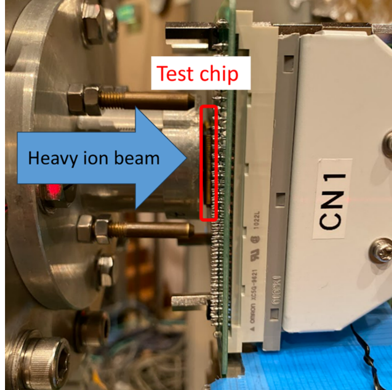

Fig. 6. Experimental setup at CYRIC.

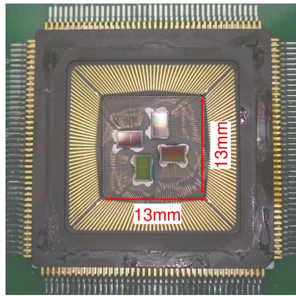

Fig. 7. Four chips in a package to increase measurement results.

used as a measurement target to increase the number of SEU events, which is small enough for the beam diameter because the chip size is 2.0 $\times$ 3.0 mm^2

All heavy ion test were performed in static test conditions. All FFs stored same logic values (All0 or All1) and the supply voltage was set to the nominal voltage of 1.2 V. Heavy ions were irradiated for 30 seconds, and all stored values were read out after irradiation.

B. Experimental results

Fig. 8 shows the cross sections of the FFs by Ar ions for each condition of stored values (Q) and the clock signal (CLK). The error bars in Fig. 8 represent 95% confidence intervals. The results indicate that the Ar-induced SEU rate of the TFT FF is more than three orders of magnitude lower than that of the standard FF in the 65 nm FD-SOI process. The total number of observed SEUs in the TFT FFs is 15. These SEUs are caused by charge sharing between the duplicated inverters and between the series-connected MOSFETs in the C-element [9]. To improve soft error

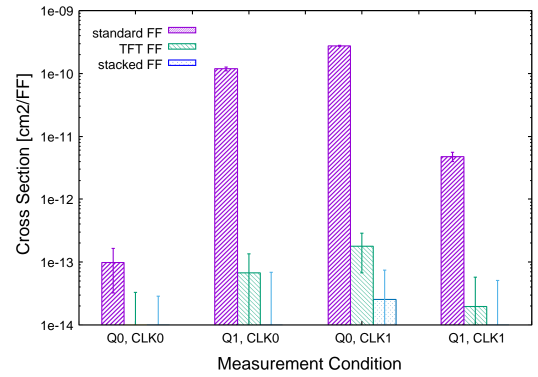

Fig. 8. Ar-ion-induced SEU rates on the 65 nm FD-SOI process.

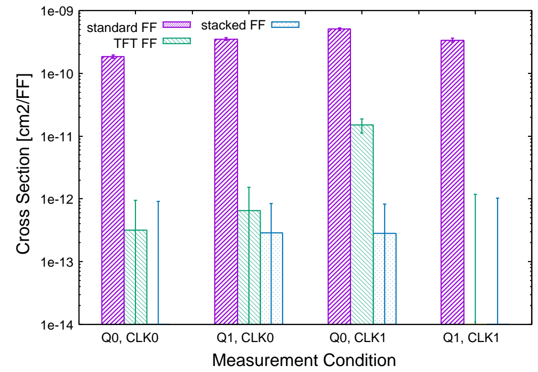

Fig. 9. Xe-ion-induced SEU rates on the 65 nm FD-SOI process.

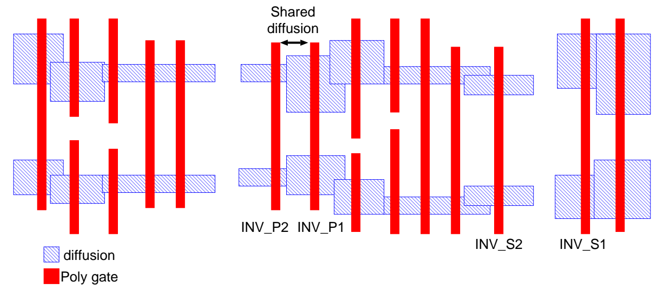

Fig. 10. Simplified layout of the TFT FF.

tolerance of the TFT FF, these critical node pairs should be placed apart as well as redundant FFs in a bulk process [6], [10].

Fig. 9 shows the cross sections of the FFs by Xe ions. Compared with Ar ion results, the cross section of the TFT FF increased by about two orders of magnitude at (Q, CLK) = (0, 1). However, average cross section of the TFT FF is 1/100 of that of the standard FF and the TFT FF achieved sufficient improvement of radiation resistance up to 69 MeV-cm^2/mg. The large increase in the cross section under the condition (Q, CLK) = (0,1) is due to the shared diffusion region of the duplicated inverters. As shown in Fig. 10, the duplicated inverters in the primary latch of the TFT FF, INV_P1 and INV_P2 share diffusion region, while

INV_S1 and INV_S2 in the secondary latch do not share diffusion region. We assume that these differences in layout are observed as differences in the cross section.

The stacked FF achieves higher SEU tolerance than the TFT FF. It is due to the large input capacitance of the stacked structure, which increases the feedback loop delay and critical charge of the stacked FF. Since the delay overhead of the TFT FF is 22% of that of the stacked FF, the TFT FF is more effective if it is connected to critical path. In contrast, the stacked FF can provide better area efficiency and circuit reliability if it is connected to smaller number of logic gates than the critical path.

IV. Conclusions

In this paper, we report cross sections of a radiation-hardened FF combined with the TFT structure and FD-SOI technology. Experimental tests using Ar ions with LET of 16 MeV-cm2/mg show that the TFT FF achieves over 1,000x higher radiation hardness than the standard FF in a 65 nm FD-SOI process with 35%, 15% and 9% increases in area, delay time and power consumption, respectively. Although the TFT FF could not achieve equivalent radiation tolerance of the conventional stacked FF, it can achieve smaller performance overhead while achieving sufficiently high radiation tolerance since the delay overhead of the TFT FF is 22% of that of the stacked FF. To improve the soft error tolerance, each critical node pair of the TFT FF should be placed apart as well as redundant FFs, and diffusion regions of the duplicated inverters should not be shared.

Acknowledgments

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